



## 1A Low-Dropout Regulator with Reverse Current Protection

### FEATURES

- Stable with 1.0µF or Larger Ceramic Output Capacitor
- Input Voltage Range: 2.2V to 5.5V
- Ultra-Low Dropout Voltage: 130mV typ at 1A
- Excellent Load Transient Response—Even With Only 1.0µF Output Capacitor
- NMOS Topology Delivers Low Reverse Leakage Current
- 0.5% Initial Accuracy
- 3% Overall Accuracy Over Line, Load, and Temperature
- Less Than 20nA typical  $I_Q$  in Shutdown Mode
- Thermal Shutdown and Current Limit for Fault Protection
- Available in Multiple Output Voltage Versions
  - Adjustable Output: 1.20V to 5.5V
  - Custom Outputs Available Using Factory Package-Level Programming

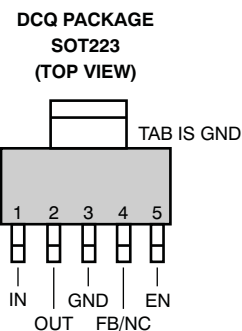
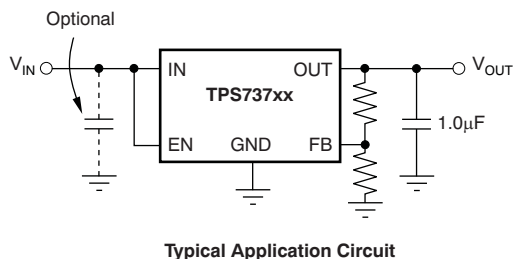
### DESCRIPTION

The TPS737xx family of linear low-dropout (LDO) voltage regulators uses an NMOS pass element in a voltage-follower configuration. This topology is relatively insensitive to output capacitor value and ESR, allowing a wide variety of load configurations. Load transient response is excellent, even with a small 1.0µF ceramic output capacitor. The NMOS topology also allows very low dropout for the die size used.

The TPS737xx family uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 1µA and ideal for portable applications. These devices are protected by thermal shutdown and foldback current limit.

### APPLICATIONS

- Point of Load Regulation for DSPs, FPGAs, ASICs, and Microprocessors
- Post-Regulation for Switching Supplies
- Portable/Battery-Powered Equipment



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**ORDERING INFORMATION<sup>(1)</sup>**

PRODUCT	V <sub>OUT</sub> <sup>(2)</sup>
TPS737xxyyyz	XX is nominal output voltage (for example, 25 = 2.5V, 01 = Adjustable <sup>(3)</sup> ). YYY is package designator. Z is package quantity.

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) Most output voltages from 1.5V to 5.0V in 100mV increments are available on a quick-turn basis using innovative factory package-level programming. Minimum order quantities apply; contact factory for details and availability.
- (3) For fixed 1.2V operation, tie FB to OUT.

**ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range unless otherwise noted<sup>(1)</sup>

	TPS737xx	UNIT
V <sub>IN</sub> range	-0.3 to +6.0	V
V <sub>EN</sub> range	-0.3 to +6.0	V
V <sub>OUT</sub> range	-0.3 to +5.5	V
Peak output current	Internally limited	
Output short-circuit duration	Indefinite	
Continuous total power dissipation	See <a href="#">Dissipation Ratings Table</a>	
Junction temperature range, T <sub>J</sub>	-55 to +150	°C
Storage temperature range	-65 to +150	°C
ESD rating, HBM	2	kV
ESD rating, CDM	500	V

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the *Electrical Characteristics* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

**POWER DISSIPATION RATINGS<sup>(1)</sup>**

BOARD	PACKAGE	R <sub>θJC</sub>	R <sub>θJA</sub>	DERATING FACTOR ABOVE T <sub>A</sub> = +25°C	T <sub>A</sub> ≤ +25°C POWER RATING	T <sub>A</sub> = +70°C POWER RATING	T <sub>A</sub> = +85°C POWER RATING
Low-K <sup>(2)</sup>	DCQ	15°C/W	53°C/W	18.9mW/°C	1.89W	1.04W	0.76W

- (1) See [Power Dissipation](#) in the [Applications](#) section for more information related to thermal design.
- (2) The JEDEC Low-K (1s) board design used to derive this data was a 3-inch × 3-inch, 2-layer board with 2-ounce copper traces on top of the board.

**ELECTRICAL CHARACTERISTICS**

Over operating temperature range ( $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ),  $V_{IN} = V_{OUT(nom)} + 1.0\text{V}^{(1)}$ ,  $I_{OUT} = 10\text{mA}$ ,  $V_{EN} = 2.2\text{V}$ , and  $C_{OUT} = 2.2\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = +25^\circ\text{C}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$	Input voltage range <sup>(1)(2)</sup>		2.2		5.5	V
$V_{FB}$	Internal reference (TPS73701)	$T_J = +25^\circ\text{C}$	1.198	1.20	1.210	V
$V_{OUT}$	Output voltage range (TPS73701)		$V_{FB}$		$5.5 - V_{DO}$	V
	Accuracy <sup>(1)(3)</sup> over $V_{IN}$ , $I_{OUT}$ , and T	Nominal	$T_J = +25^\circ\text{C}$	-1.0		+1.0
		$V_{OUT} + 0.5\text{V} \leq V_{IN} \leq 5.5\text{V};$ $10\text{mA} \leq I_{OUT} \leq 1\text{A}$	-3.0	$\pm 0.5$	+3.0	
$\Delta V_{OUT}\%/\Delta V_{IN}$	Line regulation <sup>(1)</sup>	$V_{OUT(nom)} + 0.5\text{V} \leq V_{IN} \leq 5.5\text{V}$		0.01		%/V
$\Delta V_{OUT}\%/\Delta I_{OUT}$	Load regulation	$1\text{mA} \leq I_{OUT} \leq 1\text{A}$		0.002		%/mA
		$10\text{mA} \leq I_{OUT} \leq 1\text{A}$		0.0005		
$V_{DO}$	Dropout voltage <sup>(4)</sup> ( $V_{IN} = V_{OUT(nom)} - 0.1\text{V}$ )	$I_{OUT} = 1\text{A}$		130	500	mV
$Z_O(\text{DO})$	Output impedance in dropout	$2.2\text{V} \leq V_{IN} \leq V_{OUT} + V_{DO}$		0.25		$\Omega$
$I_{CL}$	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(nom)}$	1.05	1.6	2.2	A
$I_{SC}$	Short-circuit current	$V_{OUT} = 0\text{V}$		450		mA
$I_{REV}$	Reverse leakage current <sup>(5)</sup> ( $-I_{IN}$ )	$V_{EN} \leq 0.5\text{V}$ , $0\text{V} \leq V_{IN} \leq V_{OUT}$		0.1		$\mu\text{A}$
$I_{GND}$	Ground pin current	$I_{OUT} = 10\text{mA}$ ( $I_Q$ )		400		$\mu\text{A}$
		$I_{OUT} = 1\text{A}$		800		
$I_{SHDN}$	Shutdown current ( $I_{GND}$ )	$V_{EN} \leq 0.5\text{V}$ , $V_{OUT} \leq V_{IN} \leq 5.5$		20		nA
$I_{FB}$	FB pin current (TPS73701)			0.1	0.6	$\mu\text{A}$
PSRR	Power-supply rejection ratio (ripple rejection)	$f = 100\text{Hz}$ , $I_{OUT} = 1\text{A}$ , $V_{IN} = V_{OUT} + 1\text{V}$		58		dB
		$f = 10\text{kHz}$ , $I_{OUT} = 1\text{A}$ , $V_{IN} = V_{OUT} + 1\text{V}$		37		
$V_N$	Output noise voltage BW = 10Hz – 100kHz	$C_{OUT} = 10\mu\text{F}$		$27 \times V_{OUT}$		$\mu\text{V}_{RMS}$
$t_{STR}$	Startup time	$V_{OUT} = 3\text{V}$ , $R_L = 30\Omega$ , $C_{OUT} = 1\mu\text{F}$		600		$\mu\text{s}$
$V_{EN(HI)}$	Enable high (enabled)		1.7		$V_{IN}$	V
$V_{EN(LO)}$	Enable low (shutdown)		0		0.5	V
$I_{EN(HI)}$	Enable pin current (enabled)	$V_{EN} = 5.5\text{V}$		20		nA
$T_{SD}$	Thermal shutdown temperature	Shutdown, temperature increasing		+160		$^\circ\text{C}$
		Reset, temperature decreasing		+140		
$T_J$	Operating junction temperature		-40		+125	$^\circ\text{C}$

(1) Minimum  $V_{IN} = V_{OUT} + V_{DO}$  or 2.2V, whichever is greater.

(2) For  $V_{OUT(nom)} < 1.6\text{V}$ , when  $V_{IN} \leq 1.6\text{V}$ , the output will lock to  $V_{IN}$  and may result in an over-voltage condition on the output. To avoid this situation, disable the device before powering down  $V_{IN}$ .

(3) Tolerance of external resistors not included in this specification.

(4)  $V_{DO}$  is not measured for fixed output versions with  $V_{OUT(nom)} < 2.3\text{V}$  since minimum  $V_{IN} = 2.2\text{V}$ .

(5) Refer to the [Applications](#) section for more information.

FUNCTIONAL BLOCK DIAGRAMS

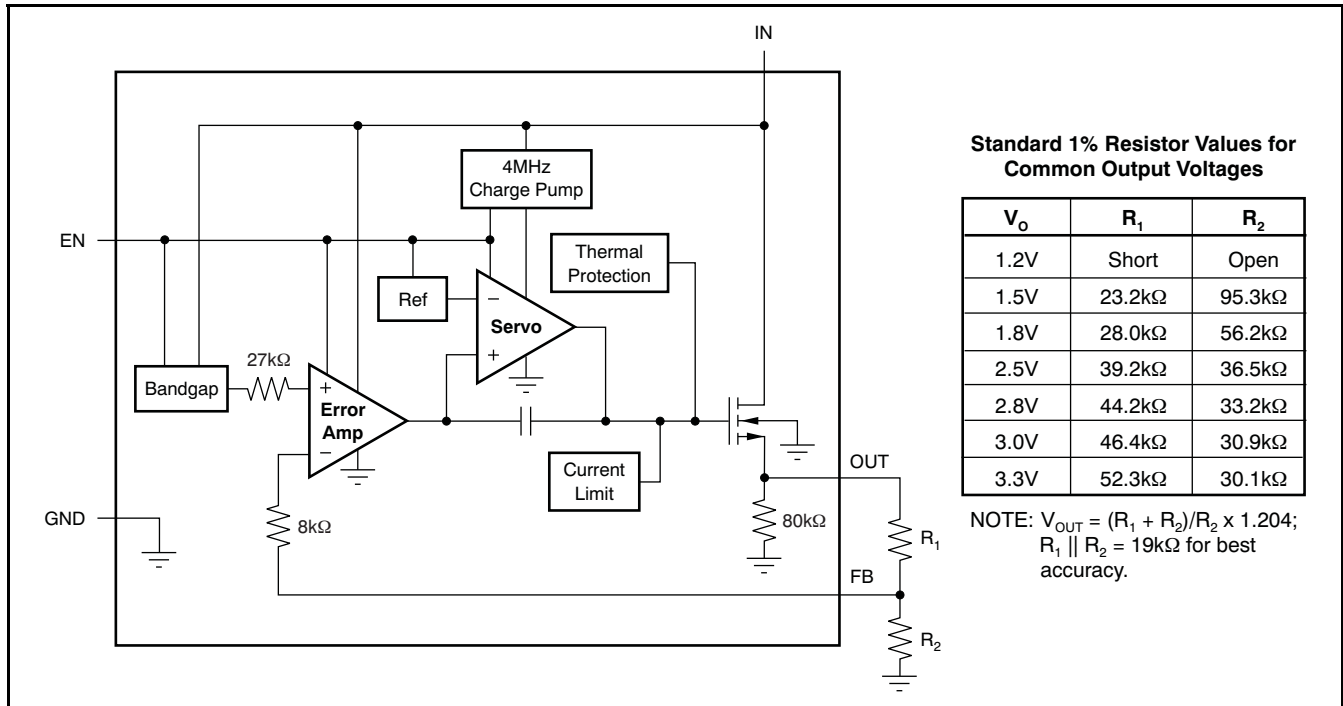


Figure 1. Adjustable Voltage Version

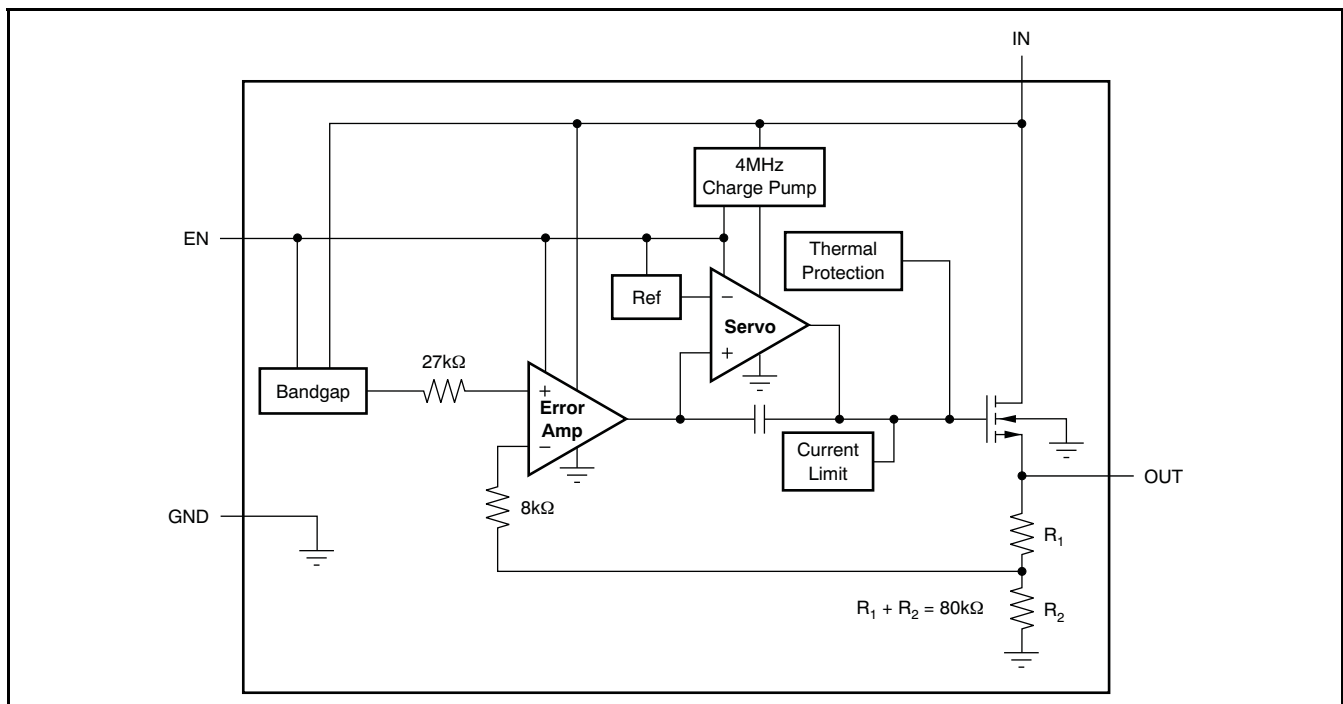
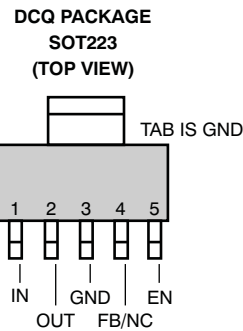


Figure 2. Fixed-Voltage Version

## PIN ASSIGNMENTS



**Table 1. Terminal Functions**

NAME	SOT223 (DCQ) PIN NO.	DESCRIPTION
IN	1	Unregulated input supply
GND	3, TAB	Ground
EN	5	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. Refer to the <a href="#">Shutdown</a> section under <a href="#">Applications Information</a> for more details. EN can be connected to IN if not used.
FB	4	Adjustable voltage version only—this is the input to the control loop error amplifier, and is used to set the output voltage of the device.
OUT	2	Regulator output. A 1.0 $\mu$ F or larger capacitor of any type is required for stability.
NC	—	Not connected

**TYPICAL CHARACTERISTICS**

For all voltage versions at  $T_J = +25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 1.0\text{V}$ ,  $I_{OUT} = 10\text{mA}$ ,  $V_{EN} = 2.2\text{V}$ , and  $C_{OUT} = 2.2\mu\text{F}$ , unless otherwise noted.

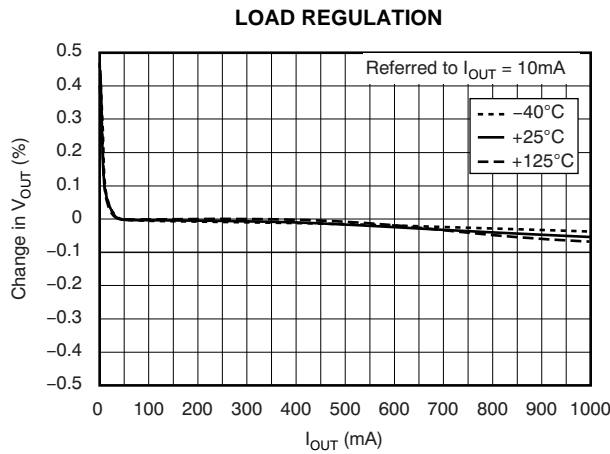


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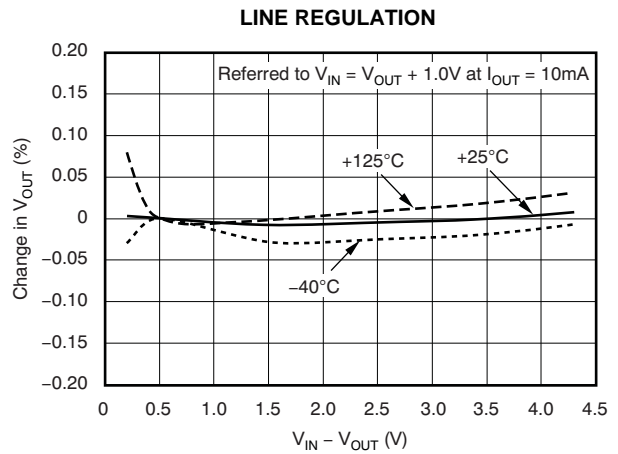


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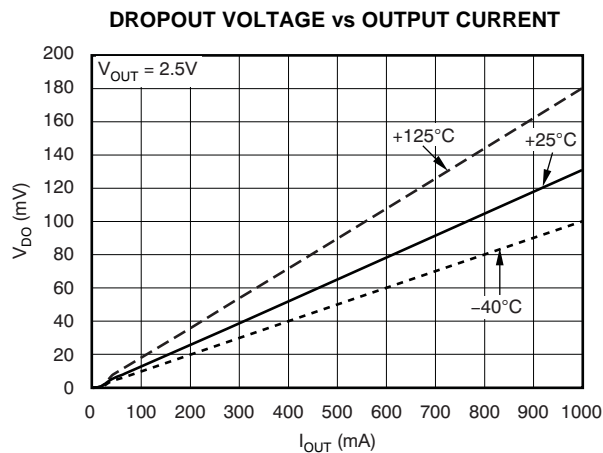


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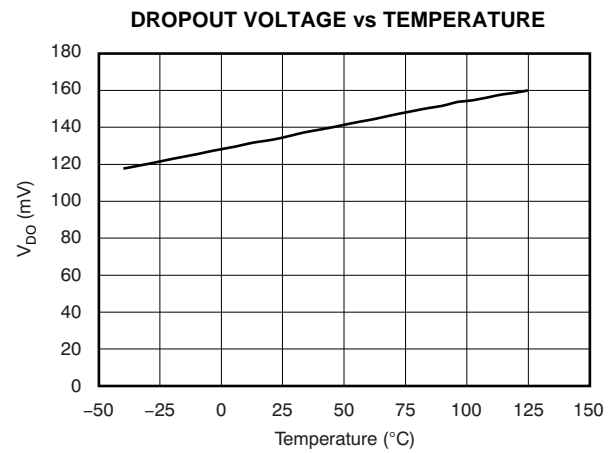


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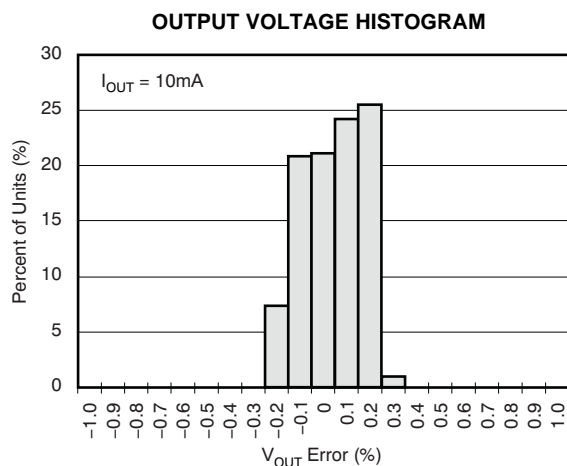


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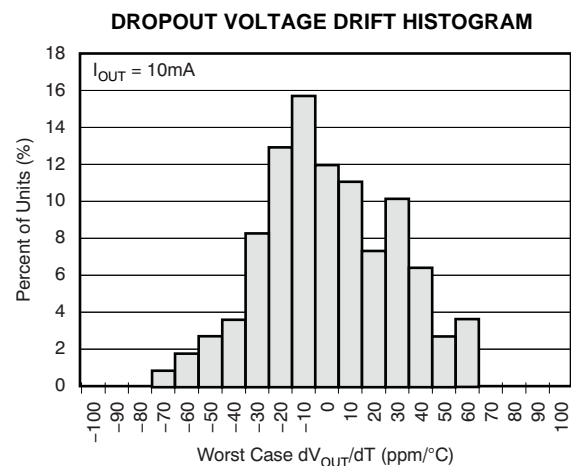


Figure 8.

**TYPICAL CHARACTERISTICS (continued)**

For all voltage versions at  $T_J = +25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 1.0\text{V}$ ,  $I_{OUT} = 10\text{mA}$ ,  $V_{EN} = 2.2\text{V}$ , and  $C_{OUT} = 2.2\mu\text{F}$ , unless otherwise noted.

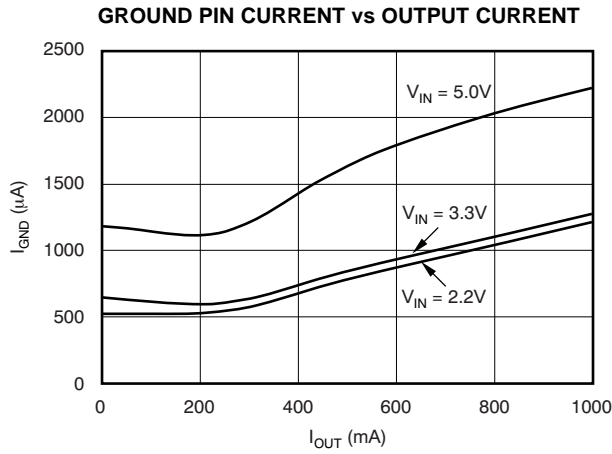


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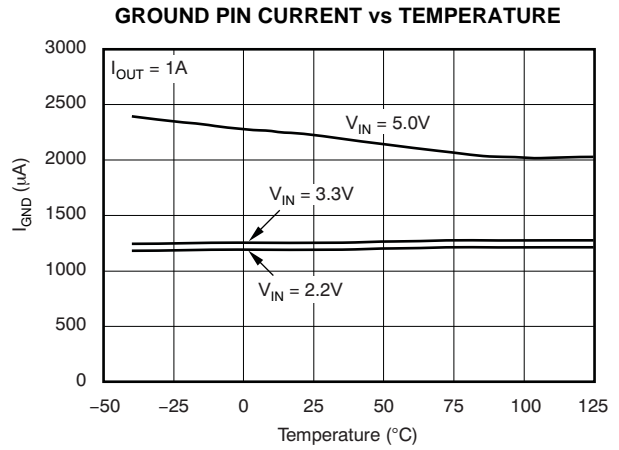


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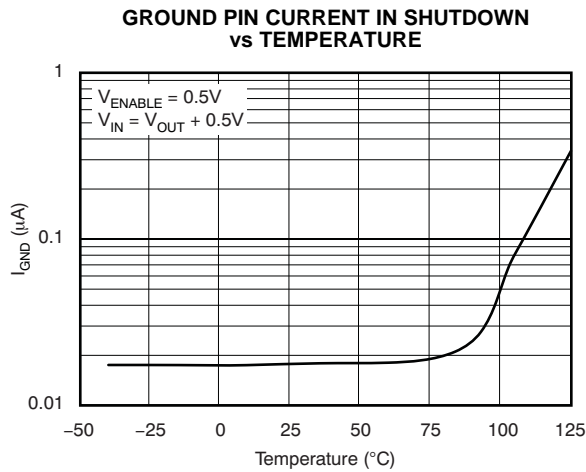


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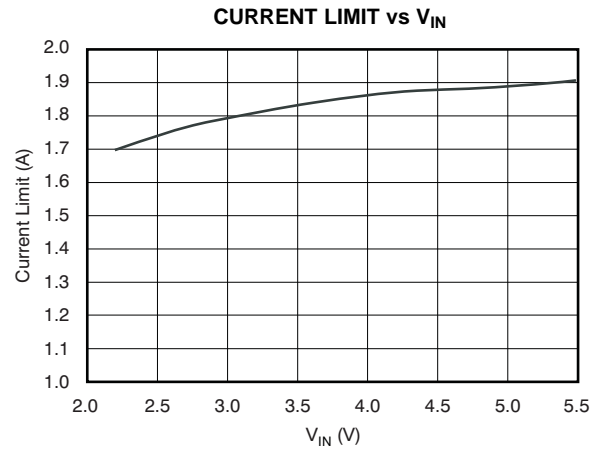


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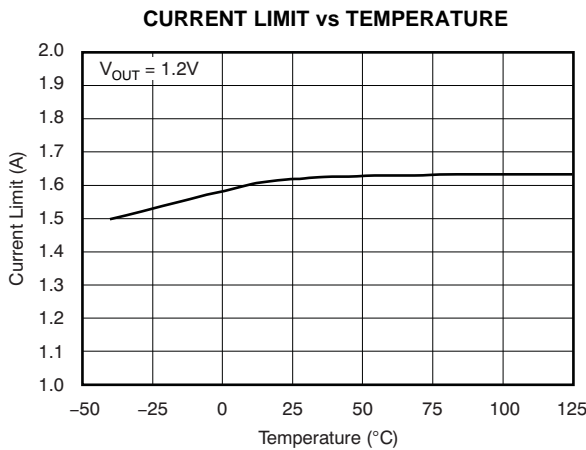


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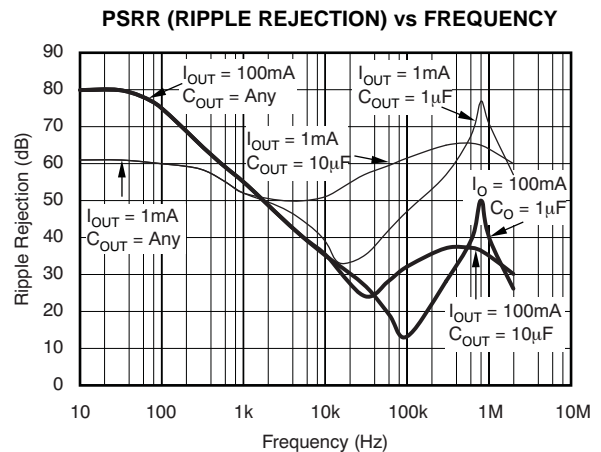


Figure 14.

**TYPICAL CHARACTERISTICS (continued)**

For all voltage versions at  $T_J = +25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 1.0\text{V}$ ,  $I_{OUT} = 10\text{mA}$ ,  $V_{EN} = 2.2\text{V}$ , and  $C_{OUT} = 2.2\mu\text{F}$ , unless otherwise noted.

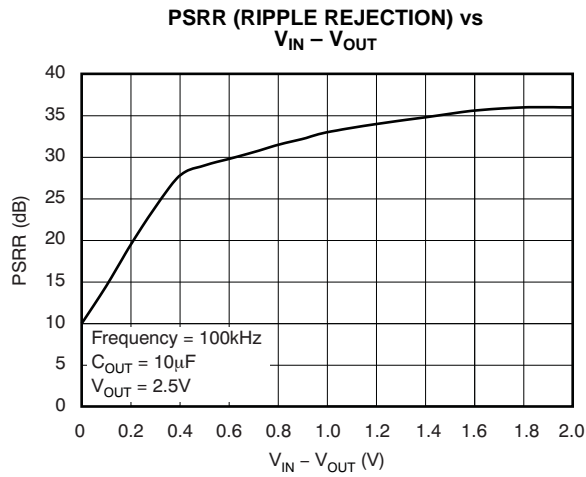


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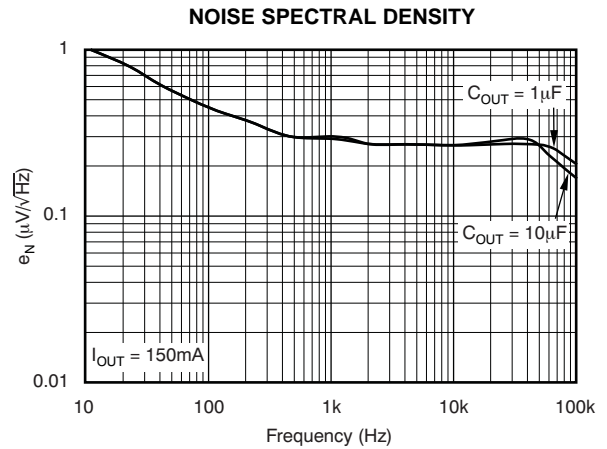


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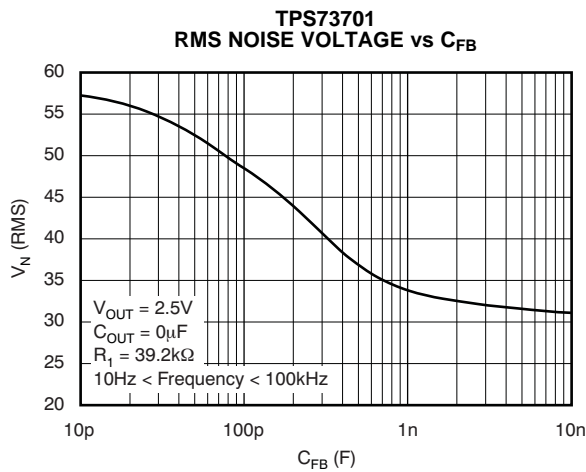


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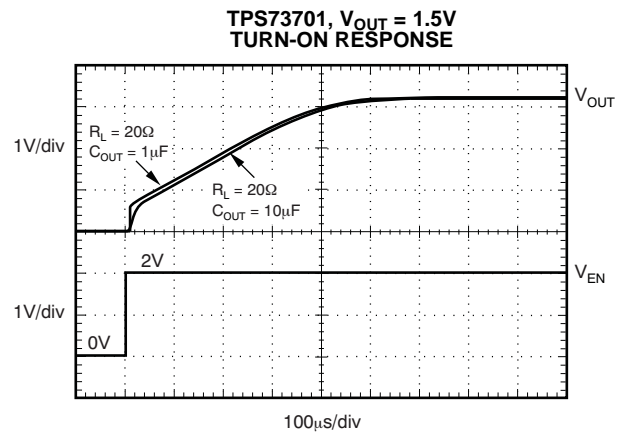


Figure 18.

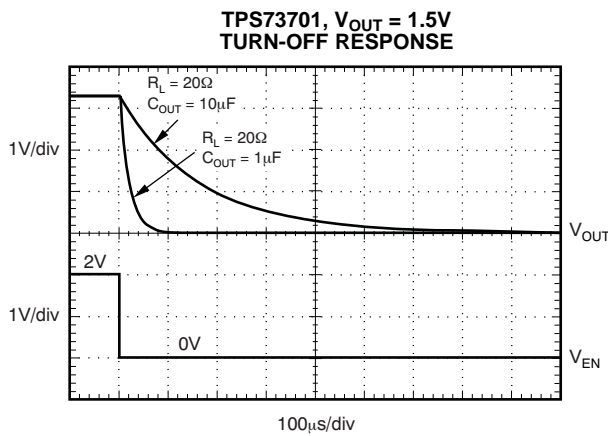


Figure 19.

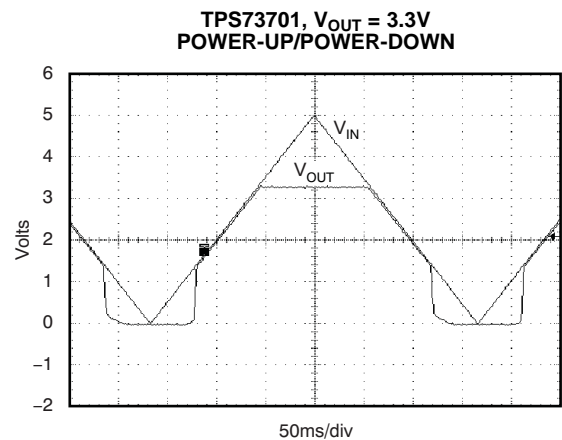


Figure 20.



**TYPICAL CHARACTERISTICS (continued)**

For all voltage versions at  $T_J = +25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 1.0\text{V}$ ,  $I_{OUT} = 10\text{mA}$ ,  $V_{EN} = 2.2\text{V}$ , and  $C_{OUT} = 2.2\mu\text{F}$ , unless otherwise noted.

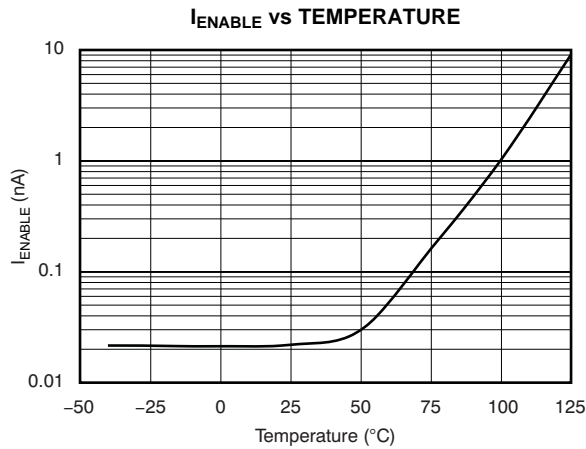


Figure 21.

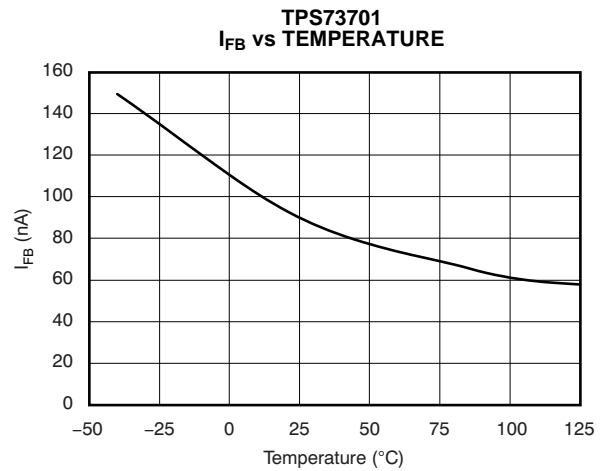


Figure 22.

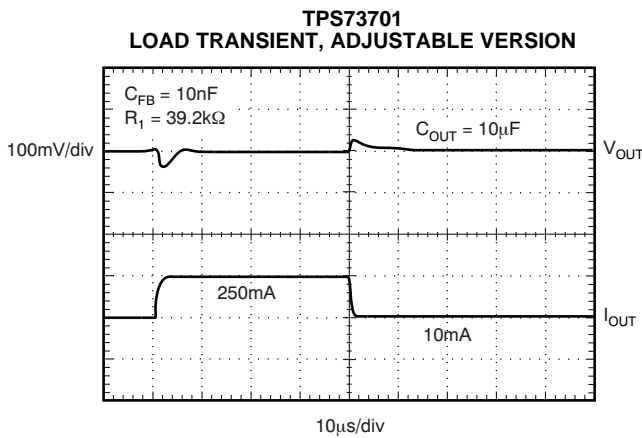


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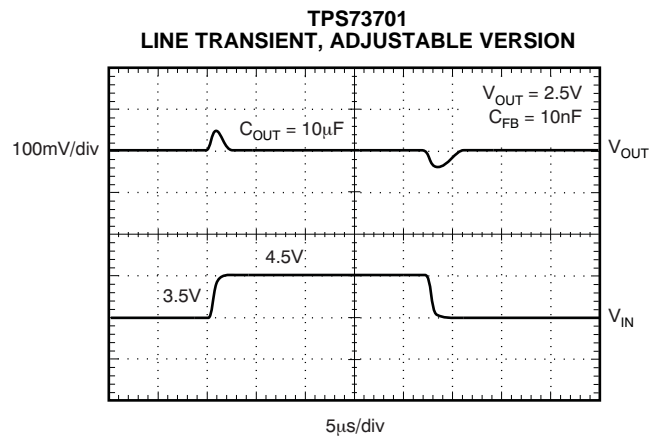
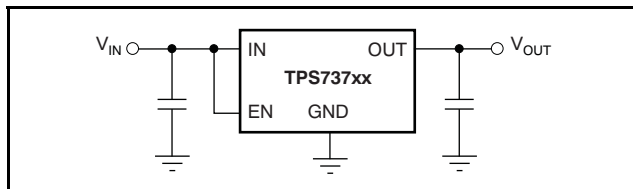


Figure 24.

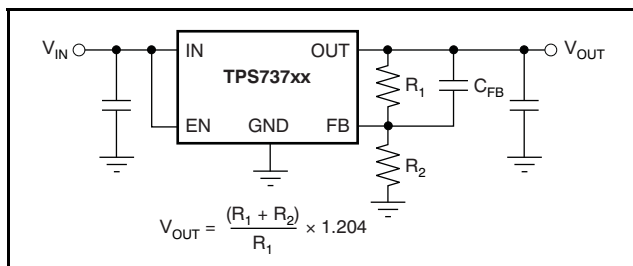
## APPLICATION INFORMATION

The TPS737xx belongs to a family of new generation LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features combined with an enable input make the TPS737xx ideal for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and over-current protection, including foldback current limit.

Figure 25 shows the basic circuit connections for the fixed voltage models. Figure 26 gives the connections for the adjustable output version (TPS73701).



**Figure 25. Typical Application Circuit for Fixed-Voltage Versions**



**Figure 26. Typical Application Circuit for Adjustable-Voltage Versions**

$R_1$  and  $R_2$  can be calculated for any output voltage using the formula shown in Figure 26. Sample resistor values for common output voltages are shown in Figure 2.

For best accuracy, make the parallel combination of  $R_1$  and  $R_2$  approximately equal to  $19\text{k}\Omega$ . This  $19\text{k}\Omega$ , in addition to the internal  $8\text{k}\Omega$  resistor, presents the same impedance to the error amp as the  $27\text{k}\Omega$  bandgap reference output. This impedance helps compensate for leakages into the error amp terminals.

## INPUT AND OUTPUT CAPACITOR REQUIREMENTS

Although an input capacitor is not required for stability, it is good analog design practice to connect a  $0.1\mu\text{F}$  to  $1\mu\text{F}$  low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS737xx requires a  $1.0\mu\text{F}$  output capacitor for stability. It is designed to be stable for all available types and values of capacitors. In applications where  $V_{\text{IN}} - V_{\text{OUT}} < 0.5\text{V}$  and multiple low ESR capacitors are in parallel, ringing may occur when the product of  $C_{\text{OUT}}$  and total ESR drops below  $50\text{n}\Omega\text{F}$ . Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance will meet this requirement.

## OUTPUT NOISE

A precision bandgap reference is used to generate the internal reference voltage,  $V_{\text{REF}}$ . This reference is the dominant noise source within the TPS737xx and it generates approximately  $32\mu\text{V}_{\text{RMS}}$  (10Hz to 100kHz) at its output. The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32\mu\text{V}_{\text{RMS}} \times \frac{(R_1 + R_2)}{R_2} = 32\mu\text{V}_{\text{RMS}} \times \frac{V_{\text{OUT}}}{V_{\text{REF}}} \quad (1)$$

Since the value of  $V_{\text{REF}}$  is  $1.2\text{V}$ , this relationship reduces to:

$$V_N(\mu\text{V}_{\text{RMS}}) = 27 \left( \frac{\mu\text{V}_{\text{RMS}}}{\text{V}} \right) \times V_{\text{OUT}} (\text{V}) \quad (2)$$

Connecting a feedback capacitor,  $C_{\text{FB}}$ , from the output to the FB pin reduces output noise and improve load transient performance. This capacitor should be limited to  $0.1\mu\text{F}$ .

The TPS737xx uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above  $V_{\text{OUT}}$ . The charge pump generates  $\sim 250\mu\text{V}$  of switching noise at  $\sim 2\text{MHz}$ ; however, charge-pump noise contribution is negligible at the output of the regulator for most values of  $I_{\text{OUT}}$  and  $C_{\text{OUT}}$ .

## BOARD LAYOUT RECOMMENDATION TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the printed circuit board (PCB) be designed with separate ground planes for  $V_{IN}$  and  $V_{OUT}$ , with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

## INTERNAL CURRENT LIMIT

The TPS737xx internal current limit helps protect the regulator during fault conditions. Foldback helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when  $V_{OUT}$  drops below 0.5V.

## SHUTDOWN

The Enable pin is active high and is compatible with standard TTL-CMOS levels.  $V_{EN}$  below 0.5V (max) turns the regulator off and drops the ground pin current to approximately 10nA. When shutdown capability is not required, the Enable pin can be connected to  $V_{IN}$ . When a pull-up resistor is used, and operation down to 1.8V is required, use pull-up resistor values below 50k $\Omega$ .

## DROPOUT VOLTAGE

The TPS737xx uses an NMOS pass transistor to achieve extremely low dropout. When  $(V_{IN} - V_{OUT})$  is less than the dropout voltage ( $V_{DO}$ ), the NMOS pass device is in its linear region of operation and the input-to-output resistance is the  $R_{DS, ON}$  of the NMOS pass element.

For large step changes in load current, the TPS737xx requires a larger voltage drop from  $V_{IN}$  to  $V_{OUT}$  to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the dc dropout. Values of  $V_{IN} - V_{OUT}$  above this line ensure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom ( $V_{IN}$  to  $V_{OUT}$  voltage drop). Under worst-case conditions [full-scale instantaneous load change with  $(V_{IN} - V_{OUT})$  close to dc dropout levels], the TPS737xx can take a couple of hundred microseconds to return to the specified regulation accuracy.

## TRANSIENT RESPONSE

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without a 1.0 $\mu$ F output capacitor. As with any regulator, the addition of additional capacitance from the output pin to ground reduces undershoot magnitude but increases duration. In the adjustable version, the addition of a capacitor,  $C_{FB}$ , from the output to the adjust pin will also improve the transient response.

The TPS737xx does not have active pull-down when the output is over-voltage. This architecture allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This architecture also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor  $C_{OUT}$  and the internal/external load resistance. The rate of decay is given by:

(Fixed voltage version)

$$\frac{dV}{dT} = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel R_{LOAD}} \quad (3)$$

(Adjustable voltage version)

$$\frac{dV}{dT} = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel (R_1 + R_2) \parallel R_{LOAD}} \quad (4)$$

## REVERSE CURRENT

The NMOS pass element of the TPS737xx provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the enable pin must be driven low before the input voltage is removed. If this is not done, the pass element may be left on because of stored charge on the gate.

After the enable pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Note that reverse current is specified as the current flowing out of the IN pin because of voltage applied on the OUT pin. There will be additional current flowing into the OUT pin as a result of the 80k $\Omega$  internal resistor divider to ground (see [Figure 1](#) and [Figure 2](#)).

For the TPS73701, reverse current may flow when  $V_{FB}$  is more than 1.0V above  $V_{IN}$ .

## THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS737xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS737xx into thermal shutdown will degrade device reliability.

## POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are shown in the [Power Dissipation Ratings](#) table. Using heavier copper will increase the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers will also improve the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation ( $P_D$ ) is equal to the product of the output current times the voltage drop across the output pass element ( $V_{IN}$  to  $V_{OUT}$ ):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (5)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

## Package Mounting

Solder pad footprint recommendations for the TPS737xx are presented in Application Bulletin *Solder Pad Recommendations for Surface-Mount Devices* ([SBFA015](#)), available from the Texas Instruments web site at [www.ti.com](http://www.ti.com).

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS73701DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73701DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73701DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS73701DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

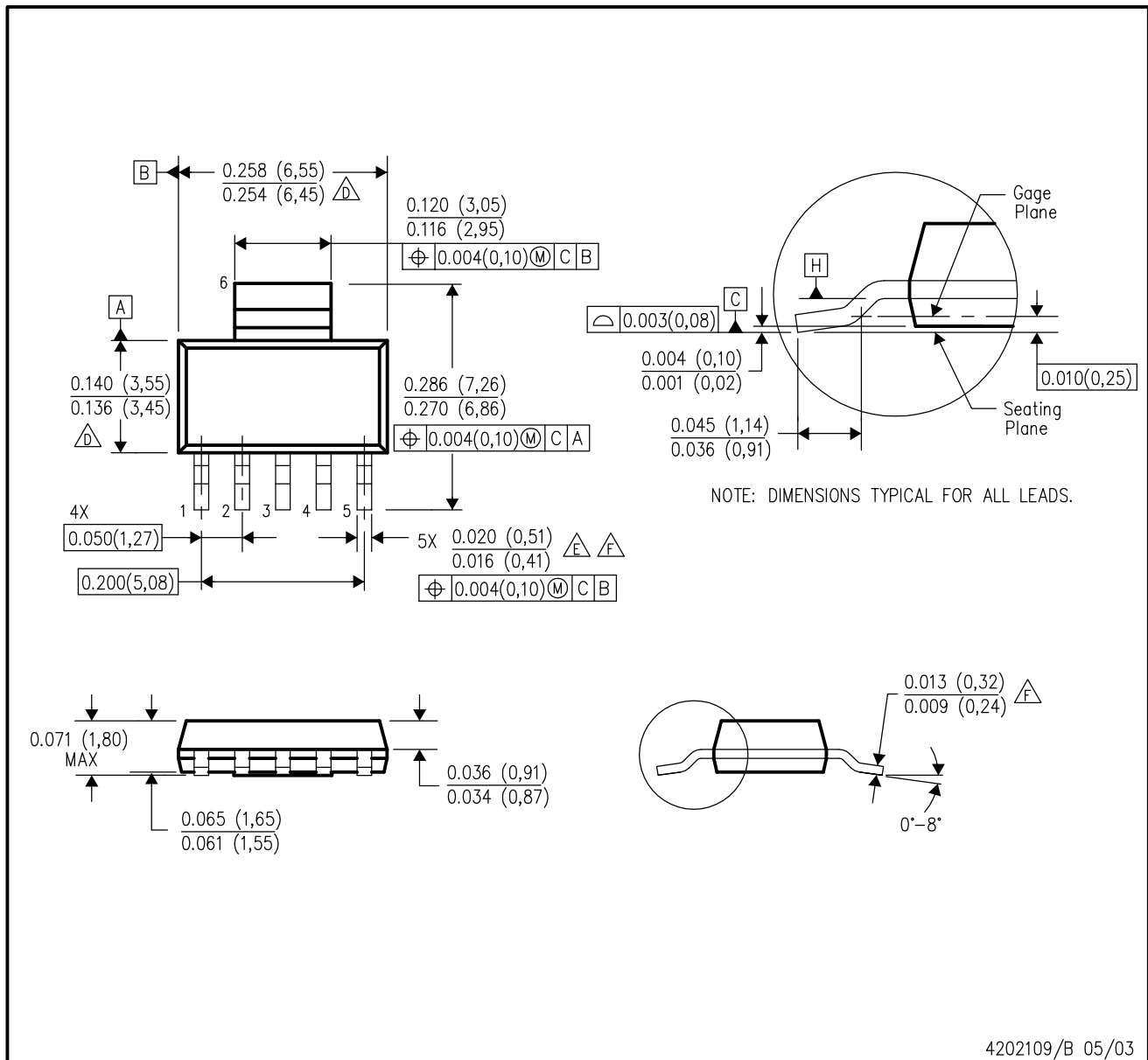
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DCQ (R-PDSO-G6)

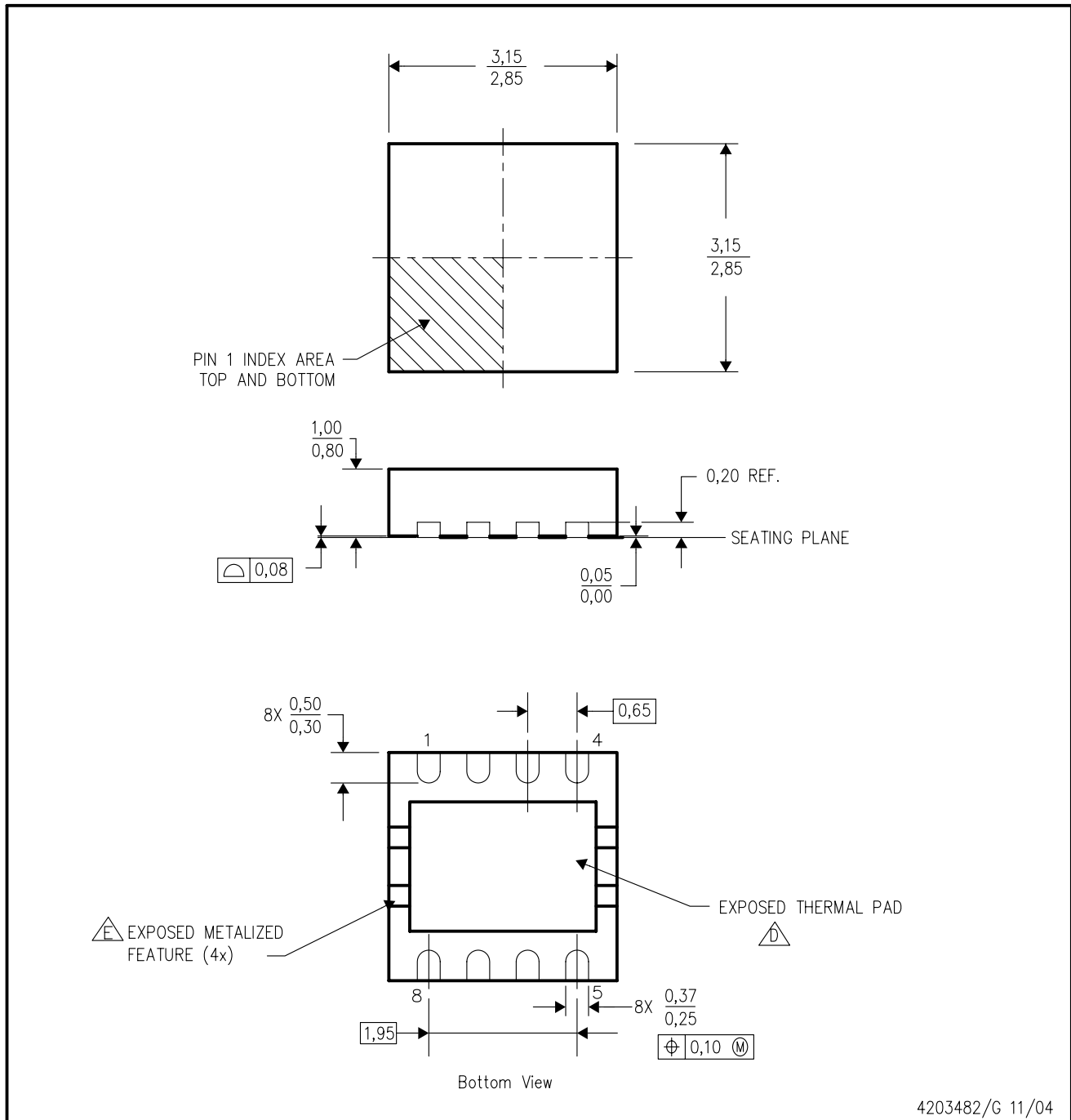
PLASTIC SMALL-OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Controlling dimension in inches.
  - $\triangle D$  Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
  - $\triangle E$  Lead width dimension does not include dambar protrusion.
  - $\triangle F$  Lead width and thickness dimensions apply to solder plated leads.
  - G. Interlead flash allow 0.008 inch max.
  - H. Gate burr/protrusion max. 0.006 inch.
  - I. Datums A and B are to be determined at Datum H.
  - J. Package dimensions per JEDEC outline drawing TO-261, issue B, dated Feb. 1999. This variation is not yet included.

DRB (S-PDSO-N8)

PLASTIC SMALL OUTLINE



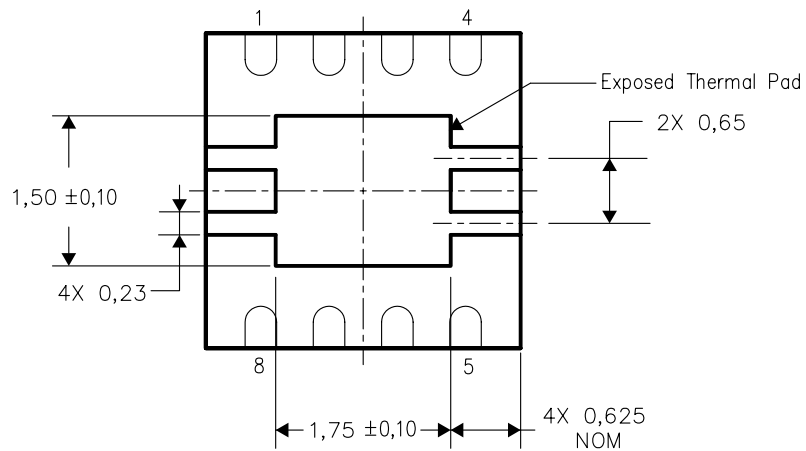
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Small Outline No-Lead (SON) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - Metalized features are supplier options and may not be on the package.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



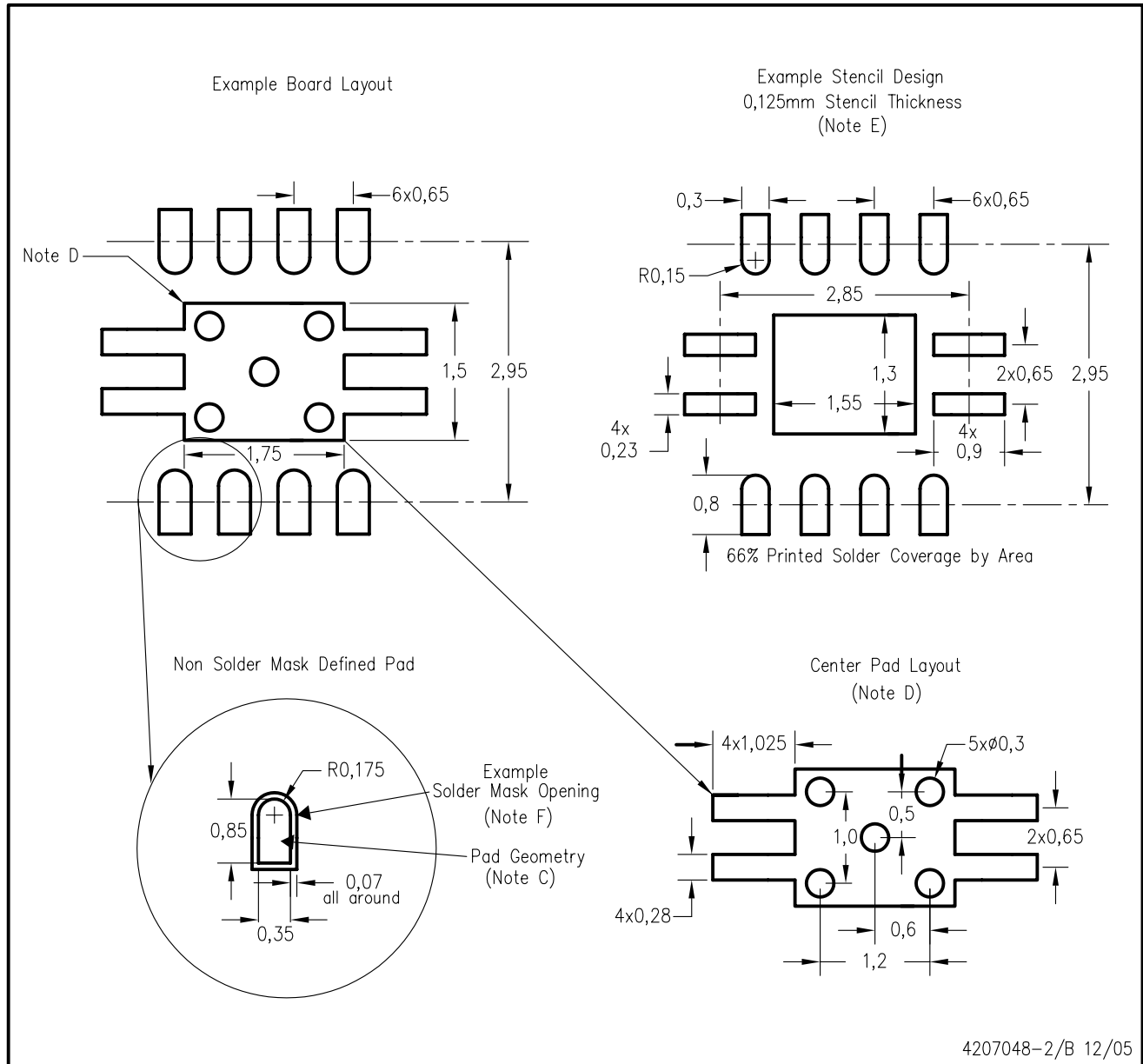
Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions



DRB (S-PDSO-N8)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for solder mask tolerances.

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