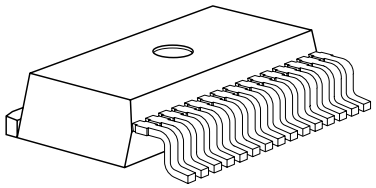
Data Sheet

1 Overview



P-TO263-15-1

1.1 Features

- Quad D-MOS switch
- Free configurable as bridge or quad-switch
- Optimized for DC motor management applications
- Low $R_{DS\ ON}$: 26 mΩ high-side switch, 14 mΩ low-side switch (typical values @ 25 °C)
- Maximum peak current: typ. 42 A @ 25 °C
- Very low quiescent current: typ. 4 µA @ 25 °C
- Small outline, thermal optimized PowerPak
- Load and GND-short-circuit-protection
- Operates up to 40 V
- Status flag for over temperature
- Open load detection in Off-mode
- Overtemperature shut down with hysteresis
- Internal clamp diodes
- Isolated sources for external current sensing
- Under-voltage detection with hysteresis

Type	Ordering Code	Package
BTS 781 GP	Q67006-A9526	P-TO263-15-1

1.2 Description

The **BTS 781 GP** is part of the **TrilithIC** family containing three dies in one package: One double high-side switch and two low-side switches. The drains of these three vertical DMOS chips are mounted on separated leadframes. The sources are connected to individual pins, so the **BTS 781 GP** can be used in H-bridge- as well as in any other configuration. The double high-side is manufactured in **SMART SIPMOS**® technology which combines low $R_{DS\ ON}$ vertical DMOS power stages with CMOS control circuit. The high-side switch is fully protected and contains the control and diagnosis circuit. To achieve low $R_{DS\ ON}$ and fast switching performance, the low-side switches are manufactured in **S-FET 2** logic level technology. The equivalent standard product is the **SPD30N06S2L-13**.

1.3 Pin Configuration
(top view)

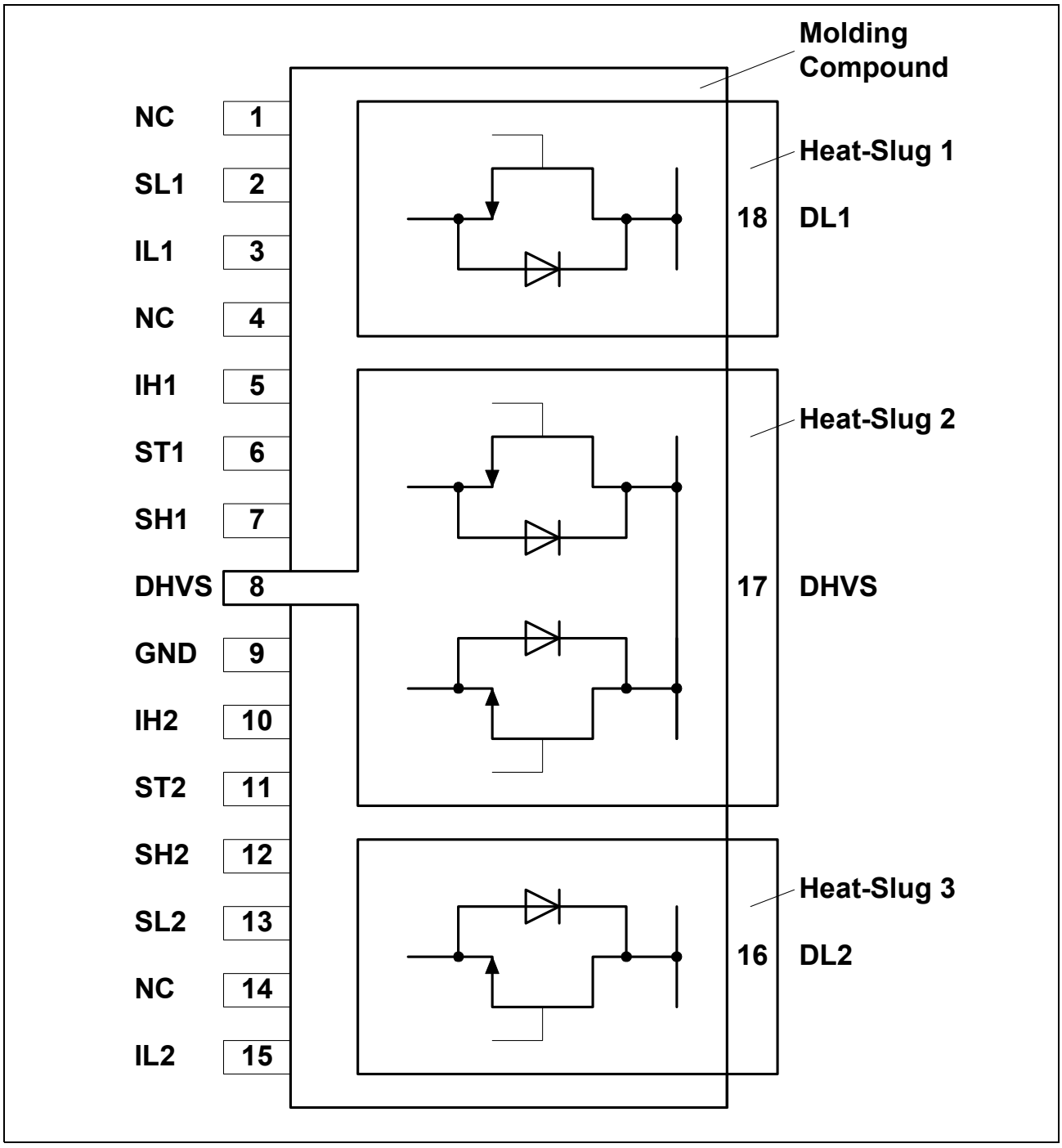


Figure 1

1.4 Pin Definitions and Functions

Pin No.	Symbol	Function
1	NC	Not connected
2	**SL1**	**Source of low-side switch 1**
3	IL1	Analog input of low-side switch 1
4	NC	Not connected
5	IH1	Digital input of high-side switch 1
6	ST1	Status of high-side switch 1; open Drain output
7	**SH1**	**Source of high-side switch 1**
8	**DHVS**	**Drain of high-side switches and power supply voltage**
9	GND	Ground of high-side switches
10	IH2	Digital input of high-side switch 2
11	ST2	Status of high-side switch 2; open Drain output
12	**SH2**	**Source of high-side switch 2**
13	**SL2**	**Source of low-side switch 2**
14	NC	Not connected
15	IL2	Analog input of low-side switch 2
16	**DL2**	**Drain of low-side switch 2** **Heat-Slug 3**
17	**DHVS**	**Drain of high-side switches and power supply voltage** **Heat-Slug 2**
18	**DL1**	**Drain of low-side switch 1** **Heat-Slug 1**

Pins written in **bold type** need power wiring.

1.5 Functional Block Diagram

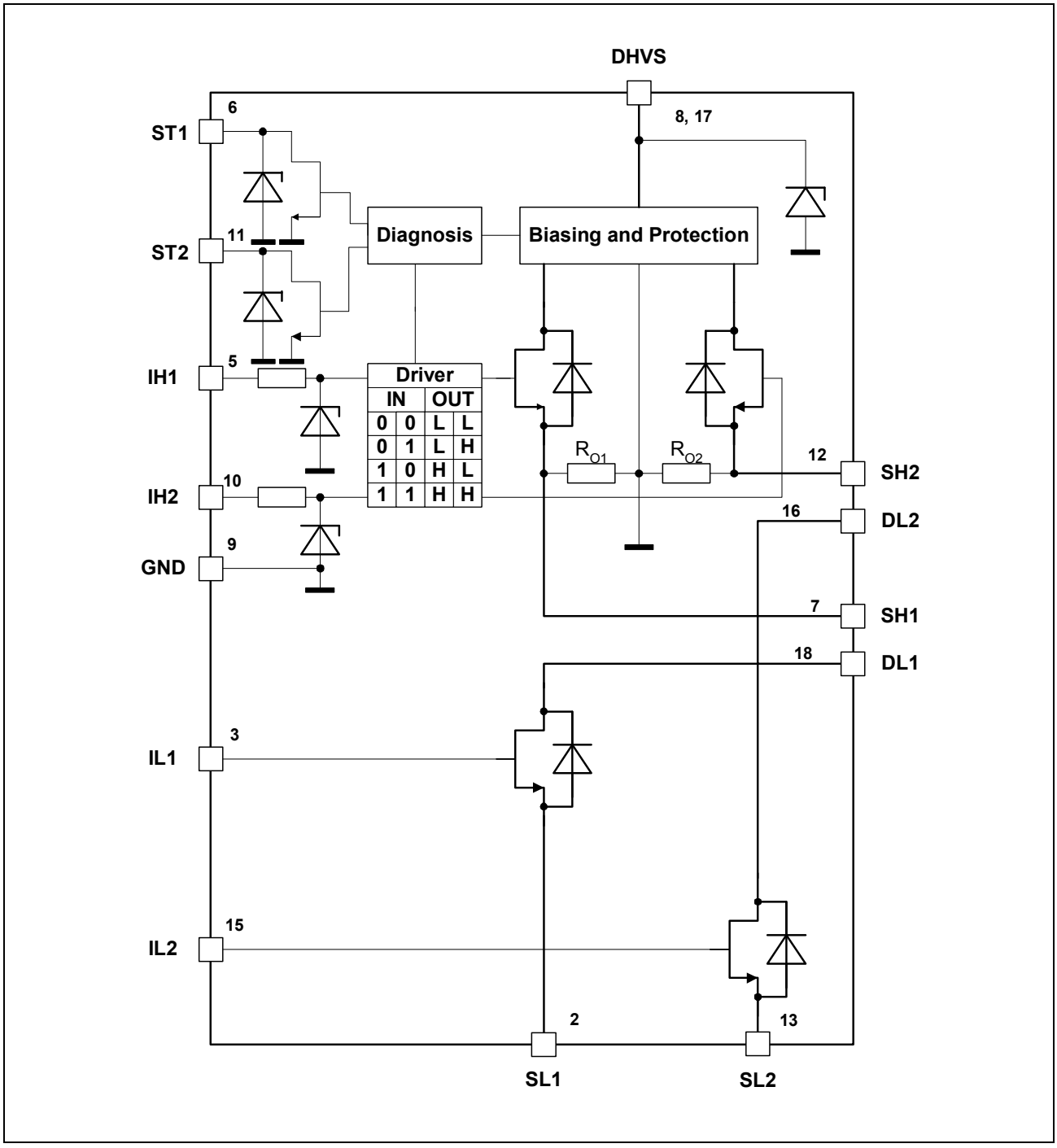


Figure 2
Block Diagram

1.6 Circuit Description

Input Circuit

The control inputs IH1,2 consist of TTL/CMOS compatible Schmitt-Triggers with hysteresis. Buffer amplifiers are driven by these stages and convert the logic signal into the necessary form for driving the power output stages. The inputs are protected by ESD clamp-diodes.

The inputs IL1 and IL2 are connected to the gates of the standard N-channel vertical power-MOS-FETs.

Output Stages

The output stages consist of a low $R_{DS\,ON}$ Power-MOS H-bridge. In H-bridge configuration, the D-MOS body diodes can be used for freewheeling when commutating inductive loads. If the high-side switches are used as single switches, positive and negative voltage spikes which occur when driving inductive loads are limited by integrated power clamp diodes.

Short Circuit Protection

The outputs are protected against

– output short circuit to ground
– overload (load short circuit).

An internal OP-amp controls the Drain-Source-voltage by comparing the DS-voltage-drop with an internal reference voltage. Above this trippoint the OP-Amp reduces the output current depending on the junction temperature and the drop voltage.

In the case of overloaded high-side switches the status output is set to low.

Overtemperature Protection

The high-side switches incorporate an overtemperature protection circuit with hysteresis which switches off the output transistors and sets the status output to low.

Undervoltage-Lockout (UVLO)

When V_S reaches the switch-on voltage V_{UVON} the IC becomes active with a hysteresis. The high-side output transistors are switched off if the supply voltage V_S drops below the switch off value $V_{UVOFF.}$

Open Load Detection

Open load is detected by voltage measurement in off state. If the output voltage exceeds a specified level the error flag is set with a delay.

Status Flag

The two status flag outputs are an open drain output with Zener-diode which require a pull-up resistor, c.f. the application circuit on page 15. ST1 and ST2 provide separate diagnosis for each high-side switch. Various errors as listed in the table “Diagnosis” are detected by switching the open drain output ST1/2 to low. Forward current in the integrated body diode of the highside switch may cause undefined voltage levels at the corresponding status output. The open load detection can be used to detect a short to Vs as long as both lowside switches are off and R_{OL} is disconnected from 5V by BCR192W.

2 Truthtable and Diagnosis (valid only for the High-Side-Switches)

Flag	IH1	IH2	SH1	SH2	ST1	ST2	Remarks
	Inputs		Outputs				
Normal operation; identical with functional truth table	0 0 1 1	0 1 0 1	L L H H	L H L H	1 1 1 1	1 1 1 1	stand-by mode switch2 active switch1 active both switches active
Open load at high-side switch 1 Open load at high-side switch 2	0 1 X X	X X 0 1	Z H X X	X X Z H	0 1 1 1	1 1 0 1	detected detected
Overtemperature high-side switch1	0 1	X X	L L	X X	1 0	1 1	 detected
Overtemperature high-side switch2	X X	0 1	X X	L L	1 1	1 0	 detected
Overtemperature both high-side switches	0 X 1	0 1 X	L L L	L L L	1 1 0	1 0 1	 detected detected
Undervoltage	X	X	L	L	1	1	not detected

*Note: * multiple simultaneous errors are not shown in this table*

Inputs:
0 = Logic LOW
1 = Logic HIGH
X = don’t care

Outputs:
Z = Output in tristate condition
L = Output in sink condition
H = Output in source condition
X = Voltage level undefined

Status:
1 = No error
0 = Error

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

– 40 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
High-Side-Switches (Pins DHVS, IH1,2 and SH1,2)					
Supply voltage	V_S	– 0.3	42	V	–
Supply voltage for full short circuit protection	$V_{S(SCP)}$		28	V	–
HS-drain current	I_S	– 10	*	A	T_C = 125°C; DC
HS-input current	I_{IH}	– 5	5	mA	Pin IH1 and IH2
HS-input voltage	V_{IH}	– 10	16	V	Pin IH1 and IH2
*Note: * internally limited*					
Status Output ST (Pins ST1 and ST2)					
Status pull up voltage	V_{ST}	– 0.3	5.4	V	–
Status Output current	I_{ST}	– 5	5	mA	Pin ST1 or ST2
Low-Side-Switches (Pins DL1,2, IL1,2 and SL1,2)					
Drain- source break down voltage	V_{DSL}	55	–	V	V_{IL} = 0 V; $I_D \leq$ 1 mA
LS-drain current	I_{DL}	–20	20	A	T_C = 125°C; DC
LS-drain current T_C = 85°C	I_{DL}	–	25	A	t_p < 100 ms; ν < 0.1
		–	100	A	t_p < 1 ms; ν < 0.1
LS-input voltage	V_{IL}	– 20	20	V	Pin IL1 and IL2
Temperatures					
Junction temperature	T_j	– 40	150	°C	–
Storage temperature	T_{stg}	– 55	150	°C	–

3.1 Absolute Maximum Ratings (cont'd)

– 40 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Thermal Resistances (one HS-LS-Path active)					
LS-junction case	$R_{thjC\ L}$	–	0.6	K/W	
HS-junction case	$R_{thjC\ H}$	–	0.75	K/W	
Junction ambient $R_{thja} = T_{j(HS)}/(P_{(HS)}+P_{(LS)})$	R_{thja}	–	35	K/W	device soldered to reference PCB with 6 cm^2 cooling area
ESD Protection (Human Body Model acc. MIL STD 883D, method 3015.7 and EOS/ ESD assn. standard S5.1 - 1993)					
Input LS-Switch	V_{ESD}		0.5	kV	
Input HS-Switch	V_{ESD}		1	kV	
Status HS-Switch	V_{ESD}		2	kV	
Output LS and HS-Switch	V_{ESD}		4	kV	all other pins connected to Ground

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

3.2 Operating Range

– 40 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	V_{UVOFF}	42	V	After V_S rising above V_{UVON}
Input voltages HS	V_{IH}	– 0.3	15	V	–
Input voltages LS	V_{IL}	– 0.3	20	V	–
Status output current	I_{ST}	0	2	mA	–
Junction temperature	T_{jHS}	– 40	150	°C	–

Note: In the operating range the functions given in the circuit description are fulfilled.

3.3 Electrical Characteristics

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0$ A; – 40 °C < T_j < 150 °C; 8 V < V_S < 18 V
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current Consumption HS-switch						
Quiescent current	$I_{S\,Q}$	–	4	9	µA	IH1 = IH2 = 0 V T_j = 85 °C
		–	–	20	µA	IH1 = IH2 = 0 V
Supply current	I_S	–	2.5	4.5	mA	IH1 or IH2 = 5 V
		–	5	9	mA	IH1 and IH2 = 5 V
Leakage current of highside switch	$I_{SH\,LK}$	–	–	7	µA	$V_{IH} = V_{SH}$ = 0 V T_j = 85 °C
Leakage current through logic GND in free wheeling condition	$I_{LKCL} = I_{FH} + I_{SH}$	–	2.2	10	mA	I_{FH} =5 A
Current Consumption LS-switch						
Input current	I_{IL}	–	10	100	nA	V_{IL} = 20 V V_{DSL} = 0 V
Leakage current of lowside switch	$I_{DL\,LK}$	–	–	12	µA	V_{IL} = 0 V V_{DSL} = 40 V T_j = 85 °C
Under Voltage Lockout (UVLO) HS-switch						
Switch-ON voltage	V_{UVON}	–	–	5	V	V_S increasing
Switch-OFF voltage	V_{UVOFF}	1.8	–	4.5	V	V_S decreasing
Switch ON/OFF hysteresis	V_{UVHY}	–	1	–	V	$V_{UVON} - V_{UVOFF}$

3.3 Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0$ A; – 40 °C < T_j < 150 °C; 8 V < V_S < 18 V
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output stages						
Inverse diode of high-side switch; Forward-voltage	V_{FH}	–	0.8	1.2	V	I_{FH} = 5 A
Inverse diode of lowside switch; Forward-voltage	V_{FL}	–	0.8	1.2	V	I_{FL} = 5 A
Static drain-source on-resistance of highside switch	$R_{DS\ ON\ H}$	–	26	35	mΩ	I_{SH} = 5 A T_j = 25 °C
Static drain-source on-resistance of lowside switch	$R_{DS\ ON\ L}$	–	14	17	mΩ	I_{SL} = 5 A; V_{IL} = 5 V T_j = 25 °C
Static path on-resistance	$R_{DS\ ON}$	–	–	100	mΩ	$R_{DS\ ON\ H} + R_{DS\ ON\ L}$ I_{SH} = 5 A;
Short Circuit of highside switch to GND						
Initial peak SC current	$I_{SCP\ H}$	35	48	65	A	T_j = – 40 °C
Initial peak SC current	$I_{SCP\ H}$	30	42	54	A	T_j = + 25 °C
Initial peak SC current	$I_{SCP\ H}$	25	32	42	A	T_j = + 150 °C
Note: Peak SC current is significantly lower at V_S > 18V						
Short Circuit of highside switch to V_s						
Output pull-down-resistor	R_O	7	14	42	kΩ	V_{DSL} = 3 V

3.3 Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0$ A; – 40 °C < T_j < 150 °C; 8 V < V_S < 18 V
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Thermal Shutdown						
Thermal shutdown junction temperature	$T_{j\,SD}$	155	180	190	°C	–
Thermal switch-on junction temperature	$T_{j\,SO}$	150	170	180	°C	–
Temperature hysteresis	ΔT	–	10	–	°C	$\Delta T = T_{jSD} - T_{jSO}$
Status Flag Output ST of highside switch						
Low output voltage	$V_{ST\,L}$	–	0.2	0.6	V	I_{ST} = 1.6 mA
Leakage current	$I_{ST\,LK}$	–	–	5	µA	V_{ST} = 5 V
Zener-limit-voltage	$V_{ST\,Z}$	5.4		–	V	I_{ST} = 1.6 mA
Status change after positive input slope with open load	$t_{d(SToffo+)}$	–	–	20	µs	
Status change after negative input slope with open load	$t_{d(SToffo-)}$	–	–	700	µs	
Status change after positive input slope with overtemperature	$t_{d(STofft+)}$	–	1.6	10	µs	R_{ST} = 47 kΩ
Status change after negative input slope with overtemperature	$t_{d(STofft-)}$	–	14	100	µs	R_{ST} = 47 kΩ

Note: times are guaranteed by design

Open load detection in Off condition						
Open load detection voltage	$V_{OUT(OL)}$	2	3	4	V	

3.3 Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0$ A; – 40 °C < T_j < 150 °C; 8 V < V_S < 18 V
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Switching times of highside switch						
Turn-ON-time; to 90% V_{SH}	t_{ON}	–	100	220	µs	R_{Load} = 12 Ω V_S = 12 V
Turn-OFF-time; to 10% V_{SH}	t_{OFF}	–	120	250	µs	R_{Load} = 12 Ω V_S = 12 V
Slew rate on 10 to 30% V_{SH}	dV/dt_{ON}	–	0.5	1.1	V/µs	R_{Load} = 12 Ω V_S = 12 V
Slew rate off 70 to 40% V_{SH}	$-dV/dt_{OFF}$	–	0.7	1.3	V/µs	R_{Load} = 12 Ω V_S = 12 V
Note: switching times are guaranteed by design						
Switching times of low-side switch						
Turn-ON delay time; V_{IL} = 5V; R_{Gate}= 16Ω	$t_{d\_ON\_L}$	–		40	ns	resistive load I_{SL} = 10 A; V_S = 12 V
Switch-ON time; V_{IL}= 5V; R_{Gate} = 16Ω	t_{ON_L}	–		170	ns	resistive load I_{SL} = 10 A; V_S = 12 V
Switch-OFF delay time; V_{IL}= 5V; R_{Gate} = 16Ω	$t_{d\_OFF\_L}$	–		100	ns	resistive load I_{SL} = 10 A; V_S = 12 V
Switch-OFF time; V_{IL}= 5V; R_{Gate} = 16Ω	t_{OFF_L}	–		200	ns	resistive load I_{SL} = 10 A; V_S = 12 V
Input to source charge;	Q_{IS}	–	4.5	6	nC	I_{SL} = 10 A; V_S = 40 V
Input to drain charge;	Q_{ID}	–	16	24	nC	I_{SL} = 10 A; V_S = 40 V
Input charge total;	Q_I	–	55	69	nC	I_{SL} = 10 A; V_S = 40 V V_{IL} = 0 to 10 V
Input plateau voltage;	$V_{(plateau)}$	–	2.6	–	V	I_{SL} = 10 A; V_S = 40 V
Note: switching times and input charges are guaranteed by design						

3.3 Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0$ A; – 40 °C < T_j < 150 °C; 8 V < V_S < 18 V
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Control Inputs of highside switches IH 1, 2						
H-input voltage	$V_{IH\ High}$	–	–	2.5	V	–
L-input voltage	$V_{IH\ Low}$	1	–	–	V	–
Input voltage hysterese	$V_{IH\ HY}$	–	0.5	–	V	–
H-input current	$I_{IH\ High}$	5	30	60	µA	V_{IH} = 5 V
L-input current	$I_{IH\ Low}$	5	14	25	µA	V_{IH} = 0.4 V
Input series resistance	R_I	2.7	4	6	kΩ	–
Zener limit voltage	$V_{IH\ Z}$	5.4	–	–	V	I_{IH} = 1.6 mA
Control Inputs IL1, 2						
Gate-threshold-voltage I_{DL} = 1 mA	$V_{IL\ th}$	–	1.9	2.6	V	T_j = – 40 °C
		–	1.7	–		T_j = + 25 °C
		0.8	1.1	–		T_j = + 150 °C

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and V_S = 12 V.

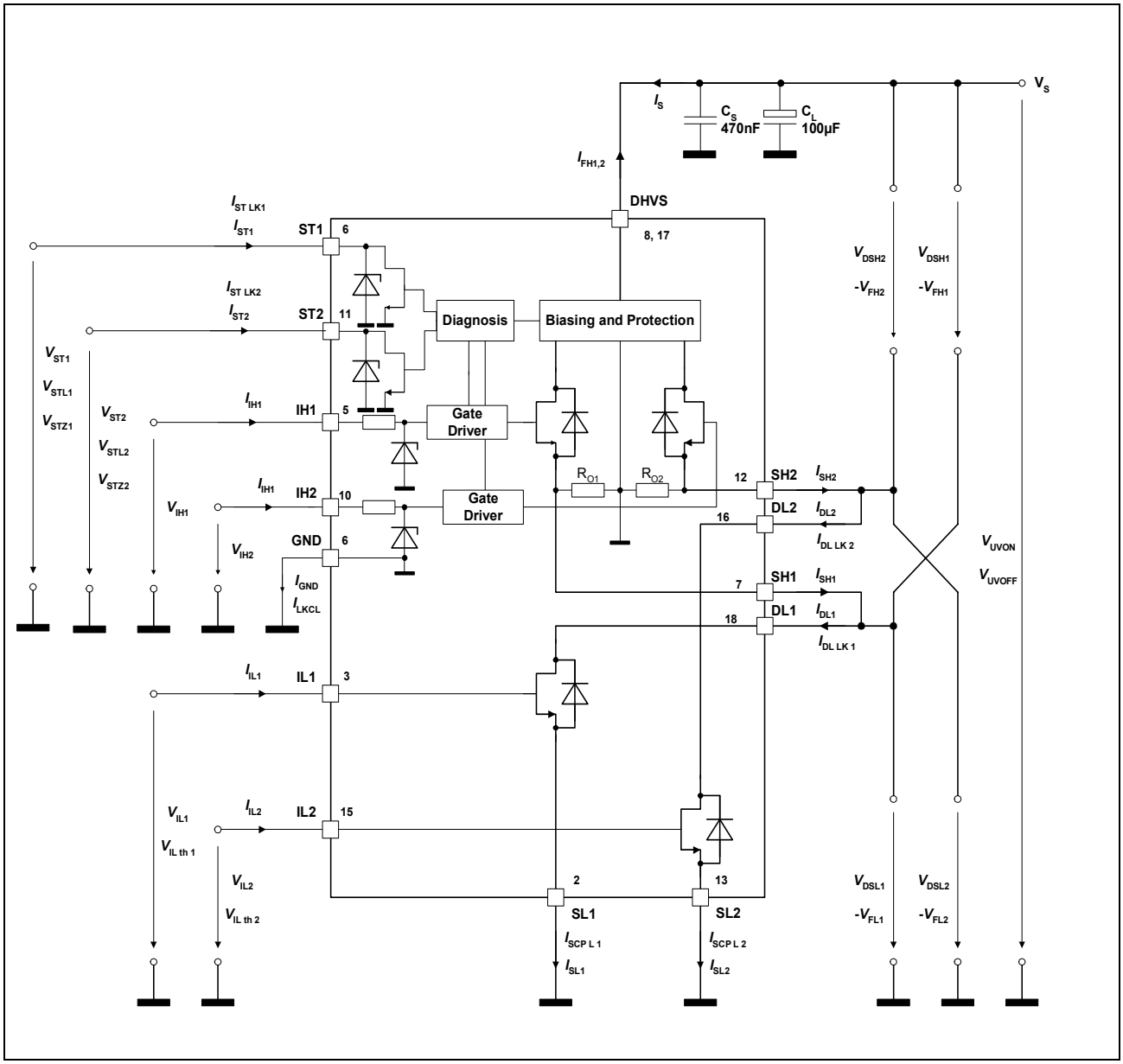


Figure 3
Test Circuit

HS-Source-Current	Named during Short Circuit	Named during Leakage-Cond.
$I_{SH1,2}$	$I_{SCP\ H}$	$I_{DL\ LK}$

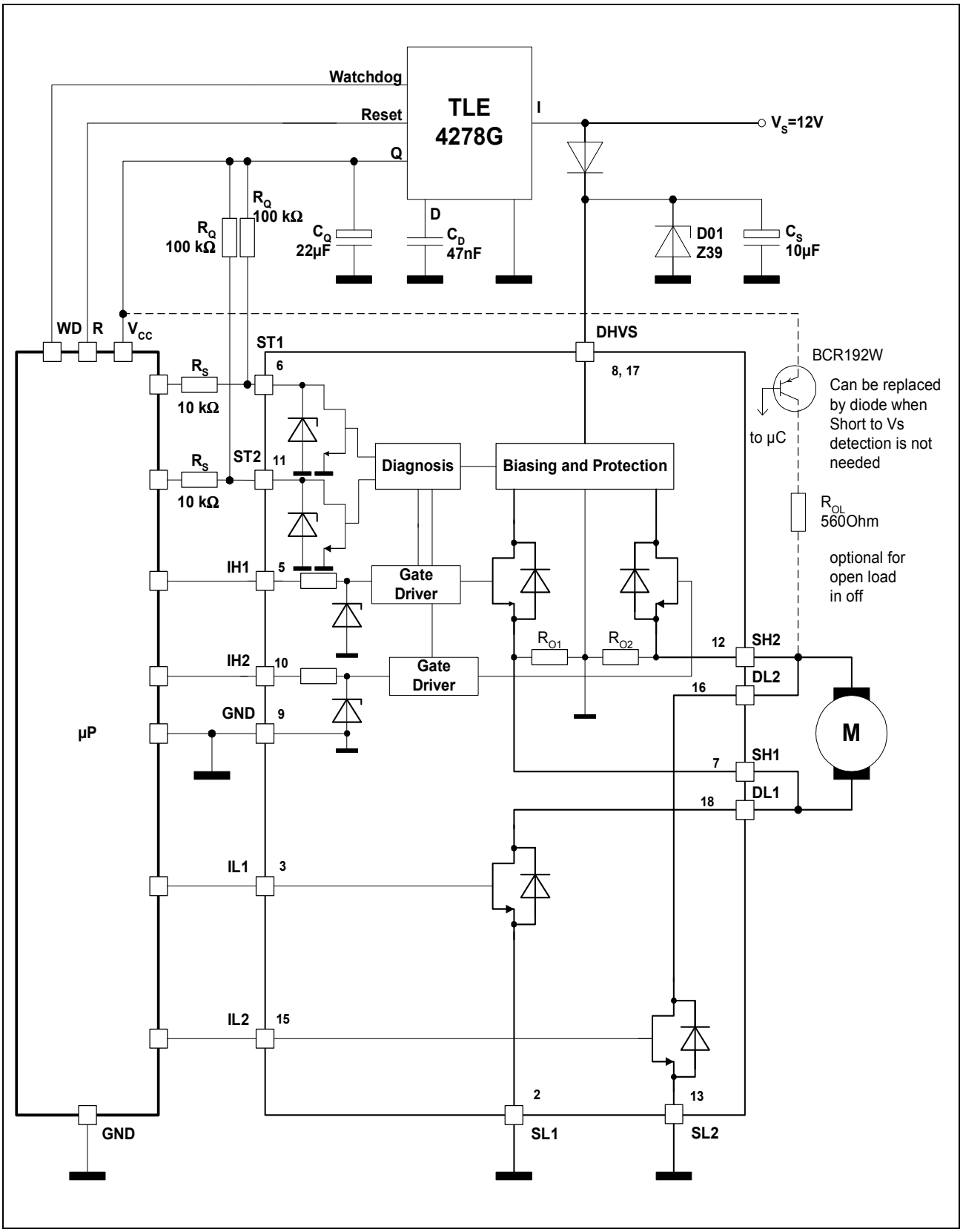
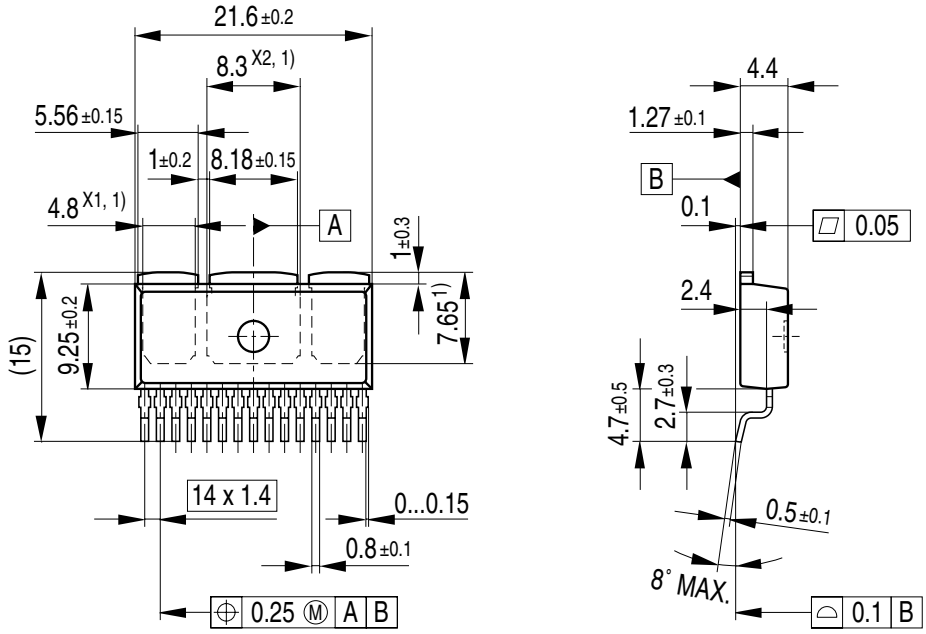


Figure 4
Application Circuit

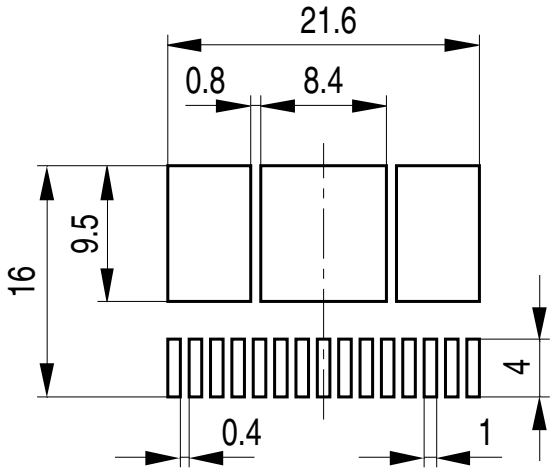
4 Package Outlines

P-TO263-15-1
(Plastic Transistor Single



1) Typical
Metal surface min. X1 = 3.57, X2 = 7.03, Y = 6.9
All metal surfaces tin plated, except area of cut.

Footprint



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

Published by
Infineon Technologies AG,
Bereichs Kommunikation
St.-Martin-Strasse 53,
D-81541 München

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.