

CMOS Dual 'D'-Type Flip-Flop

High-Voltage Types (20-Volt Rating)

■ CD4013B consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and \bar{Q} outputs. These devices can be used for shift register applications, and, by connecting \bar{Q} output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

The CD4013B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

RECOMMENDED OPERATING CONDITIONS

At $T_A = 25^\circ\text{C}$, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | V_{DD} (V) | LIMITS | | UNITS |
|--|--------------|--------|------|---------------|
| | | MIN. | MAX. | |
| Supply-Voltage Range (For $T_A =$ Full Package Temperature Range) | — | 3 | 18 | V |
| Data Setup Time t_S | 5 | 40 | — | ns |
| | 10 | 20 | — | |
| | 15 | 15 | — | |
| Clock Pulse Width t_W | 5 | 140 | — | ns |
| | 10 | 60 | — | |
| | 15 | 40 | — | |
| Clock Input Frequency f_{CL} | 5 | — | 3.5 | MHz |
| | 10 | dc | 8 | |
| | 15 | — | 12 | |
| Clock Rise or Fall Time $t_{r,CL}, t_{f,CL}$ | 5 | — | 500 | μs |
| | 10 | — | 30 | |
| | 15 | — | 6 | |
| Set or Reset Pulse Width t_W | 5 | 180 | — | ns |
| | 10 | 80 | — | |
| | 15 | 50 | — | |

*If more than one unit is cascaded in a parallel clocked operation, $t_{r,CL}$ should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

CD4013B Types

Features:

- Set-Reset capability
- Static flip-flop operation — retains state indefinitely with clock level either "high" or "low"
- Medium-speed operation — 16 MHz (typ.) clock toggle rate at 10V
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of $1\ \mu\text{A}$ at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 1 V at $V_{DD}=5\ \text{V}$
 2 V at $V_{DD}=10\ \text{V}$
 2.5 V at $V_{DD}=15\ \text{V}$
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Registers, counters, control circuits

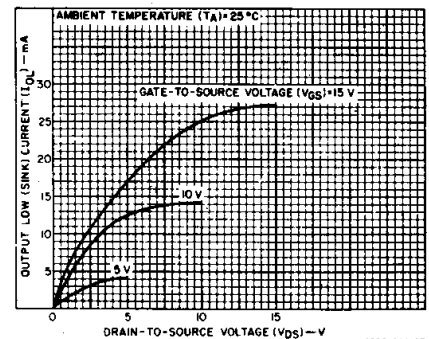
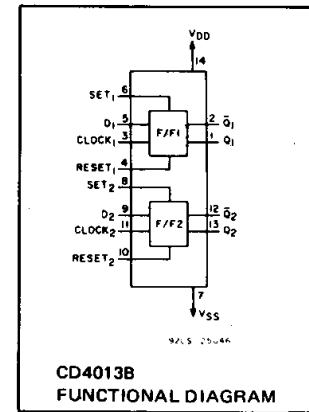


Fig. 1 — Typical output low (sink) current characteristics.

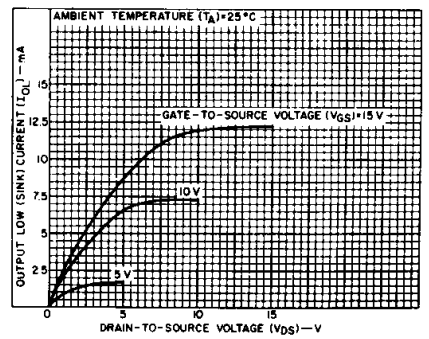


Fig. 2 — Minimum output low (sink) current characteristics.

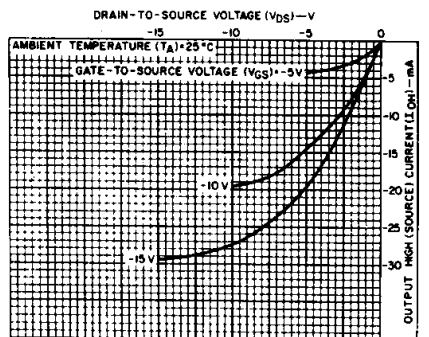


Fig. 3 — Typical output high (source) current characteristics.

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4013B Types

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|--|-----------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | -55 | -40 | +85 | +125 | +25 | | | |
| | | | | | | | | Min. | Typ. | Max. | |
| Quiescent Device Current I _{DD} Max. | — | 0.5 | 5 | 1 | 1 | 30 | 30 | — | 0.02 | 1 | μA |
| | — | 0.10 | 10 | 2 | 2 | 60 | 60 | — | 0.02 | 2 | |
| | — | 0.15 | 15 | 4 | 4 | 120 | 120 | — | 0.02 | 4 | |
| | — | 0.20 | 20 | 20 | 20 | 600 | 600 | — | 0.04 | 20 | |
| Output Low (Sink) Current, I _{OL} Min. | 0.4 | 0.5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | — | mA |
| | 0.5 | 0.10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | — | |
| | 1.5 | 0.15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | — | |
| | 4.6 | 0.5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | — | |
| | 2.5 | 0.5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | — | |
| | 9.5 | 0.10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | — | |
| Output High (Source) Current, I _{OH} Min. | 13.5 | 0.15 | 15 | -4.2 | -4 | -2.8 | -2.4 | -3.4 | -6.8 | — | |
| | — | 0.5 | 5 | — | — | — | — | — | — | — | |
| | — | 0.10 | 10 | — | — | — | — | — | — | — | |
| Output Voltage: Low-Level, V _{OL} Max. | — | 0.5 | 5 | — | — | — | — | — | — | — | V |
| | — | 0.10 | 10 | — | — | — | — | — | — | — | |
| | — | 0.15 | 15 | — | — | — | — | — | — | — | |
| Output Voltage: High-Level, V _{OH} Min. | — | 0.5 | 5 | — | — | — | — | — | — | — | V |
| | — | 0.10 | 10 | — | — | — | — | — | — | — | |
| | — | 0.15 | 15 | — | — | — | — | — | — | — | |
| Input Low Voltage, V _{IL} Max. | 0.5, 4.5 | — | 5 | — | — | — | — | — | — | — | V |
| | 1.9 | — | 10 | — | — | — | — | — | — | — | |
| | 1.5, 13.5 | — | 15 | — | — | — | — | — | — | — | |
| Input High Voltage, V _{IH} Min. | 0.5, 4.5 | — | 5 | — | — | — | — | — | — | — | V |
| | 1.9 | — | 10 | — | — | — | — | — | — | — | |
| | 1.5, 13.5 | — | 15 | — | — | — | — | — | — | — | |
| Input Current, I _{IN} Max. | — | 0.18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | — | ±10 ⁻⁵ | ±0.1 | μA |

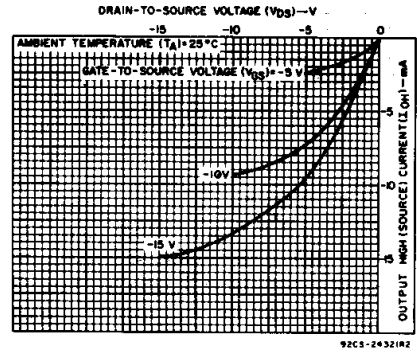


Fig. 4 — Minimum output high (source) current characteristics.

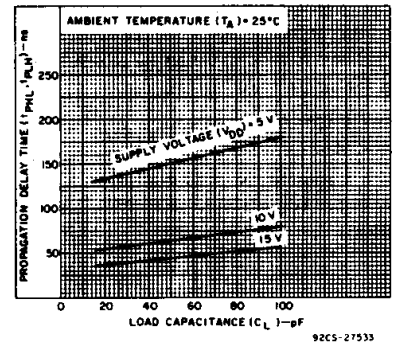


Fig. 5 — Typical propagation delay time vs. load capacitance (CLOCK or SET to Q, CLOCK or RESET to Q).

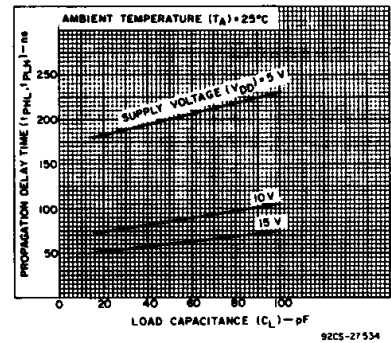


Fig. 6 — Typical propagation delay time vs. load capacitance (SET to Q or RESET to Q).

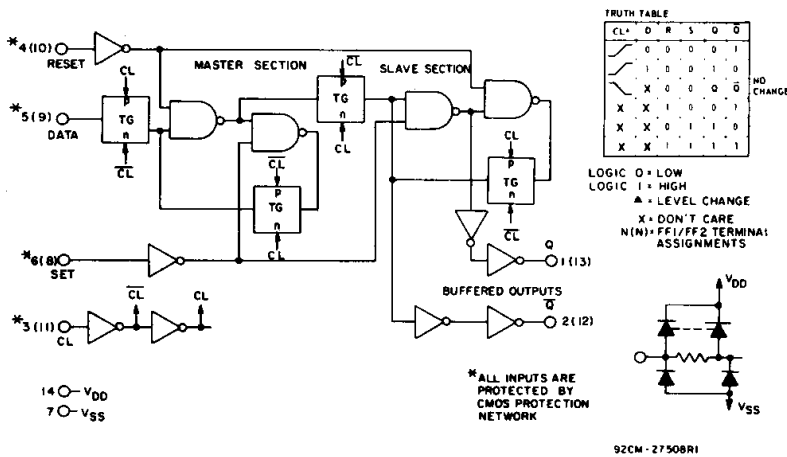


Fig. 7 — Logic diagram and truth table for CD4013B (one of two identical flip-flops).

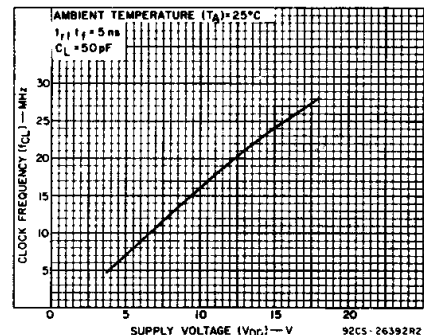


Fig. 8 — Typical maximum clock frequency vs. supply voltage.

CD4013B Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT ±10mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -55°C to +100°C 500mW

For T_A = +100°C to +125°C Derate Linearity at 12mW/°C to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to +125°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max +265°C

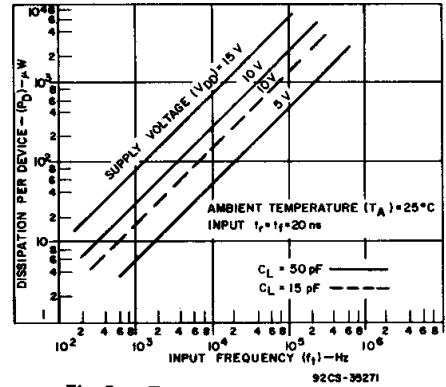


Fig. 9 – Typical power dissipation vs. frequency.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 20 kΩ

| CHARACTERISTIC | TEST CONDITIONS V _{DD} (V) | LIMITS | | | UNITS |
|---|--|----------------|-----------------|-------------------|-------|
| | | MIN. | TYP. | MAX. | |
| Propagation Delay Time: Clock to Q or \bar{Q} Outputs t _{PHL} , t _{PLH} | 5 10 15 | — — — | 150 65 45 | 300 130 90 | ns |
| Set to Q or Reset to \bar{Q} t _{PLH} | 5 10 15 | — — — | 150 65 45 | 300 130 90 | ns |
| Set to \bar{Q} or Reset to Q t _{PHL} | 5 10 15 | — — — | 200 85 60 | 400 170 120 | ns |
| Transition Time t _{THL} , t _{TLH} | 5 10 15 | — — — | 100 50 40 | 200 100 80 | ns |
| Maximum Clock Input Frequency# f _{CL} | 5 10 15 | 3.5 8 12 | 7 16 24 | — — — | MHz |
| Minimum Clock Pulse Width t _w | 5 10 15 | — — — | 70 30 20 | 140 60 40 | ns |
| Minimum Set or Reset Pulse Width t _w | 5 10 15 | — — — | 90 40 25 | 180 80 50 | ns |
| Minimum Data Setup Time t _s | 5 10 15 | — — — | 20 10 7 | 40 20 15 | ns |
| Minimum Data Hold Time t _h | 5 10 15 | — — — | 2 2 2 | 5 5 5 | ns |
| Clock Input Rise or Fall Time t _{rCL} , t _{fCL} | 5 10 15 | — — — | — — — | 500 30 6 | μs |
| Input Capacitance C _{IN} | Any Input | — | 5 | 7.5 | pF |

#Input t_r, t_f = 5 ns.

TEST CIRCUITS

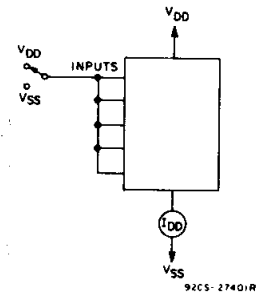


Fig. 10 – Quiescent device current.

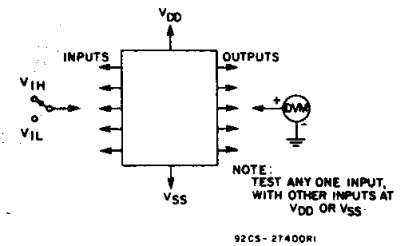


Fig. 11 – Input voltage.

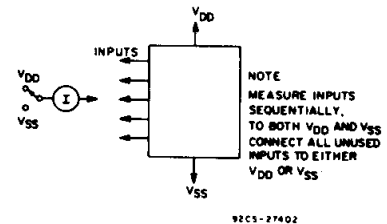


Fig. 12 – Input current.

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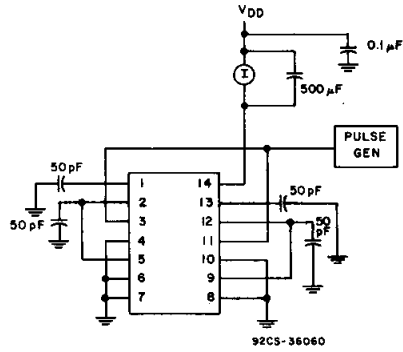
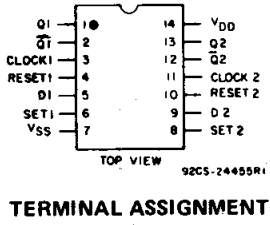
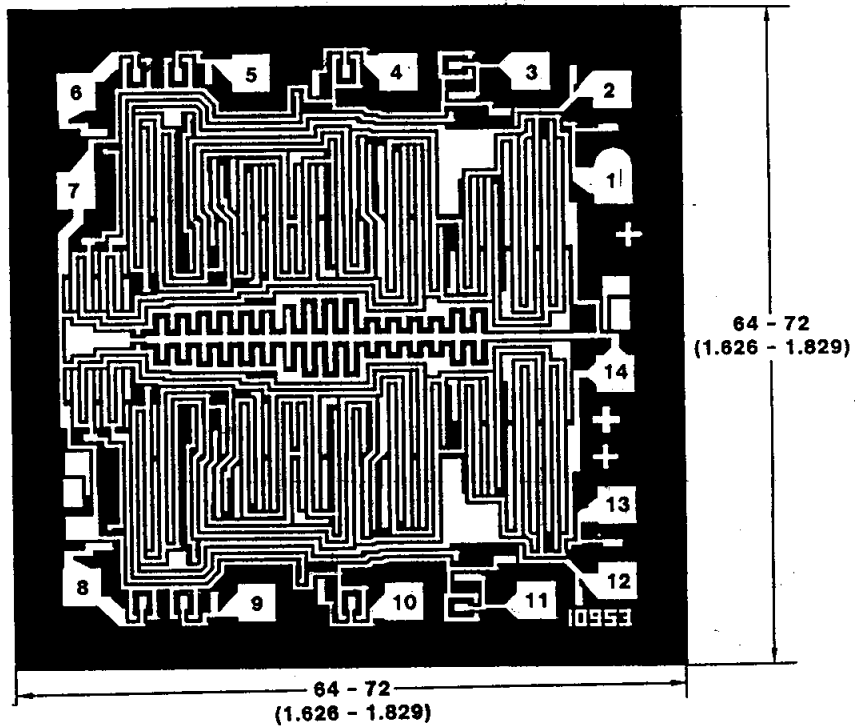


Fig. 13—Dynamic power dissipation test circuit.

DIMENSIONS AND PAD LAYOUT FOR CD4013BH



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



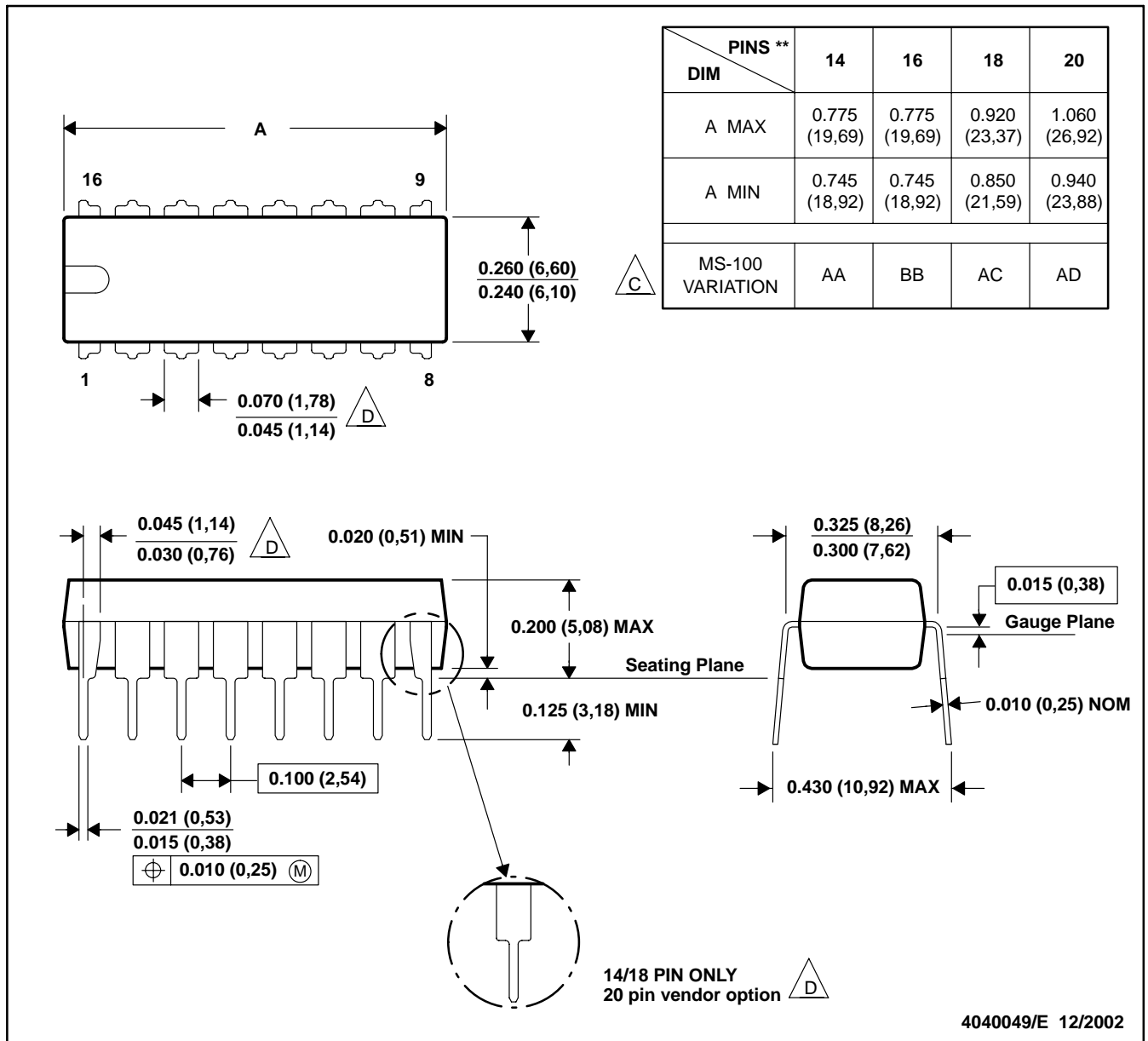
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



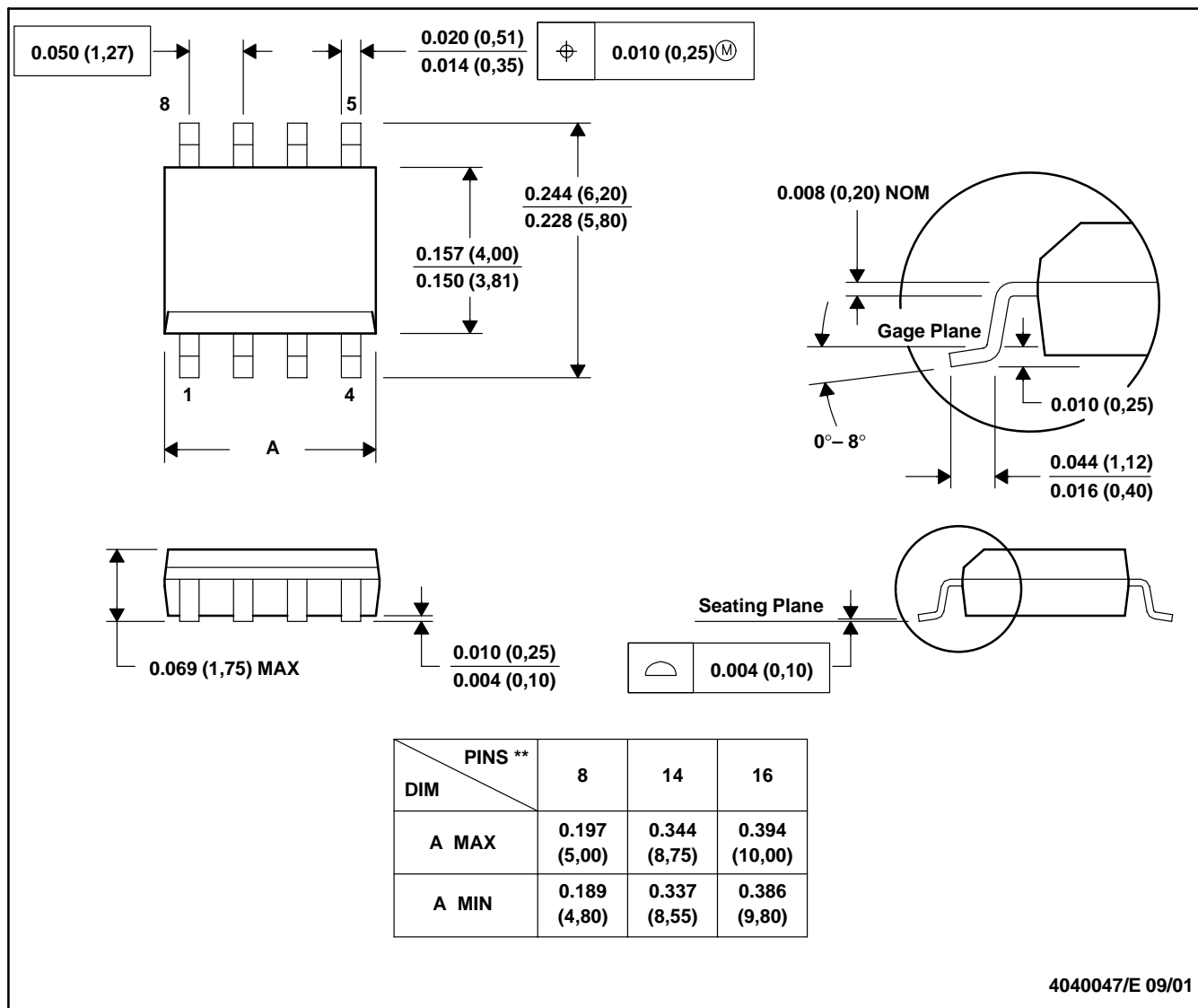
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265