

## 74AC14 • 74ACT14 Hex Inverter with Schmitt Trigger Input

### General Description

The 74AC14 and 74ACT14 contain six inverter gates each with a Schmitt trigger input. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

The 74AC14 and 74ACT14 have hysteresis between the positive-going and negative-going input thresholds (typically 1.0V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

### Features

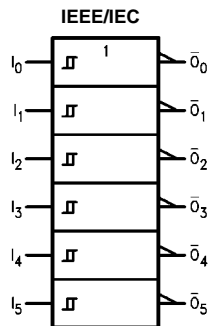
- $I_{CC}$  reduced by 50%
- Outputs source/sink 24 mA
- 74ACT14 has TTL-compatible inputs

### Ordering Code:

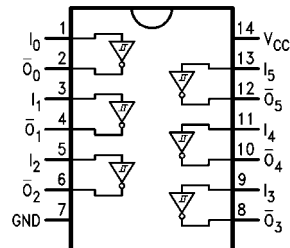
Order Number	Package Number	Package Description
74AC14SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
74AC14SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC14MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MS-153, 4.4mm Wide
74AC14PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT14SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
74ACT14MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MS-153, 4.4mm Wide
74ACT14PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

### Logic Symbol



### Connection Diagram



### Pin Descriptions

Pin Names	Description
$I_n$	Inputs
$\bar{O}_n$	Outputs

### Function Table

Input	Output
A	$\bar{O}$
L	H
H	L

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**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	±50 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature ( $T_J$ )	
PDIP	140°C

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
PDIP	-40°C to +85°C

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

**DC Electrical Characteristics for AC**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits				
$V_{OH}$	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu\text{A}$	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		V		3.0		2.56	2.46	$I_{OH} = 12$ $I_{OH} = 24 \text{ mA}$ $I_{OH} = 24 \text{ mA (Note 2)}$
				4.5		3.86	3.76	
				5.5		4.86	4.76	
$V_{OL}$	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		V		3.0		0.36	0.44	$I_{OL} = 12$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA (Note 2)}$
				4.5		0.36	0.44	
				5.5		0.36	0.44	
$I_{IN}$ (Note 4)	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}, \text{GND}$	
$V_{th}$	Maximum Positive Threshold	3.0		2.2	2.2	V	$T_A = \text{Worst Case}$	
		4.5		3.2	3.2			
		5.5		3.9	3.9			
$V_{tl}$	Minimum Negative Threshold	3.0		0.5	0.5	V	$T_A = \text{Worst Case}$	
		4.5		0.9	0.9			
		5.5		1.1	1.1			
$V_{H(MAX)}$	Maximum Hysteresis	3.0		1.2	1.2	V	$T_A = \text{Worst Case}$	
		4.5		1.4	1.4			
		5.5		1.6	1.6			
$V_{H(MIN)}$	Minimum Hysteresis	3.0		0.3	0.3	V	$T_A = \text{Worst Case}$	
		4.5		0.4	0.4			
		5.5		0.5	0.5			
$I_{OLD}$	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V \text{ Max}$	
$I_{OHD}$	Output Current (Note 3)	5.5			-75	mA	$V_{OHD} = 3.85V \text{ Min}$	
$I_{CC}$ (Note 4)	Maximum Quiescent Supply Current	5.5		2.0	20.0	μA	$V_{IN} = V_{CC}$ or GND	

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

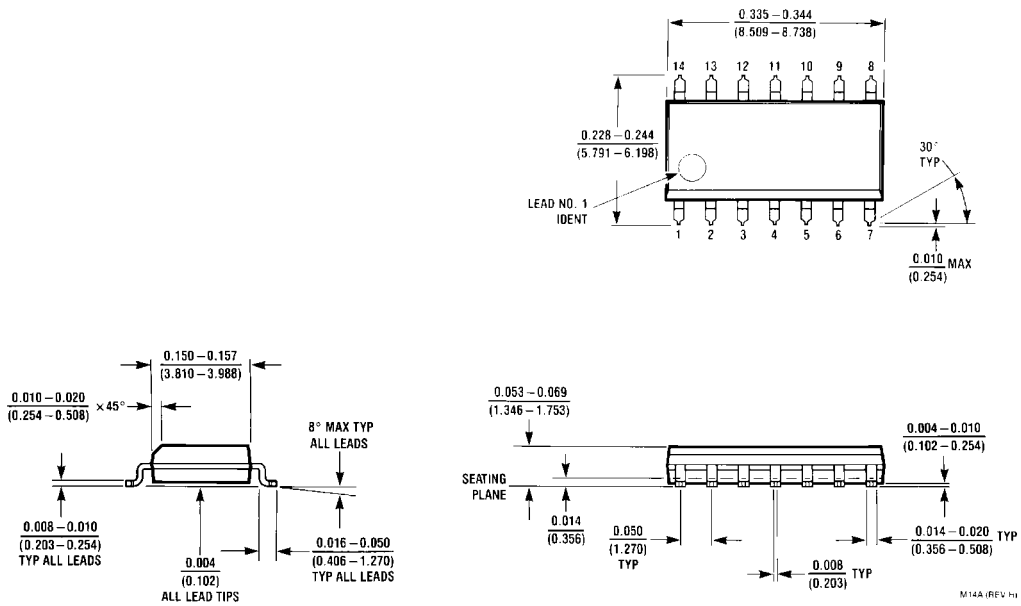
**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 4:**  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .

AC Electrical Characteristics for AC								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 5)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	3.3	1.5	9.5	13.5	1.5	15.0	ns
		5.0	1.5	7.0	10.0	1.5	11.0	
t <sub>PHL</sub>	Propagation Delay	3.3	1.5	7.5	11.5	1.5	13.0	ns
		5.0	1.5	6.0	8.5	1.5	9.5	
<b>Note 5:</b> Voltage Range 3.3 is 3.3V ± 0.3V Voltage Range 5.0 is 5.0V ± 0.5V								
DC Electrical Characteristics for ACT								
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C	Units	Conditions	
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	
		5.5	1.5	2.0	2.0			
V <sub>IL</sub>	Maximum LOW Level Output Voltage	4.5	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	
		5.5	1.5	0.8	0.8			
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	4.5	4.49	4.34	4.4	V	I <sub>OUT</sub> = -50μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -24 mA (Note 6)	
		5.5		4.86	4.76			
V <sub>OL</sub>	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44			V
5.5		0.36	0.44					
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V <sub>i</sub> = V <sub>CC</sub> , GND	
V <sub>H(MAX)</sub>	Maximum Hysteresis	4.5		1.4	1.4	V	T <sub>A</sub> = Worst Case	
		5.5		1.6	1.6			
V <sub>H(MIN)</sub>	Minimum Hysteresis	4.5		0.4	0.4	V	T <sub>A</sub> = Worst Case	
		5.5		0.5	0.5			
V <sub>t+</sub>	Maximum Positive Threshold	4.5		2.0	2.0	V	T <sub>A</sub> = Worst Case	
		5.5		2.0	2.0			
V <sub>t-</sub>	Minimum Negative Threshold	4.5		0.8	0.8	V	T <sub>A</sub> = Worst Case	
		5.5		0.8	0.8			
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	0.6		1.5	mA	V <sub>i</sub> = V <sub>CC</sub> - 2.1V	
I <sub>OLD</sub>	Minimum Dynamic	5.5			75	mA	V <sub>OLD</sub> = 1.65V Max	
I <sub>OHD</sub>	Output Current (Note 7)	5.5			-75	mA	V <sub>OHD</sub> = 3.85V Min	
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		2.0	20.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	
<b>Note 6:</b> All outputs loaded; thresholds on input associated with output under test. <b>Note 7:</b> Maximum test duration 2.0 ms, one output loaded at a time.								

AC Electrical Characteristics for ACT								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 8)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay Data to Output	5.0	3.0	8.0	10.0	3.0	11.0	ns
t <sub>PHL</sub>	Propagation Delay Data to Output	5.0	3.0	8.0	10.0	3.0	11.0	ns
<b>Note 8:</b> Voltage Range 5.0 is 5.0V ± 0.5V								
Capacitance								
Symbol	Parameter	Typ	Units	Conditions				
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN				
C <sub>PD</sub>	Power Dissipation Capacitance for AC for ACT	25.0 80	pF	V <sub>CC</sub> = 5.0V				

**Physical Dimensions** inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body  
Package Number M14A**

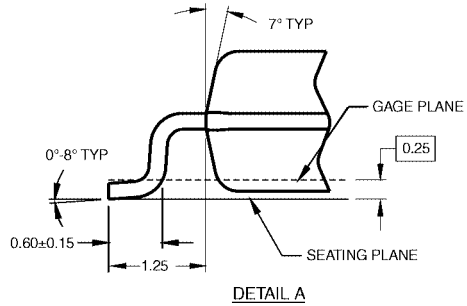
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

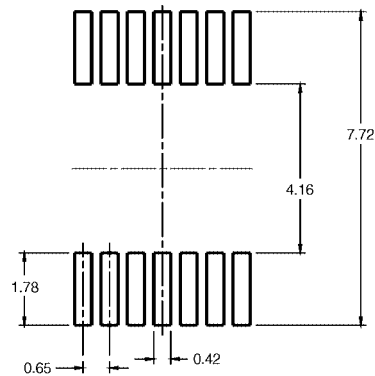
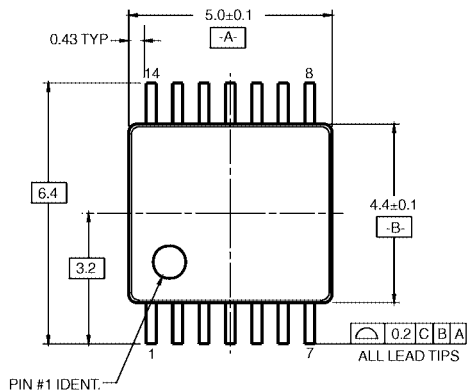
- NOTES:  
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.  
 B. DIMENSIONS ARE IN MILLIMETERS.  
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

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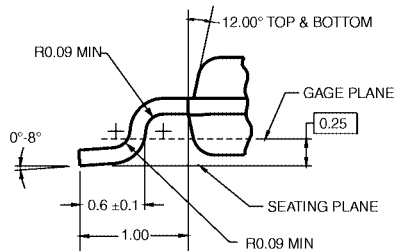
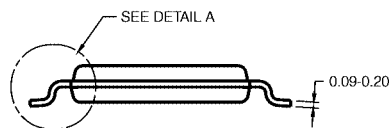
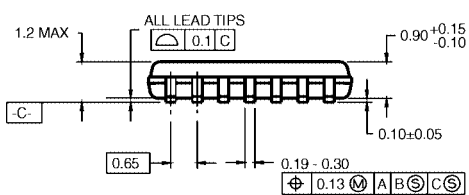


**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
 Package Number M14D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DETAIL A

- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
  - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC14RevC3

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A**

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