FAIRCHILD SEMICONDUCTOR™

July 1993
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74VHC123A
Dual Retriggerable Monostable Multivibrator

General Description

The VHC123A is an advanced high speed CMOS Monostable Multivibrator fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one-shot. The VHC123A can be triggered on the positive transition of the clear while A is held low and B is held high. The output pulse width is determined by the equation: $PW = (R_x)(C_x)$; where PW is in seconds, R is in ohms, and C is in farads.

Limits for R_x and C_x are:

External capacitor, C_x No limit

External resistors, R_x V_{CC} = 2.0V, 5 kΩ min

V_{CC} > 3.0V, 1 kΩ min

An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

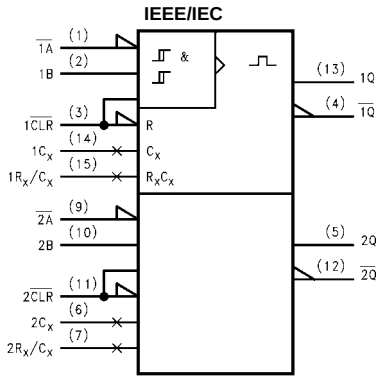
- High Speed:
  t_{PD} = 8.1 ns (typ) at T_A = 25°C
- Low Power Dissipation:
  I_{CC} = 4 μA (Max) at T_A = 25°C
- Active State: I_{CC} = 600 μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Power down protection is provided on all inputs
- Pin and function compatible with 74HC123A

Ordering Code:

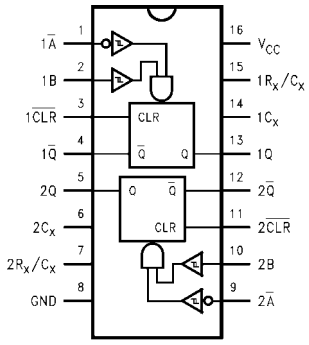
Order Number	Package Number	Package Description
74VHC123AM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow
74VHC123ASJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC123AMTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC123AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{A}$	Trigger Inputs (Negative Edge)
B	Trigger Inputs (Positive Edge)
$\overline{CLR}$	Reset Inputs
C_x	External Capacitor
R_x	External Resistor
Q, $\overline{Q}$	Outputs

Truth Table

Inputs			Outputs		Function
$\overline{A}$	B	$\overline{CLR}$	Q	$\overline{Q}$	
↓	H	H	⎍	⎍	Output Enable
X	L	H	L	H	Inhibit
H	X	H	L	H	Inhibit
L	↑	H	⎍	⎍	Output Enable
L	H	↑	⎍	⎍	Output Enable
X	X	L	L	H	Reset

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↓ = HIGH-to-LOW Transition
↑ = LOW-to-HIGH Transition

Block Diagrams

Note A: C_x, R_x, D_x are external Capacitor, Resistor, and Diode, respectively.

Note B: External clamping diode, D_x;

External capacitor is charged to V_{CC} level in the wait state, i.e. when no trigger is applied.

If the supply voltage is turned off, C_x discharges mainly through the internal (parasitic) diode. If C_x is sufficiently large and V_{CC} drops rapidly, there will be some possibility of damaging the IC through in rush current or latch-up. If the capacitance of the supply voltage filter is large enough and V_{CC} drops slowly, the in rush current is automatically limited and damage to the IC is avoided.

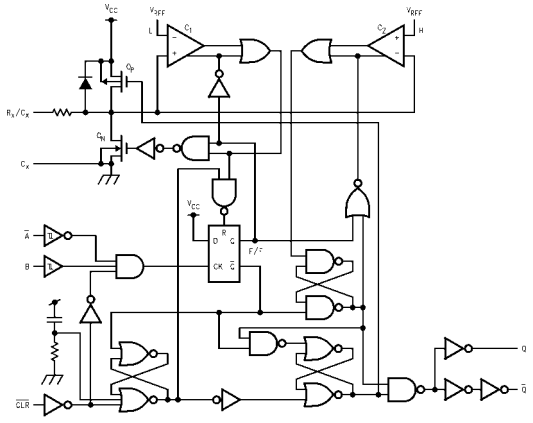
The maximum value of forward current through the parasitic diode is ±20 mA. In the case of a large Cx, the limit of fall time of the supply voltage is determined as follows:

$t_f \geq (V_{CC} - 0.7)\ C_x/20\ mA$

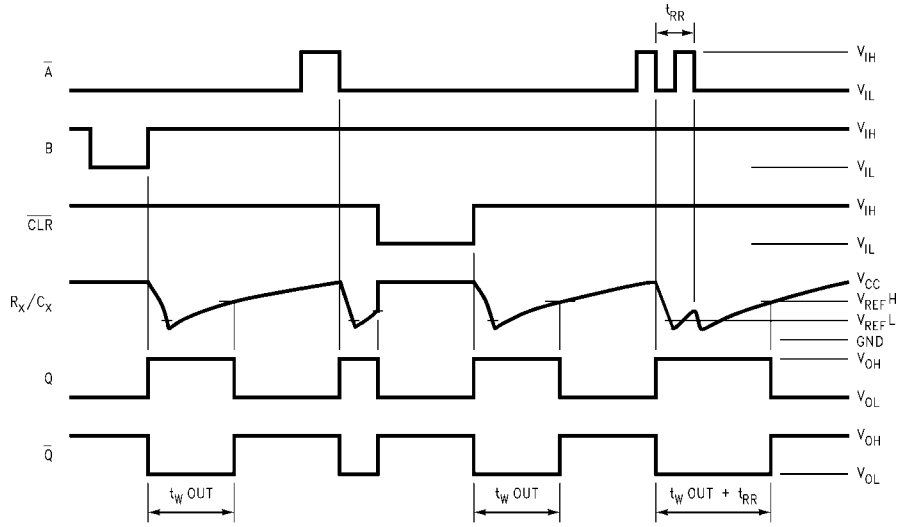
(t_f is the time between the supply voltage turn off and the supply voltage reaching 0.4 V_{CC})

In the event a system does not satisfy the above condition, an external clamping diode (D_x) is needed to protect the IC from rush current.

System Diagram



Timing Chart



Functional Description

1. Stand-by State

   The external capacitor (C_x) is fully charged to V_{CC} in the Stand-by State. That means, before triggering, the Q_P and Q_N transistors which are connected to the R_x/C_x node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies turn off. The total supply current is only leakage current.

2. Trigger Operation

   Trigger operation is effective in any of the following three cases. First, the condition where the $\overline{A}$ input is LOW, and B input has a rising signal; second, where the B input is HIGH, and the A input has a falling signal; and third, where the $\overline{A}$ input is LOW and the B input is HIGH, and the $\overline{CLR}$ input has a rising signal.

   After a trigger becomes effective, comparators C_1 and C_2 start operating, and Q_N is turned on. The external capacitor discharges through Q_N. The voltage level at the R_x/C_x node drops. If the R_x/C_x voltage level falls to the internal reference voltage $V_{ref}L$, the output of C_1 becomes LOW. The flip-flop is then reset and Q_N turns off. At that moment C_1 stops but C_2 continues operating.

   After Q_N turns off, the voltage at the R_x/C_x node starts rising at a rate determined by the time constant of external capacitor C_x and resistor R_x.

   Upon triggering, output Q becomes HIGH, following some delay time of the internal F/F and gates. It stays HIGH even if the voltage of R_x/C_x changes from falling to rising. When R_x/C_x reaches the internal reference voltage $V_{ref}H$, the output of C_2 becomes LOW, the output Q goes LOW and C_2 stops its operation. That means, after triggering, when the voltage level of the R_x/C_x node reaches $V_{ref}H$, the IC returns to its MONOSTABLE state.

   With large values of C_x and R_x, and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse, t_W (OUT), is as follows:

   t_W (OUT) = 1.0 C_x R_x

3. Retrigger operation (74VHC123A)

   When a new trigger is applied to either input $\overline{A}$ or B while in the MONOSTABLE state, it is effective only if the IC is charging C_x. The voltage level of the R_x/C_x node then falls to $V_{ref}L$ level again. Therefore the Q output stays HIGH if the next trigger comes in before the time period set by C_x and R_x.

   If the new trigger is very close to a previous trigger, such as an occurrence during the discharge cycle, it will have no effect.

   The minimum time for a trigger to be effective 2nd trigger, t_{RR} (Min), depends on V_{CC} and C_x.

4. Reset Operation

   In normal operation, the $\overline{CLR}$ input is held HIGH. If $\overline{CLR}$ is LOW, a trigger has no affect because the Q output is held LOW and the trigger control F/F is reset. Also, Q_p turns on and C_x is charged rapidly to V_{CC}.

   This means if $\overline{CLR}$ is set LOW, the IC goes into a wait state.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/Current (I_{CC})	±50 mA
Storage Temperature (T_{STG})	−65°C to 150°C
Lead Temperature (T_L)	
Soldering, 10 seconds	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature	
(T_{opr})	−40° to +85°C
Input Rise and Fall Time (t_r, t_f)	
($\overline{CLR}$ only)	
V_{CC} = 3.3V ± 0.3V	0 ~ 100 ns/V
V_{CC} = 5.0V ± 0.5V	0 ~ 20 ns/V
External Capacitor - C_x	No Limitation (Note 3) F
External Resistor - R_x	>5 kΩ (Note 3) (V_{CC} = 2.0V)
	>1 kΩ (Note 3) (V_{CC} > 3.0V)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommended operation outside data book specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

Note 3: The maximum allowable values of C_x and R_x are a function of the leakage of capacitor C_x, the leakage of the device, and leakage due to board layout and surface resistance. Susceptibility to externally induced noise signals may occur for R_x> 1 MΩ.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C			T_A = −40° to 85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level	2.0	1.50			1.50		V		
	Input Voltage	3.0 – 5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level	2.0			0.50		0.50	V		
	Input Voltage	3.0 – 5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	HIGH Level	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 µA
	Output Voltage	3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		I_{OH} = −4 mA
		4.5	3.94			3.80				I_{OH} = −8 mA
V_{OL}	LOW Level	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 µA
	Output Voltage	3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44			I_{OL} = 4 mA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0 – 5.5			±0.1		±1.0	µA	V_{IN} = 5.5V or GND	
I_{IN}	R_x/C_x Terminal	5.5			±0.25		±2.50	µA	V_{IN} = V_{CC} or GND	
	Off-State Current									
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	µA	V_{IN} = V_{CC} or GND	
I_{CC}	Active—State	3.0		160	250		280		V_{IN} = V_{CC} or GND	
	(Note 4)	4.5		380	500		650	µA	R_x/C_x = 0.5 V_{CC}	
	Supply Current	5.5		560	750		975			

Note 4: Per Circuit

AC Electrical Characteristics (Note 5)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions
			Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Time (A, B–Q, $\overline{Q}$)	3.3 ± 0.3		13.4	20.6	1.0	24.0	ns	C_L = 15 pF
				15.9	24.1	1.0	27.5		C_L = 50 pF
		5.0 ± 0.5		8.1	12.0	1.0	14.0	ns	C_L = 15 pF
				9.6	14.0	1.0	16.0		C_L = 50 pF
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$ Trigger—Q, $\overline{Q}$ \)	3.3 ± 0.3		14.5	22.4	1.0	26.0	ns	C_L = 15 pF
				17.0	25.9	1.0	29.5		C_L = 50 pF
		5.0 ± 0.5		8.7	12.9	1.0	15.0	ns	C_L = 15 pF
				10.2	14.9	1.0	17.0		C_L = 50 pF
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$—Q, $\overline{Q}$)	3.3 ± 0.3		10.3	15.8	1.0	18.5	ns	C_L = 15 pF
				12.8	19.3	1.0	22.0		C_L = 50 pF
		5.0 ± 0.5		6.3	9.4	1.0	11.0	ns	C_L = 15 pF
				7.8	11.4	1.0	13.0		C_L = 50 pF
t_{WOUT}	Output Pulse Width	3.3 ± 0.3		160	240		300	ns	C_L = 50 pF C_x = 28 pF
		5.0 ± 0.5		133	200		240		R_x = 2 kΩ
		3.3 ± 0.3	90	100	110	90	110	µs	C_L = 50 pF C_x = 0.01 µF
		5.0 ± 0.5	90	100	110	90	110		R_x = 10 kΩ
		3.3 ± 0.3	0.9	1.0	1.1	0.9	1.1	ms	C_L = 50 pF C_x = 0.1 µF
		5.0 ± 0.5	0.9	1.0	1.1	0.9	1.1		R_x = 10 kΩ
Δt_{WOUT}	Output Pulse Width Error Between Circuits (In same Package)			±1				%	
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open
C_{PD}	Power Dissipation Capacitance			73				pF	(Note 6)

Note 5: Refer to Timing Chart.

Note 6: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

I_{CC} (opr.) = C_{PD}*V_{CC}*f_{IN+} I_{CC}^{1}*Duty/100 + I_{CC}/2 (per Circuit)

I_{CC}^{1}: Active Supply Current

Duty:%

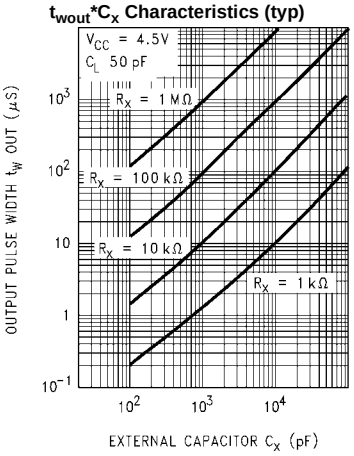
AC Operating Requirement (Note 7)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions
			Min	Typ	Max	Min	Max		
t_W(L)	Minimum Trigger	3.3		5.0			5.0	ns	
t_W(H)	Pulse Width	5.0		5.0			5.0		
t_W(L)	Minimum Clear	3.3		5.0			5.0	ns	
	Pulse Width	5.0		5.0			5.0		
t_{RR}	Minimum	3.3 ± 0.3		60				ns	R_x = 1 kΩ
	Retrigger Time	5.0 ± 0.5		39					C_X = 100 pF
		3.3		1.5				µs	R_x = 1 kΩ
		5.0		1.2					C_X = 0.01 µF

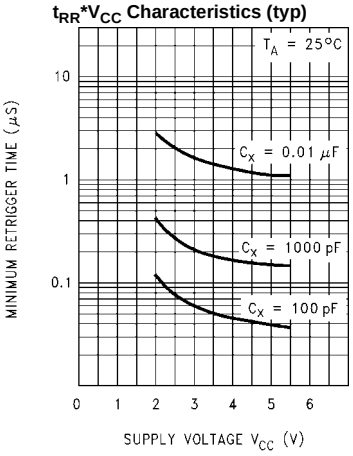
Note 7: Refer to Timing Chart.

Device Characteristics

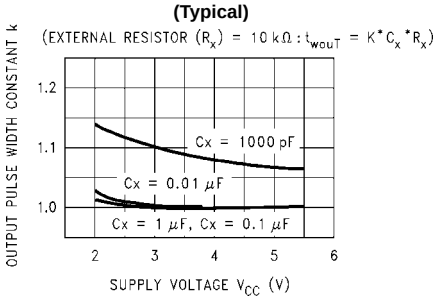
t_{wout}*C_x Characteristics (typ)



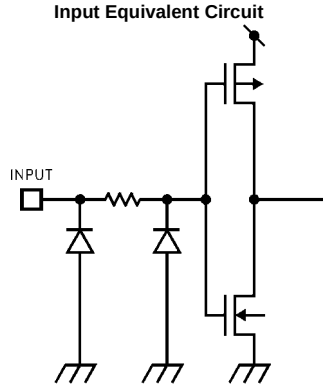
t_{RR}*V_{CC} Characteristics (typ)



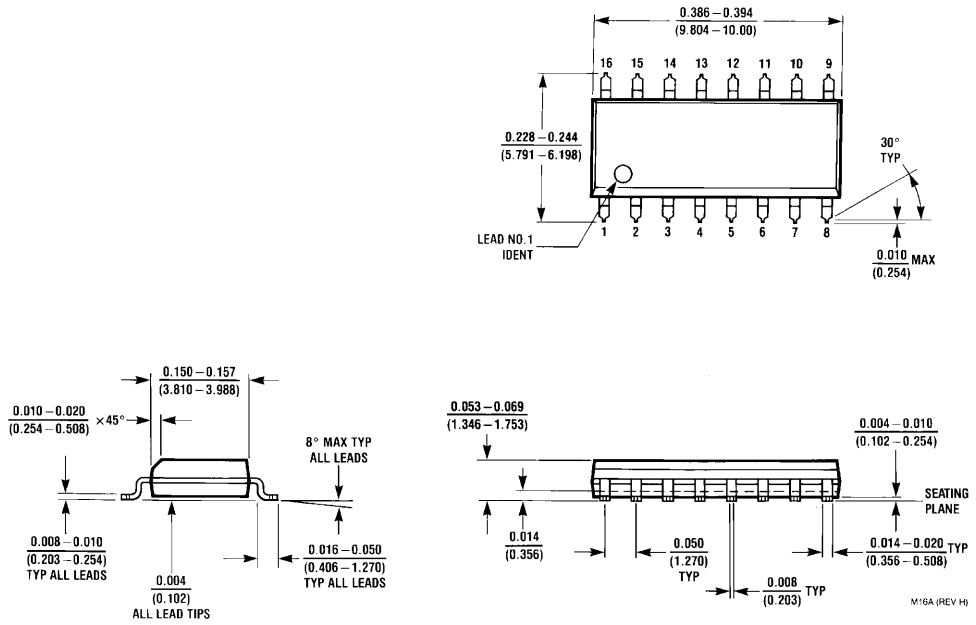
Output Pulse Width Constant K-Supply Voltage (Typical)



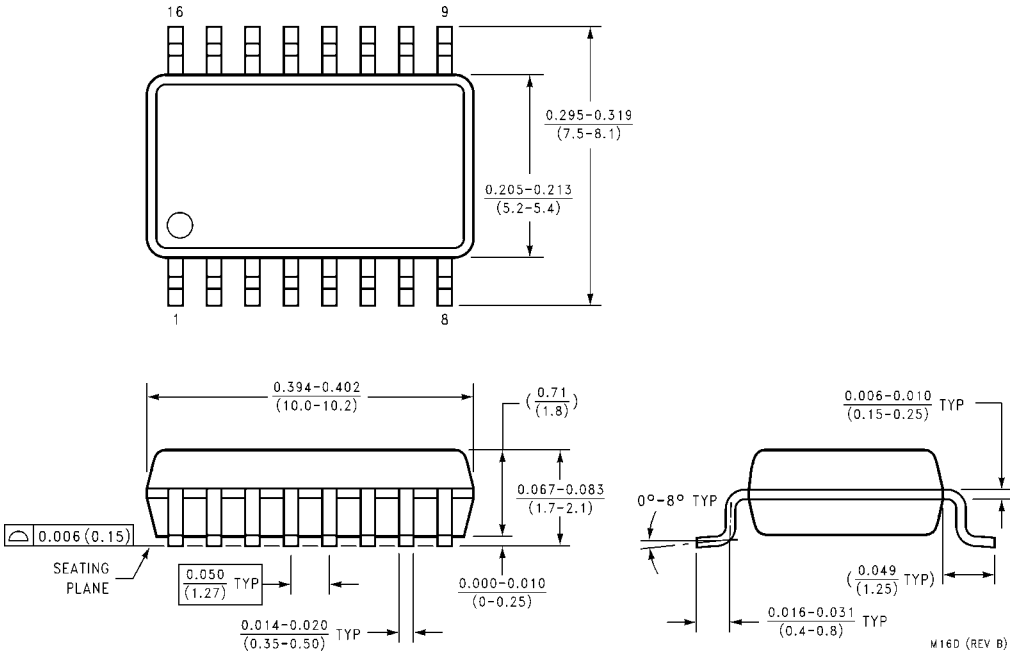
Input Equivalent Circuit



Physical Dimensions inches (millimeters) unless otherwise noted

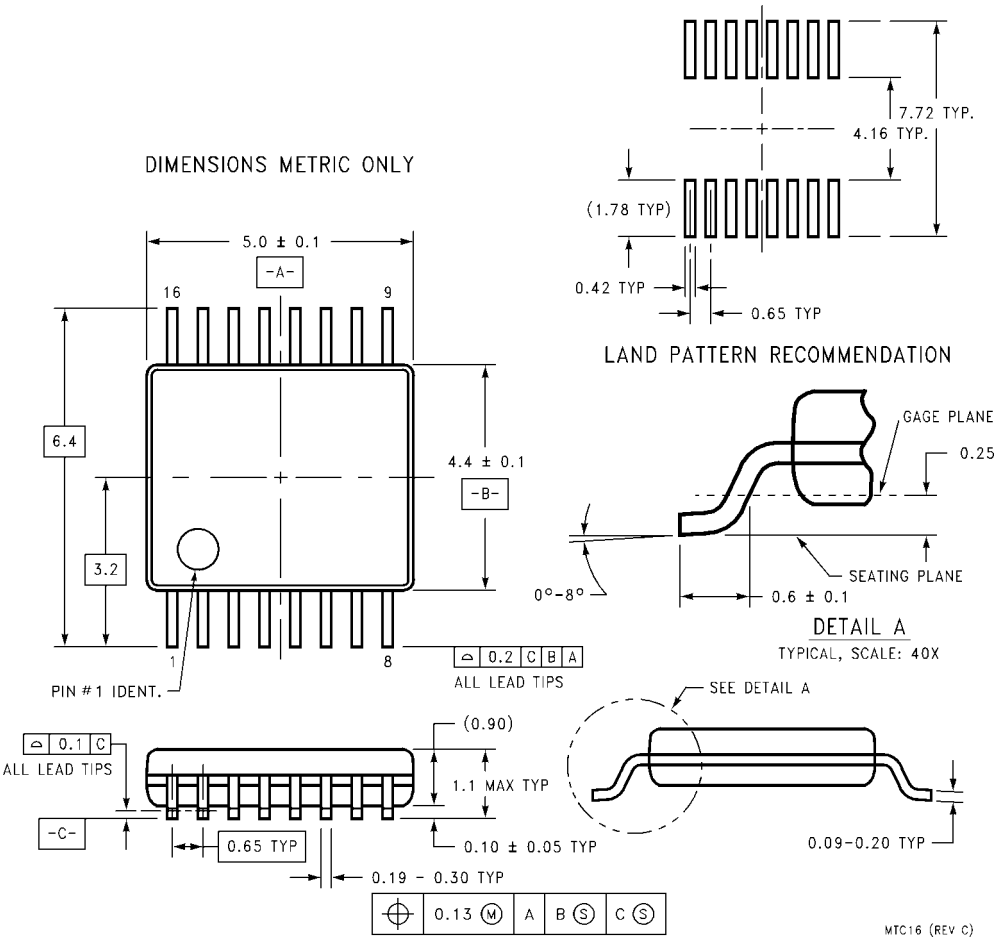


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A



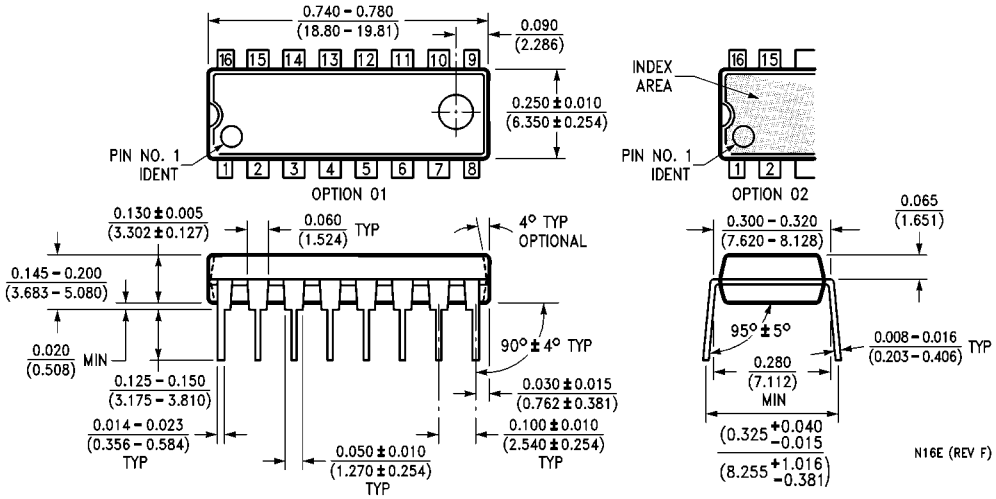
16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E