DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

FEATURES

- **Wide analog input voltage range: ± 5 V.**
- **Low "ON" resistance:**
  80 Ω (typ.) at $V_{CC} - V_{EE}$ = 4.5 V
  70 Ω (typ.) at $V_{CC} - V_{EE}$ = 6.0 V
  60 Ω (typ.) at $V_{CC} - V_{EE}$ = 9.0 V
- **Logic level translation:**
  to enable 5 V logic to communicate with ± 5 V analog signals
- **Typical "break before make" built in**
- **Output capability: non-standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT4052 are high-speed Si-gate CMOS devices and are pin compatible with the "4052" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4052 are dual 4-channel analog multiplexers/demultiplexers with common select logic. Each multiplexer has four independent inputs/outputs (nY_0 to nY_3) and a common input/output (nZ). The common channel select logics include two digital select inputs (S_0 and S_1) and an active LOW enable input ($\overline{E}$).

With $\overline{E}$ LOW, one of the four switches is selected (low impedance ON-state) by S_0 and S_1. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S_0 and S_1.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_0 and S_1, and $\overline{E}$). The V_{CC} to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY_0 to nY_3, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}$ or S_n to V_{OS}	C_L = 15 pF, R_L = 1 kΩ, V_{CC} = 5 V	28	18	ns
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}$ or S_n to V_{OS}		21	13	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	57	57	pF
C_S	max. switch capacitance independent (Y)		5	5	pF
	common (Z)		12	12	pF

V_{EE} = GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:

   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs
   C_L = output load capacitance in pF
   C_S = max. switch capacitance in pF
   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 5, 2, 4	$2Y_0$ to $2Y_3$	independent inputs/outputs
6	$\overline{E}$	enable input (active LOW)
7	V_{EE}	negative supply voltage
8	GND	ground (0 V)
10, 9	S_0, S_1	select inputs
12, 14, 15, 11	$1Y_0$ to $1Y_3$	independent inputs/outputs
13, 3	1Z, 2Z	common inputs/outputs
16	V_{CC}	positive supply voltage

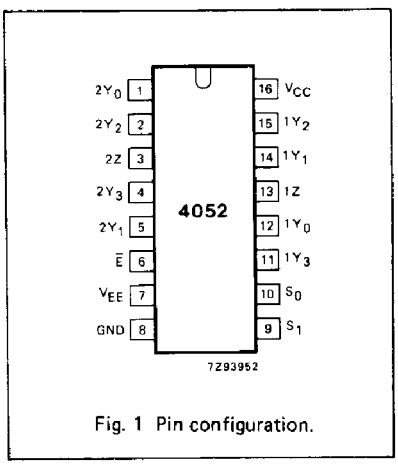


Fig. 1 Pin configuration.

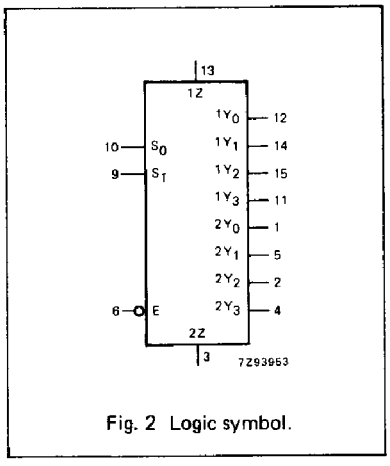


Fig. 2 Logic symbol.

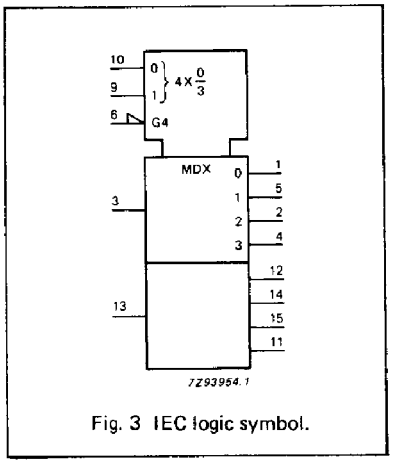


Fig. 3 IEC logic symbol.

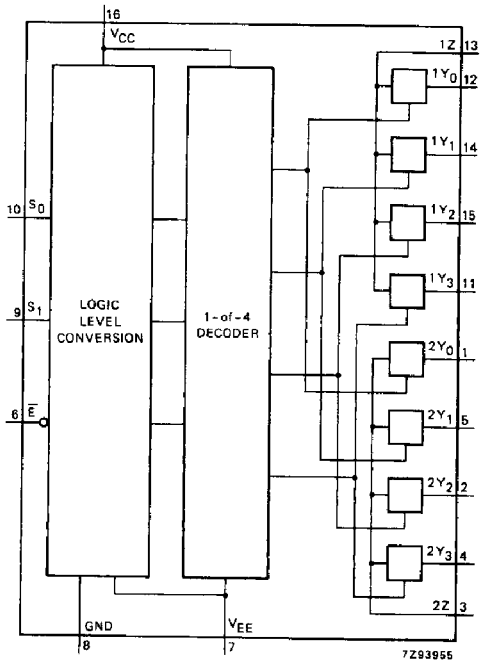


Fig. 4 Functional diagram.

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

FUNCTION TABLE

INPUTS			CHANNEL ON
$\overline{E}$	S_1	S_0	
L	L	L	$nY_0 - nZ$
L	L	H	$nY_1 - nZ$
L	H	L	$nY_2 - nZ$
L	H	H	$nY_3 - nZ$
H	X	X	none

H = HIGH voltage level
L = LOW voltage level
X = don't care

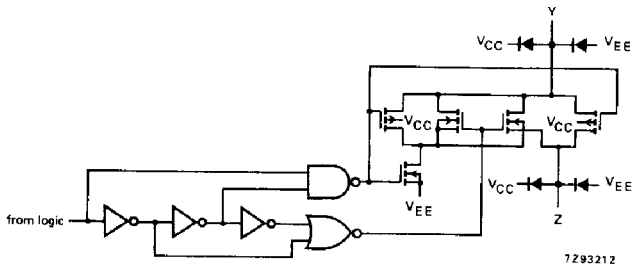


Fig. 5 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to V_{EE} = GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V
$\pm I_S$	DC switch current		25	mA	for -0.5 V $< V_S < V_{CC} + 0.5$ V
$\pm I_{EE}$	DC V_{EE} current		20	mA	
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K
P_S	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminals nZ, when switch current flows in terminals nY_n, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals nZ, no V_{CC} current will flow out of terminals nY_n. In this case there is no limit for the voltage drop across the switch, but the voltages at nY_n and nZ may not exceed V_{CC} or V_{EE}.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage V_{CC}–GND	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
V_{CC}	DC supply voltage V_{CC}–V_{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V V_{CC} = 10.0 V

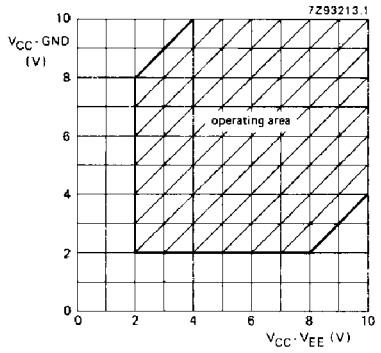


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4052.

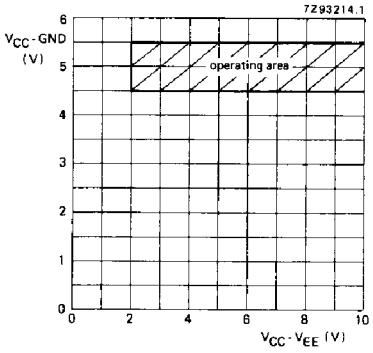


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4052.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: V_{CC} – GND or V_{CC} – V_{EE} =2.0, 4.5, 6.0 and 9.0 V
For 74HCT: V_{CC} – GND =4.5 and 5.5 V; V_{CC} – V_{EE} =2.0, 4.5, 6.0 and 9.0 V

SYMBOL	PARAMETER	T_{amb} (°C) 74HC/HCT +25 min.	+25 typ.	+25 max.	–40 to +85 min.	–40 to +85 max.	–40 to +125 min.	–40 to +125 max.	UNIT	TEST CONDITIONS V_{CC} V	V_{EE} V	I_S μA	V_{is}	V_I
R_{ON}	ON resistance (peak)		–	–		–		–	Ω	2.0	0	100	V_{CC} to V_{EE}	V_{IN} or V_{IL}
			100	180		225		270	Ω	4.5	0	1000		
			90	160		200		240	Ω	6.0	0	1000		
			70	130		165		195	Ω	4.5	–4.5	1000		
R_{ON}	ON resistance (rail)		150	–		–		–	Ω	2.0	0	100	V_{EE}	V_{IH} or V_{IL}
			80	140		175		210	Ω	4.5	0	1000		
			70	120		150		180	Ω	6.0	0	1000		
			60	105		130		160	Ω	4.5	–4.5	1000		
R_{ON}	ON resistance (rail)		150	–		–		–	Ω	2.0	0	100	V_{CC}	V_{IH} or V_{IL}
			90	160		200		240	Ω	4.5	0	1000		
			80	140		175		210	Ω	6.0	0	1000		
			65	120		150		180	Ω	4.5	–4.5	1000		
ΔR_{ON}	maximum Δ ON resistance between any two channels		–						Ω	2.0	0		V_{CC} to V_{EE}	V_{IH} or V_{IL}
			9						Ω	4.5	0			
			8						Ω	6.0	0			
			6						Ω	4.5	–4.5			

Notes to DC characteristics

1. At supply voltages (V_{CC} – V_{EE}) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. There it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
2. For test circuit measuring R_{ON} see Fig. 8.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HC											
		+25			−40 to +85		−40 to +125			V_{CC} V	V_{EE} V	V_I	OTHER
		min.	typ.	max.	min.	max.	min.	max.					
V_{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0			
V_{IL}	LOW level input voltage		0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0			
$\pm I_I$	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	0 0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch OFF-state current all channels			0.2		2.0		2.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch ON-state current			0.2		2.0		2.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 11)
I_{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	6.0 10.0	0 0	V_{CC} or GND	$V_{is} = V_{EE}$ or V_{CC}; $V_{os} = V_{CC}$ or V_{EE}

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC										
		+25			−40 to +85		−40 to +125			V_{CC} V	V_{EE} V	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}		14 5 4 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = \infty$; C_L = 50 pF (see Fig. 18)
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}$ to V_{os} S_n to V_{os}		105 38 30 26	325 65 55 46		405 81 69 58		490 98 83 69	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = \infty$; C_L = 50 pF (see Figs 19, 20 and 21)
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}$ to V_{os} S_n to V_{os}		74 27 22 22	250 50 43 38		315 63 54 48		375 75 64 57	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HCT											
		+25			−40 to +85		−40 to +125			V_{CC} V	V_{EE} V	V_I	OTHER
		min.	typ.	max.	min.	max.	min.	max.					
V_{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5			
V_{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5			
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch OFF-state current all channels			0.2		2.0		2.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 10)
$\pm I_S$	analog switch ON-state current			0.2		2.0		2.0	μA	10.0	0	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - V_{EE}$ (see Fig. 11)
I_{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	5.5 5.0	0 −5.0	V_{CC} or GND	$V_{is} = V_{EE}$ or V_{CC}; $V_{os} = V_{CC}$ or V_{EE}
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	0	V_{CC} − 2.1 V	other inputs at V_{CC} or GND

Note to HCT types

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
   To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
S_n	0.45
$\overline{E}$	0.45

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_{EE} V	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}		5 4	12 8		15 10		18 12	ns	4.5 4.5	0 −4.5	$R_L = \infty$; C_L = 50 pF (see Fig. 18)
t_{PZH}/ t_{PZL}	turn "ON" time $\overline{E}$ to V_{os} S_n to V_{os}		41 28	70 48		88 60		105 72	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)
t_{PHZ}/ t_{PLZ}	turn "OFF" time $\overline{E}$ to V_{os} S_n to V_{os}		26 21	50 38		63 48		75 57	ns	4.5 4.5	0 −4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 19, 20 and 21)

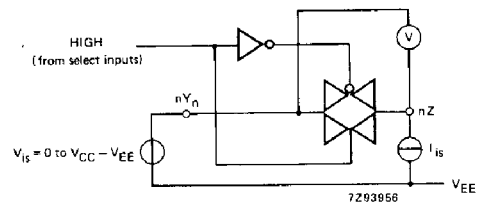


Fig. 8 Test circuit for measuring R_{ON}.

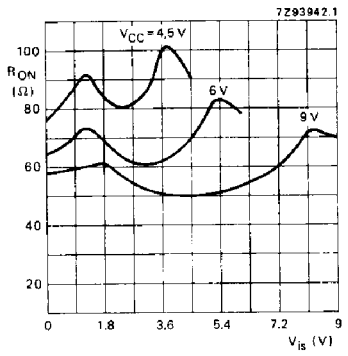


Fig. 9 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to $V_{CC} - V_{EE}$.

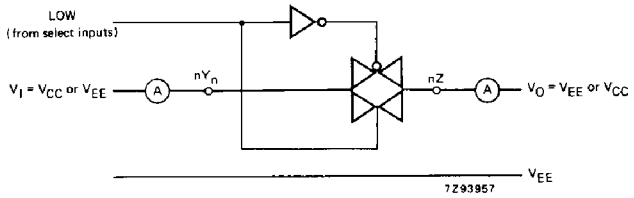


Fig. 10 Test circuit for measuring OFF-state current.

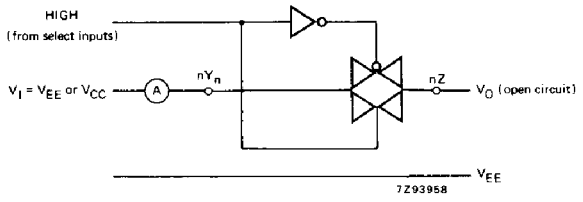


Fig. 11 Test circuit for measuring ON-state current.

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	typ.	UNIT	V_{CC} V	V_{EE} V	$V_{is(p-p)}$ V	CONDITIONS
	sine-wave distortion f = 1 kHz	0.04 0.02	% %	2.25 4.5	−2.25 −4.5	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 14)
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	2.25 4.5	−2.25 −4.5	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig. 14)
	switch "OFF" signal feed-through	−50 −50	dB dB	2.25 4.5	−2.25 −4.5	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (see Figs 12 and 15)
	crosstalk between any two switches/ multiplexers	−60 −60	dB dB	2.25 4.5	−2.25 −4.5	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (see Fig. 16)
$V_{(p-p)}$	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 −4.5		R_L = 600 Ω; C_L = 50 pF; f = 1 MHz ($\overline{E}$ or S_n, square-wave between V_{CC} and GND, t_r = t_f = 6 ns) (see Fig. 17)
f_{max}	minimum frequency response (−3dB)	170 180	MHz MHz	2.25 4.5	−2.25 −4.5	note 2	R_L = 50 Ω; C_L = 50 pF (see Figs 13 and 14)
C_S	maximum switch capacitance independent (Y) common (Z)	 5 12	 pF pF				

Notes to AC characteristics

General note

V_{is} is the input voltage at an nY_n or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at an nY_n or nZ terminal, whichever is assigned as an output.

Notes

1. Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

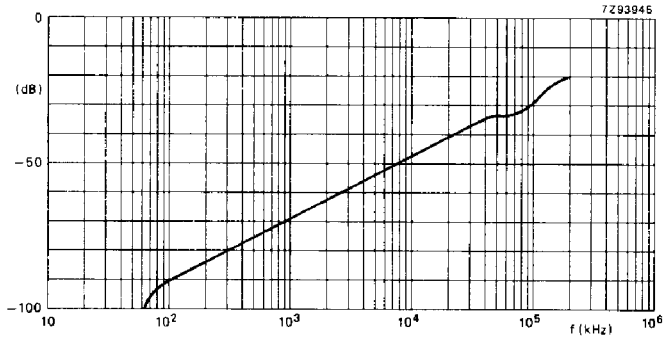
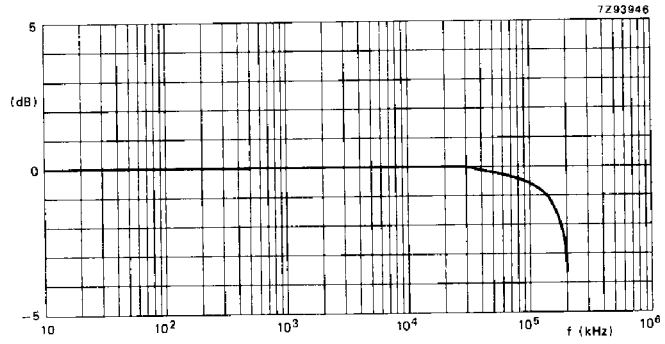


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.



Note to Figs 12 and 13

Test conditions:
V_{CC} = 4.5 V; GND = 0 V; V_{EE} = −4.5 V;
R_L = 50 Ω; R_{source} = 1 kΩ.

Fig. 13 Typical frequency response.

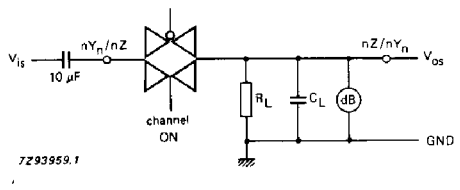


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

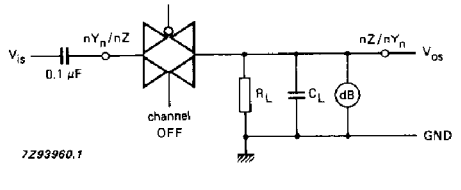


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

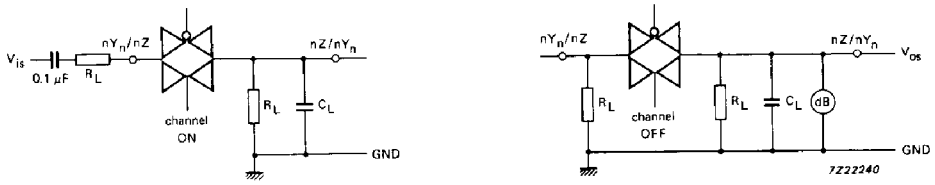


Fig. 16 Test circuits for measuring crosstalk between any two switches/multiplexers.
(a) channel ON condition; (b) channel OFF condition.

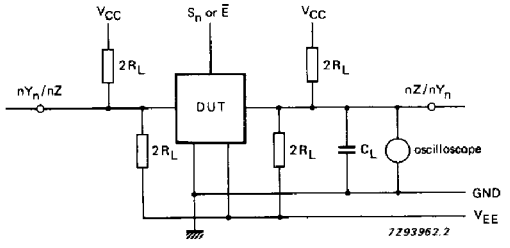
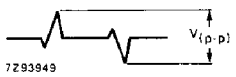


Fig. 17 Test circuit for measuring crosstalk between control and any switch.

Note to Fig. 17

The crosstalk is defined as follows (oscilloscope output):



AC WAVEFORMS

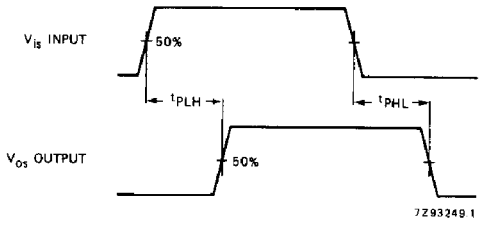


Fig. 18 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

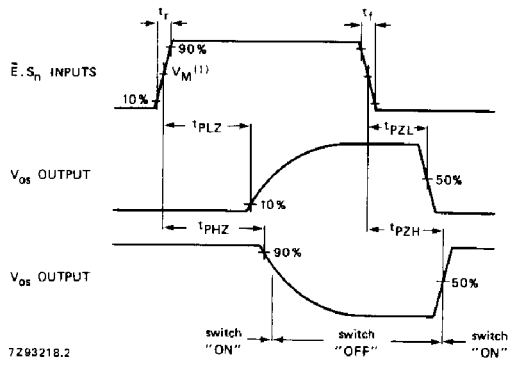


Fig. 19 Waveforms showing the turn-ON and turn-OFF times.

Note to Fig. 19

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

TEST CIRCUIT AND WAVEFORMS

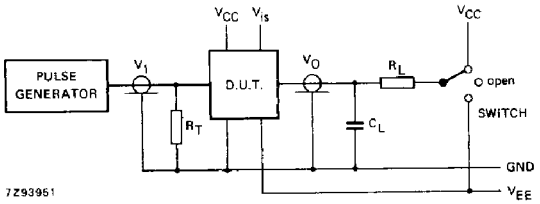


Fig. 20 Test circuit for measuring AC performance.

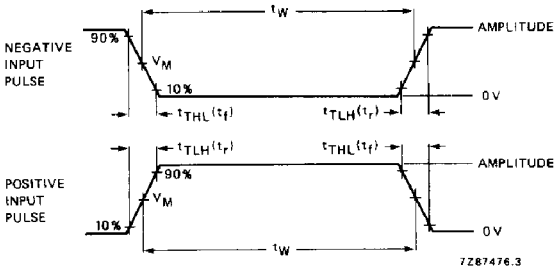


Fig. 21 Input pulse definitions.

Conditions

TEST	SWITCH	V_{is}
t_{PZH}	V_{EE}	V_{CC}
t_{PZL}	V_{CC}	V_{EE}
t_{PHZ}	V_{EE}	V_{CC}
t_{PLZ}	V_{CC}	V_{EE}
others	open	pulse

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Definitions for Figs 20 and 21:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint to t_r, t_f with 50% duty factor.