3.3V 10Base-T/100Base-TX Integrated PHYceiver™

General

The ICS1893AF is a lower cost, re-packaged version of the ICS1893Y-10. The ICS1893AF is a fully integrated, Physical Layer device (PHY) that is compliant with both the 10Base-T and 100Base-TX CSMA/CD Ethernet Standard, ISO/IEC 8802-3. The ICS1893AF uses the same proven silicon as the ICS1893Y-10 but offers a lower cost solution by using a lower cost 300mil 48-lead SSOP package.

All parametric specifications and timing diagrams for the ICS1893Y-10 apply to the ICS1893AF. Refer to the 1893 Data Sheet for detailed specifications and timings.

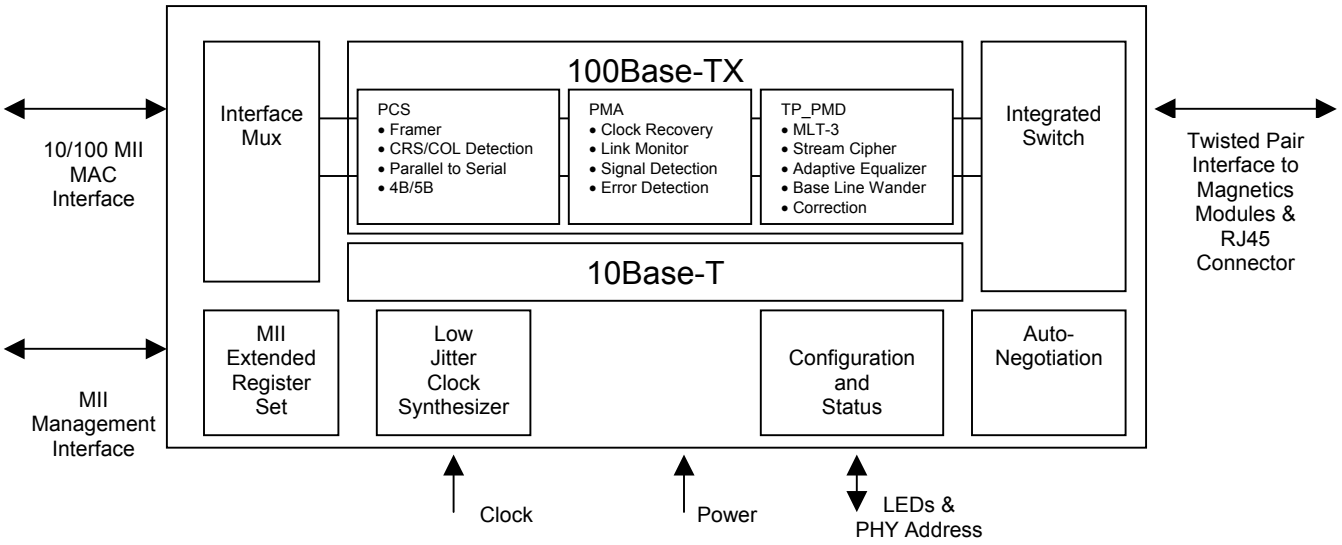
The ICS1893AF uses the same twisted-pair transmit and receive circuits as the ICS1893Y-10, and the same recommended board layout techniques apply to the ICS1893AF.

The ICS1893AF is intended for Node applications using the standard MII interface to the MAC.

All changes are listed in the ICS1893AF / ICS1893Y-10 Feature Set Comparison Table on page 2.

ICS1893AF Features

- Single 3.3V power supply
- Supports category 5 cables with attenuation in excess of 24dB at 100 MHz across a temperature range from -5º to +85º C.
- DSP-based baseline wander correction to virtually eliminate killer packets across temperature range of -5º to +85º C.
- Low-power, 0.35-micron CMOS (typically 400mW)
- Single-chip, fully integrated PHY provides PCS, PMA, PMD and AUTONEG Sublayers of the IEEE Std.
- 10Base-T and 100Base-TX IEEE 8802-3 compliant
- Clock or crystal supported.
- Media Independent Interface (MII) supported.
- Managed or Unmanaged Applications
- 10M or 100M Half and Full Duplex Modes
- Auto-Negotiation with Next Page. Parallel detection for Legacy products.
- Fully-integrated, DSP-based PMD includes:
  - Adaptive equalization and baseline wander correction
  - Transmit wave shaping and stream cipher scrambler
  - MLT-3 encoder and NRZ/NRZI encoder
- Highly configurable supports:
  - Node applications, managed or unmanaged
  - 10M or 100M half and full duplex modes
- Loopback mode for Diagnostic Functions
- Small footprint 48-lead 300mil SSOP package.



ICS1893 Block Diagram

Document Revision: 5 April 2002

Typical ICS1893AF Applications

The ICS1893AF is configured for the majority of single Phy Ethernet applications. These applications include Network Interface Cards, PC Motherboards, Printers, ACR Riser cards, Set top Boxes, and Game machines.

Virtually any single Phy application utilizing the standard IEEE MII interface can use the ICS1893AF. The ICS1893AF offers the same high performance at a lower cost.

ICS1893AF / ICS1893Y-10 Feature Set Comparison Table

Feature	ICS1893AF	ICS1893Y-10	Comment
Package Type	SSOP 300mil	TQFP 10x10x1.4	
Pin Count	48	64	
NOD/REP	NOD/REP pin removed tied internally to VSS	NOD/REP	ICS1893AF configured in NODE mode only.
HW/SW	HW/SW pin removed tied internally to VDD	HW/SW	ICS1893AF configured in software mode only.
MII/SI	SI/MII pin removed tied internally to VDD	SI/MII	ICS1893AF supports only MII interface to MAC.
10/100	10/100 pin is output only	10/100	The 10/100 pin in software mode is an output indicateting 100M operation when high
DPXSEL	DPXSEL pin removed	DPXSEL	FD/HD information is available in the Quick Poll Status Register Reg 17
ANSEL	ANSEL pin removed	ANSEL	ANSEL in software mode is an output. This information is available in control Reg 0, Default setting is A-N enabled
LSTA	LSTA pin removed	LSTA	Link status available on P2LI led
LOCK	LOCK pin removed	LOCK	Link status available on P2LI led
TXER	TXER pin removed tied internally to VSS	TXER	TXER function is still available by using control Reg 16 bit 2

The following bullet items describe ICS1893AF pin differences and how they affect the application:

- The ICS1893AF is hardwired for the predominate board application used in the vast majority of single Phy applications
  - Hardwired for Node configuration (NOD/REP pin removed, tied internally to VSS). Node configuration enables the 10M SQE test default setting and causes CRS to be asserted for either transmit or receive activity in half duplex, or for just receive activity when in full duplex.
  - Hardwired for Software mode (HW/SW pin removed, tied internally to VDD).
  - Hardwired for MII interface only. (SI/MII pin removed, tied internally to VDD) In this configuration the 10baseT serial and 100baseTX 5 bit symbol interfaces are NOT supported. Applications requiring these interfaces should use ICS1893Y-10.

- In the software control configuration the 10/100, DPXSEL and ANSEL pins are outputs.
  - DPXEL pin is not brought out.
  - ANSEL pin is not brought out.
  - 10/100 pin is brought out to indicate 100M operation. Some applications use this output to drive an LED indicating 100M operation.

- Pins LSTA (link status) and LOCK (rec. PLL locked) are not brought out.
    - LSTA and LOCK provided redundant information already available with the P2LI pin. P2LI indicates the Link is valid.

- Input pin TXER is removed and tied low inside the package. The TXER function is still available by using the Extended Control Register Reg 16 Bit 2. Most applications tied the TXER pin to VSS.

ICS1893AF Shared Features

- The same silicon die is used in the ICS1893AF and ICS1893Y-10.
    - Only the package type is different.

- The ICS1893AF offers the same .35µ 3.3V low power operation.

- Parametric specifications and timing diagrams same as ICS1893Y-10.

    - See ICS1893 Data Sheet for specification and timing details.

- Both the ICS1893Y-10 and the ICS1893AF incorporate Digital Signal Processing in their PMD Sub layer, thereby allowing them to transmit and receive data with Unshielded Twisted Pair (UTP) Category 5 cables up to 150 meters in length. In addition, this ICS-patented, technology has allowed the ICS1893Y-10 and ICS1893AF to address the effects of Baseline Wander correction with UTP cable lengths up to 150m.

- Both ICS1893AF and ICS1893Y-10 have improved 10Base-T Squelch operation.
- The 1893AF uses the same twisted pair transmitter and receive circuits and therefore the same recommended board layout techniques apply. See Typical Board Layout section.
- Both share improved transmit circuits resulting in decrease in the magnitude of the 10Base-T harmonic content generated during transmission (reference ISO/IEC 8802-3: 1993 Clause 8.3.1.3).

- Both use digital PLL technology resulting in lower jitter and improved stability.

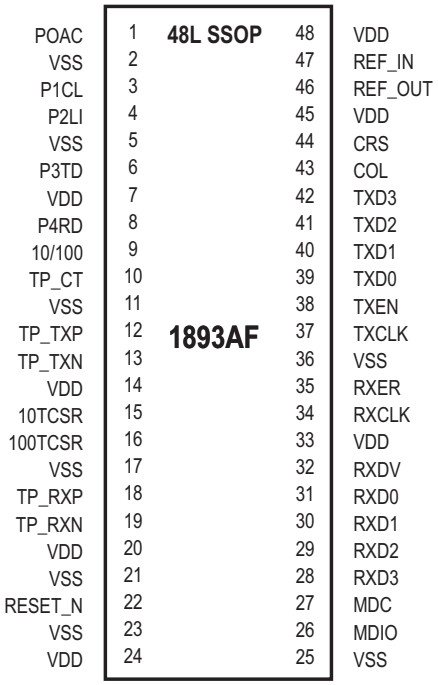
- Both seed the transmit stream cipher with the PHY address. This minimizes cross-talk, EMI and noise in multiple Phy applications.
- The MDIO Maintenance interface with the MDIO and MDC pins along with all internal registers are preserved in the ICS1893AF. This allows software configuring for FD/HD, 10baseT, 100baseTX and Auto-Negotiation to be configurable by the MDIO maintenance interface. Default setting is Auto-Negotiation Enable. All register settings are the same as in the ICS1893 datasheet.

- The ICS1893AF preserves the dual purpose LED/Phy Address control pins as in the ICS1893Y-10. The captured address seeds the scrambler for lower EMI in for multiple Phy applications.

- All Auto-Negotiation features are preserved in the ICS1893AF. The reset default mode is A_N enabled. The A_N parallel detect feature is preserved for legacy interoperability.

- Both support the Auto-Negotiation Next Page functions as described in IEEE Std 802.3u-1995 clause 28.2.3.4
- Both support Management Frame (MF) Preamble Suppression.
- Both support backward compatibility with the ICS1890 Management Registers

ICS1893AF Pin Diagram



ICS1893AF Pin Descriptions

Transformer Interface Pins		
Signal Name	**Pin No.**	**Signal Description**
TP_TXP	12	Twisted Pair Transmit Positive
TP_TXN	13	Twisted Pair Transmit Negative
TP_CT	10	Twisted Pair Center Tap
TP_RXP	18	Twisted Pair Receive Positive
TP_RXN	19	Twisted Pair Receive Negative

Multifunction Pins: PHY Address and LED Pins		
Signal Name	**Pin No.**	**Signal Description**
P4RD	8	Bit 4 of PHY Address, PHYAD[4], OR Receive LED
P3TD	6	Bit 3 of PHY Address, PHYAD[3], OR Transmit LED
P2LI	4	Bit 2 of PHY Address, PHYAD[2], OR Link Integrity LED
P1CL	3	Bit 1 of PHY Address, PHYAD[1], OR Collision LED
P0AC	1	Bit 0 of PHY Address, PHYAD[0], OR Activity LED

ICS1893AF Pin Descriptions *(Cont'd.)*

Configuration Pins		
Signal Name	**Pin No**	**Signal Description**
10/100	9	Output Indication , High=100baseTX Operation
100TCSR	16	100M Transmit Current Set Resistors (see Figure)
10TCSR	15	10M Transmit Current Set Resistor
REFIN	47	Frequency Reference Input: 25 MHz Input Clock or Crystal
REFOUT	46	Frequency Reference Output for Crystal
RESETn	22	System Reset (active low)

MAC/Repeater Interface Pins		
Signal Name	**Pin No.**	**Signal Description**
MDIO	26	Management Data Input/Output
MDC	27	Management Data Clock
RXD3	28	Receive Data 3
RXD2	29	Receive Data 2
RXD1	30	Receive Data 1
RXD0	31	Receive Data 0
RXDV	32	Receive Data Valid
RXCLK	34	Receive Clock
RXER	35	Receive Error
TXCLK	37	Transmit Clock
TXEN	38	Transmit Enable
TXD0	39	Transmit Data 0
TXD1	40	Transmit Data 1
TXD2	41	Transmit Data 2
TXD3	42	Transmit Data 3
COL	43	Collision Detect
CRS	44	Carrier Sense

ICS1893AF Pin Descriptions *(Cont'd.)*

Power and Ground Pins		
Signal Name	**Pin No.**	**Signal Description**
Power		
VDD	7	3.3V
VDD	14	3.3V
VDD	20	3.3V
VDD	24	3.3V
VDD	33	3.3V
VDD	45	3.3V
VDD	48	3.3V
Ground		
VSS	2	
VSS	5	
VSS	11	
VSS	17	
VSS	21	
VSS	23	
VSS	25	
VSS	36	

Typical Board Layouts

Twisted-Pair Transmitter Interface

The twisted-pair transmitter driver uses an H-bridge configuration. .
ICS suggests using any of the following for the H-bridge:

- Halo TG22S012ND transformer
- Transpower HB617-LP transformer
- Pulse 68517 transformer which can be turned around to move the choke windings to the RJ-45 side.

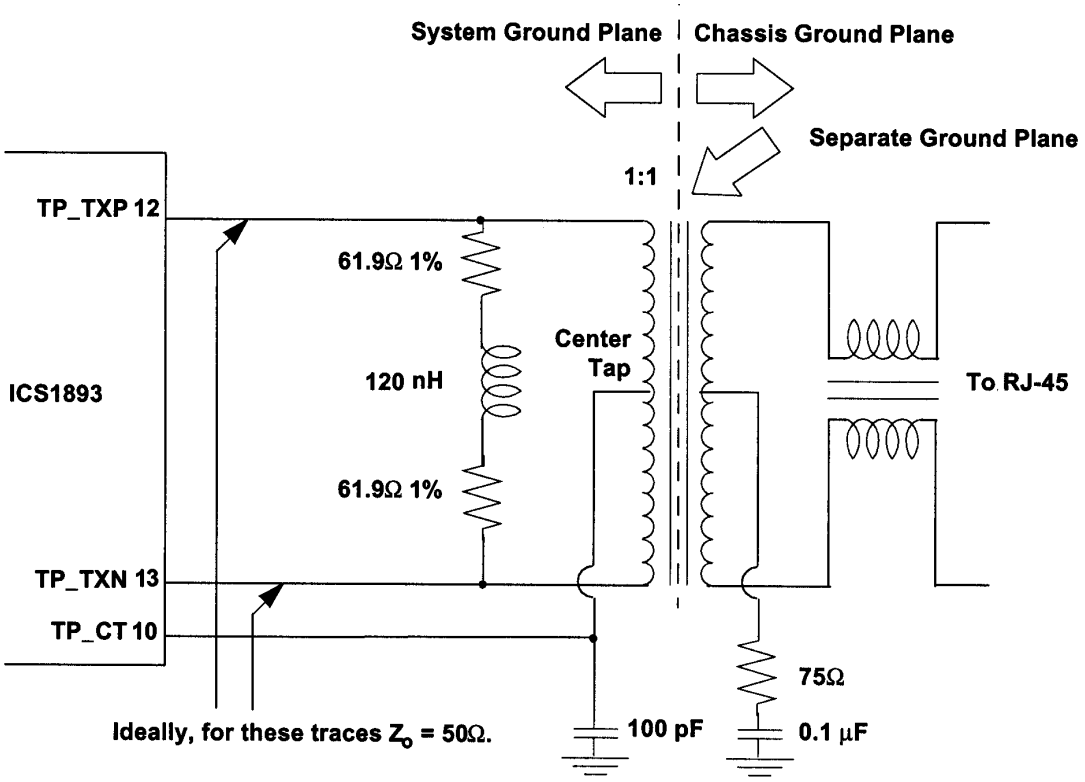
The figure below shows the design for the ICS1893 twisted-pair transmitter interface.

- Two 61.9Ω 1% resistors are in series, with a 120-nH 5% inductor between them. These components form a network that connects across both the transformer and the ICS1893 TP_TXP and TP_TXN pins.
- The ICS1893 transmitter output H drive configuration supplies power to the transformer. (No VDD connection is required.)
- The ICS1893 TP_CT pin is connected directly to the transformer transmit center tap connection and is bypassed to ground with a 100pF capacitor.

Note:

1. If the transformer has a choke, it may be put on the chip side, RJ-45 side or both.
2. Keep all TX traces as short as possible.
3. When making board traces, 50Ω–characteristic impedance is desirable.

ICS1893 Transmit Twisted Pair



Typical Board Layouts

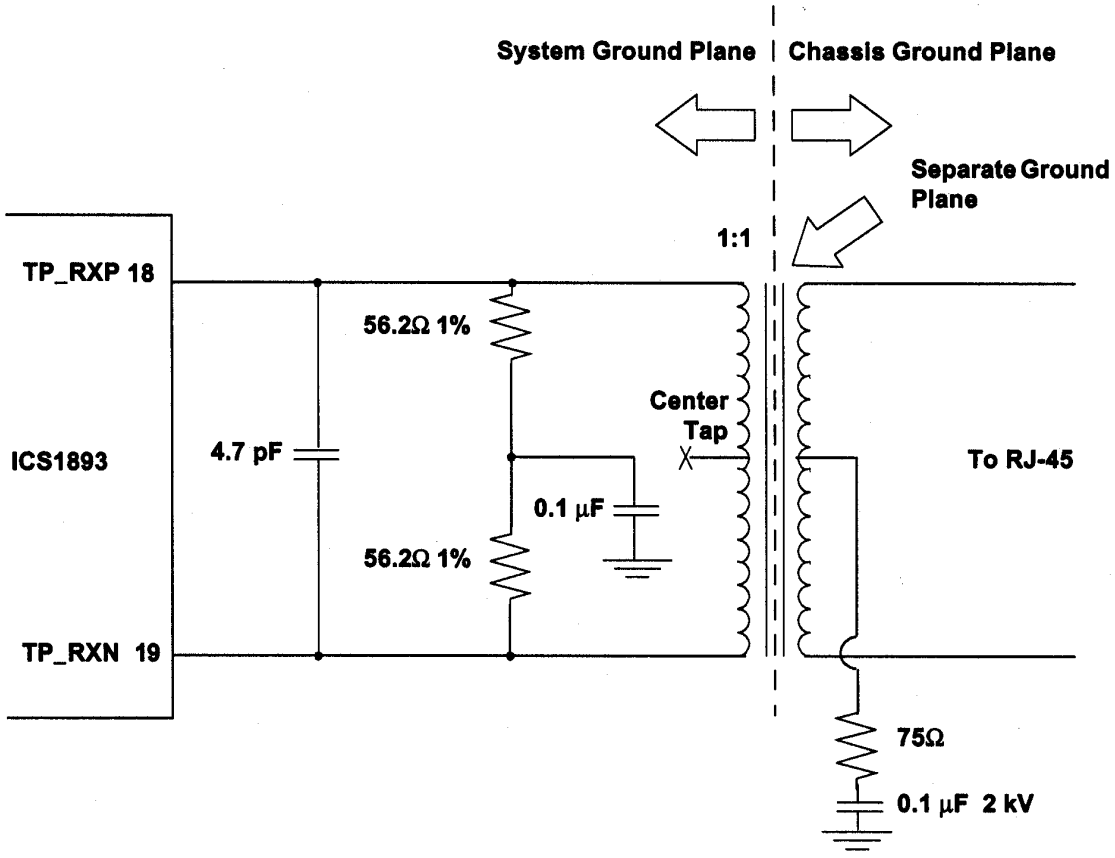
Twisted-Pair Receiver Interface

The figure below shows the design for the ICS1893 twisted-pair receiver interface.

- Two 56.2Ω 1% resistors are in series, with the center bypassed to ground with a 0.1µF bypass capacitor.
- No bypass capacitor is used with the receive transformer center tap.
- A 4.7-pF capacitor must be included across the ICS1893 side of the receive transformer.

Note:
1. Keep leads as short as possible.
2. Install the resistor network as close to the ICS1893 as possible.

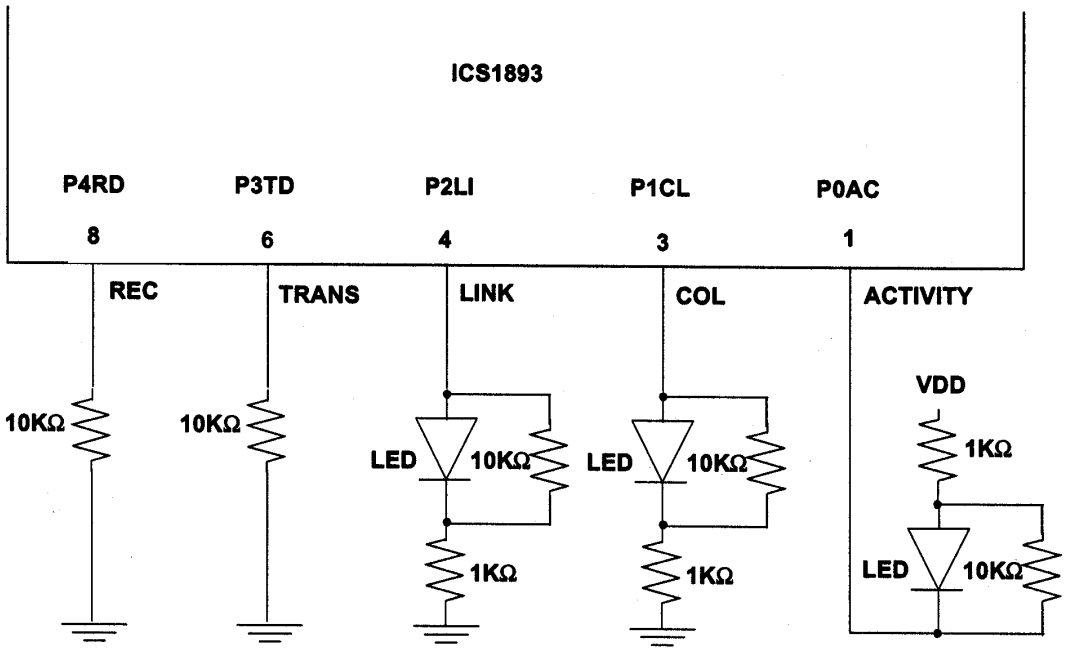
ICS1893 Receive Twisted Pair



Typical Board Layouts

The figure below shows a typical LED connection for the ICS1893.

ICS1893 LED – PHY Address Interface

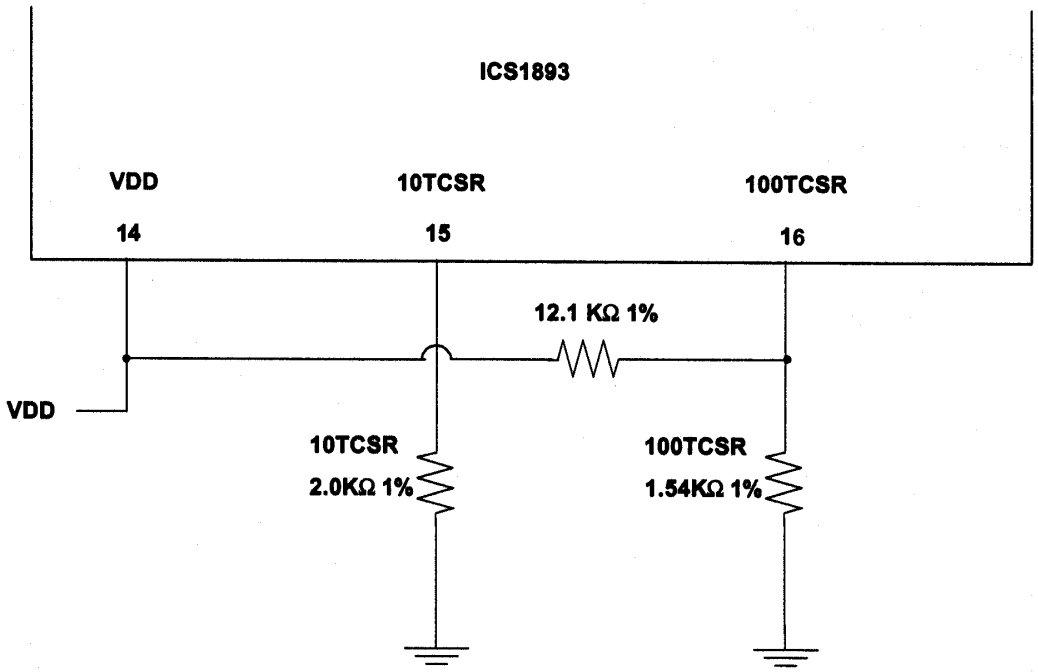


This circuit decodes to PHY address = 1.

Note:
1. All LED pins must be set during reset.
2. Caution - PHY address 00 will tri-states the MII interface. Don't use Phy address 00.
3. For more reliable address capture during power-on reset, add a 10KΩ resistor across the LED.

Typical Board Layouts

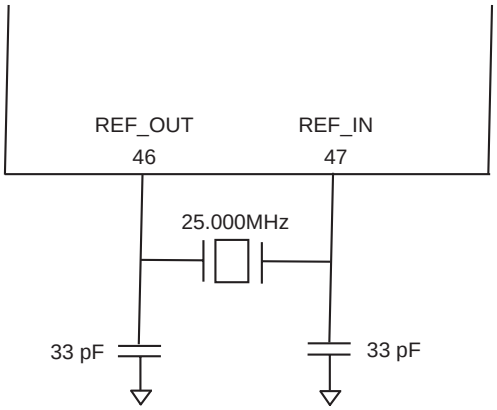
10TCSR and 100TCSR Bias Resistors



Note:

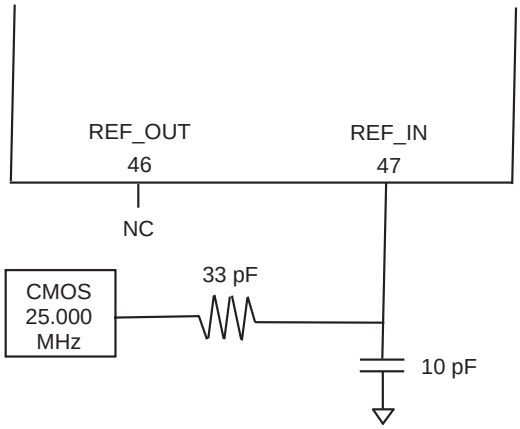
1. The VDD connection to the 12.1K resistor can connect to any VDD.

Cyrstal Operation



Or

Oscillator Operation



INTEGRATED CIRCUIT SYSTEMS, INC.

We've Got Your Timing Solution!™

For the most current information on ICS products, visit our web site at:

www.icst.com

Headquarters: 2435 Boulevard of the Generals
Valley Forge, PA 19482-0968
Tel: 610-630-5300
Fax: 610-630-5399

San Jose Operations: 525 Race Street
San Jose, CA 95126
Tel: 408-297-1201
Fax: 408-925-9460