National Semiconductor

November 2000

DS92LV1212A
16-40 MHz 10-Bit Bus LVDS Random Lock Deserializer with Embedded Clock Recovery

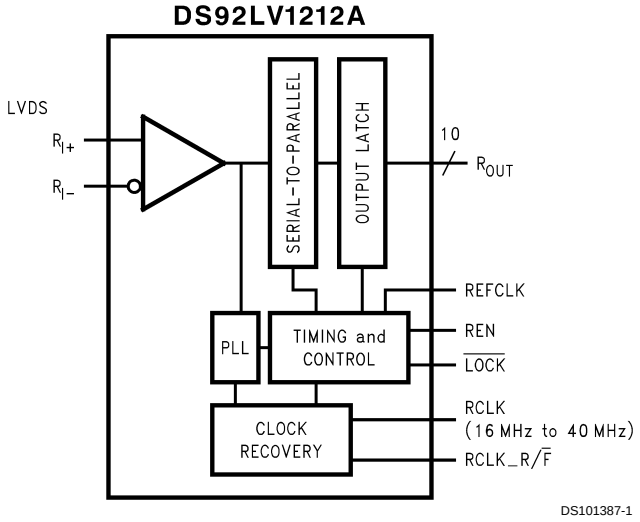
General Description

The DS92LV1212A is an upgrade of the DS92LV1212. It maintains all of the features of the DS92LV1212. The DS92LV1212A is designed to be used with the DS92LV1021 Bus LVDS Serializer. The DS92LV1212A receives a Bus LVDS serial data stream and transforms it into a 10-bit wide parallel data bus and separate clock. The reduced cable, PCB trace count and connector size saves cost and makes PCB layout easier. Clock-to-data and data-to-data skews are eliminated since one input receives both clock and data bits serially. The powerdown pin is used to save power by reducing the supply current when the device is not in use. The Deserializer will establish lock to a synchronization pattern within specified lock times but it can also lock to a data stream without SYNC patterns.

Features

- Clock recovery without SYNC patterns-random lock
- Guaranteed transition every data transfer cycle
- Chipset (Tx + Rx) power consumption < 300mW (typ) @ 40MHz
- Single differential pair eliminates multi-channel skew
- 400 Mbps serial Bus LVDS bandwidth (at 40 MHz clock)
- 10-bit parallel interface for 1 byte data plus 2 control bits or UTOPIA I Interface
- Synchronization mode and LOCK indicator
- Flow-through pinout for easy PCB layout
- High impedance on receiver inputs when power is off
- Programmable edge trigger on clock
- Footprint compatible with DS92LV1210
- Small 28-lead SSOP package-MSA

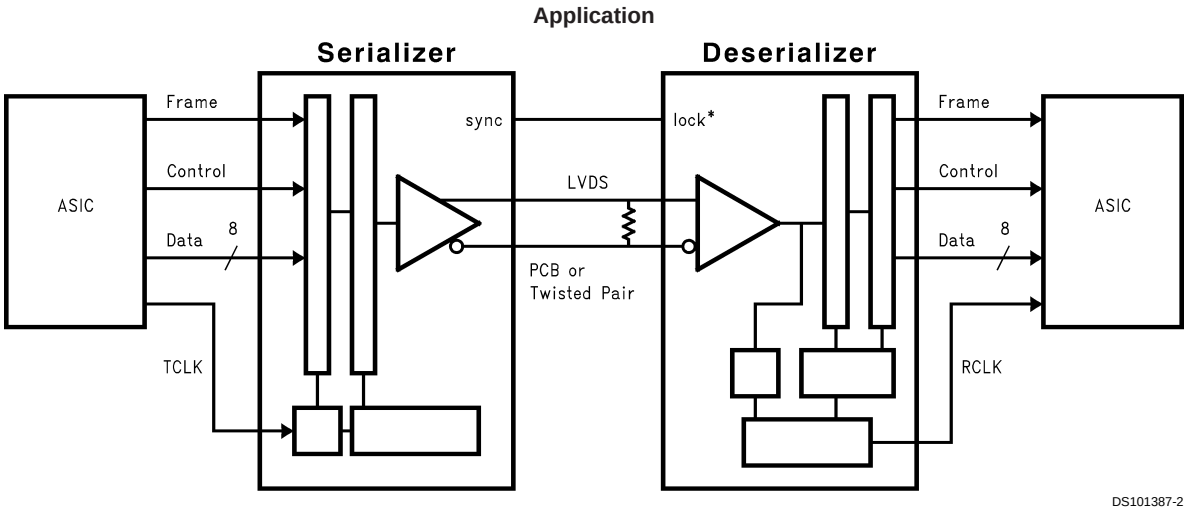
Block Diagram



DS101387-1

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Block Diagram (Continued)



Functional Description

The DS92LV1212 is a 10-bit Deserializer chip designed to receive data over heavily loaded differential backplanes at clock speeds from 16 MHz to 40 MHz. It may also be used to receive data over Unshielded Twisted Pair (UTP) cable.

The chip has three active states of operation: Initialization, Data Transfer, and Resynchronization; and two passive states: Powerdown and TRI-STATE®.

The following sections describe each operation of the active and passive states.

Initialization

Before data can be transferred, the Deserializer must be initialized. The Deserializer should be powered up with the PWRDN pin held low. After V_{CC} stabilizes, the PWRDN pin can be forced high. The Deserializer is ready to lock to the incoming data stream.

Step 1: When you apply V_{CC} to the Deserializer, the respective outputs are held in TRI-STATE and internal circuitry is disabled by on-chip power-on circuitry. When V_{CC} reaches V_{CC} OK (2.5V), the PLL is ready to lock to incoming data or synchronization patterns. You must apply the local clock to the REFCLK pin.

The Deserializer $\overline{\text{LOCK}}$ output will remain high while its PLL locks to incoming data or to SYNC patterns on the inputs.

Step 2: The Deserializer PLL must synchronize to the Serializer to complete the initialization. The Deserializer will lock to non-repetitive data patterns; however, the transmission of SYNC patterns to the Deserializer enables the Deserializer to lock to the Serializer signal within a specified time. See *Figure 7*.

The user's application determines control of the SYNC1 and SYNC2 pins. One recommendation is a direct feedback loop from the $\overline{\text{LOCK}}$ pin. Under all circumstances, the Serializer stops sending SYNC patterns after both SYNC inputs return low.

When the Deserializer detects edge transitions at the Bus LVDS input, it will attempt to lock to the embedded clock information. When the Deserializer locks to the Bus LVDS clock, the $\overline{\text{LOCK}}$ output will go low. When $\overline{\text{LOCK}}$ is low, the Deserializer outputs represent incoming Bus LVDS data.

Data Transfer

After initialization, the Serializer will accept data from inputs DIN0–DIN9. The Serializer uses the TCLK input to latch incoming Data. The TCLK_R/$\overline{\text{F}}$ pin selects which edge the Serializer uses to strobe incoming data. TCLK_R/$\overline{\text{F}}$ high selects the rising edge for clocking data and low selects the falling edge. If either of the SYNC inputs is high for 5*TCLK cycles, the data at DIN0-DIN9 is ignored regardless of clock edge.

After determining which clock edge to use, a start and stop bit, appended internally, frame the data bits in the register. The start bit is always high and the stop bit is always low. The start and stop bits function as the embedded clock bits in the serial stream.

Serialized data and clock bits (10+2 bits) are received at 12 times the TCLK frequency. For example, if TCLK is 40 MHz, the serial rate is 40 x 12 = 480 Mega bits per second. Since only 10 bits are from input data, the serial "payload" rate is 10 times the TCLK frequency. For instance, if TCLK = 40 MHz, the payload data rate is 40 x 10 = 400 Mbps. TCLK is provided by the data source and must be in the range 16 MHz to 40 MHz nominal.

The $\overline{\text{LOCK}}$ pin on the Deserializer is driven low when it is synchronized with the Serializer. The Deserializer locks to the embedded clock and uses it to recover the serialized data. ROUT data is valid when $\overline{\text{LOCK}}$ is low. Otherwise, ROUT0–ROUT9 is invalid.

The ROUT0-ROUT9 pins use the RCLK pin as the reference to data. The polarity of the RCLK edge is controlled by the RCLK_R/$\overline{\text{F}}$ input. See *Figure 5*.

ROUT(0-9), $\overline{\text{LOCK}}$ and RCLK outputs will drive a minimum of three CMOS input gates (15 pF load) with 40 MHz clock.

Resynchronization

When the Deserializer PLL locks to the embedded clock edge, the Deserializer $\overline{\text{LOCK}}$ pin asserts a low. If the Deserializer loses lock, the $\overline{\text{LOCK}}$ pin output will go high and the outputs (including RCLK) will enter TRI-STATE.

The user's system monitors the $\overline{\text{LOCK}}$ pin to detect a loss of synchronization. Upon detection, the system can arrange to pulse the Serializer SYNC1 or SYNC2 pin to resynchronize. Multiple resynchronization approaches are possible. One

Resynchronization (Continued)

recommendation is to provide a feedback loop using the LOCK pin itself to control the sync request of the Serializer (SYNC1 or SYNC2). Dual SYNC pins are provided for multiple control in a multi-drop application. Sending sync patterns for resynchronization is desirable when lock times within a specific time are critical. However, the Deserializer can lock to random data, which is discussed in the next section.

Random Lock Initialization and Resynchronization

The initialization and resynchronization methods described in their respective sections are the fastest ways to establish the link between the Serializer and Deserializer. However, the DS92LV1212A can attain lock to a data stream without requiring the Serializer to send special SYNC patterns. This allows the DS92LV1212A to operate in “open-loop” applications. Equally important is the Deserializer’s ability to support hot insertion into a running backplane. In the open loop or hot insertion case, we assume the data stream is essentially random. Therefore, because lock time varies due to data stream characteristics, we cannot possibly predict exact lock time. The primary constraint on “random” lock time is the initial phase relation between the incoming data and the REFCLK when the Deserializer powers up. As described in the next paragraph, the data contained in the data stream can also affect lock time.

If a specific pattern is repetitive, the Deserializer could enter “false lock” - falsely recognizing the data pattern as the clocking bits. We refer to such a pattern as a repetitive multi-transition, RMT. This occurs when more than one Low-High transition takes place in a clock cycle over multiple cycles. This occurs when any bit, except DIN 9, is held at a low state and the adjacent bit is held high, creating a 0-1 transition. In the worst case, the Deserializer could become locked to the data pattern rather than the clock. Circuitry within the DS92LV1212A can detect that the possibility of “false lock” exists. The circuitry accomplishes this by detecting more than one potential position for clocking bits. Upon detection, the circuitry will prevent the LOCK output from becoming active until the potential “false lock” pattern changes. The false lock detect circuitry expects the data will eventually change, causing the Deserializer to lose lock to the data pattern and then continue searching for clock bits in the serial data stream. Graphical representations of RMT are shown on the following page. Please note that RMT only applies to bits DIN0-DIN8.

Powerdown

When no data transfer occurs, you can use the Powerdown state. The Serializer and Deserializer use the Powerdown state, a low power sleep mode, to reduce power consumption. The Deserializer enters Powerdown when you drive PWRDN and REN low. The Serializer enters Powerdown when you drive PWRDN low. In Powerdown, the PLL stops and the outputs enterTRI-STATE, which disables load current and reduces supply current to the milliampere range. To exit Powerdown, you must drive the PWRDN pin high.

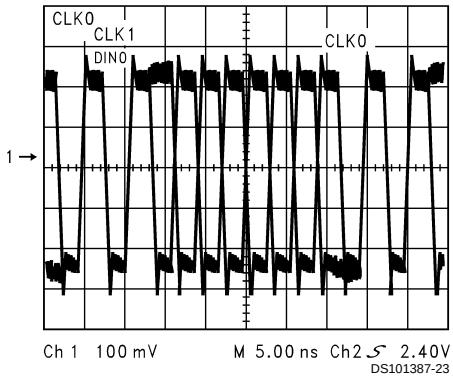
Before valid data exchanges between the Serializer and Deserializer, you must reinitialize and resynchronize the devices to each other. Initialization of the Serializer takes 510 TCLK cycles. The Deserializer will initialize and assert LOCK high until lock to the Bus LVDS clock occurs.

TRI-STATE

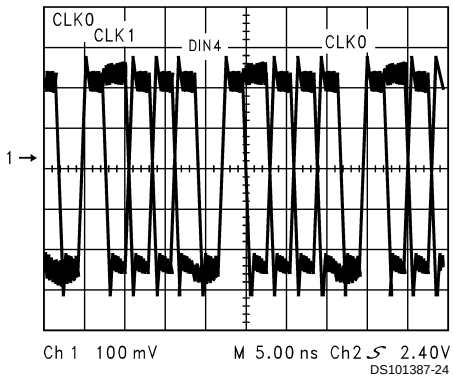
The Serializer enters TRI-STATE when the DEN pin is driven low. This puts both driver output pins (DO+ and DO−) into TRI-STATE. When you drive DEN high, the Serializer returns to the previous state, as long as all other control pins remain static (SYNC1, SYNC2, PWRDN, TCLK_R/F).

When you drive the REN pin low, the Deserializer enters TRI-STATE. Consequently, the receiver output pins (ROUT0–ROUT9) and RCLK will enter TRI-STATE. The LOCK output remains active, reflecting the state of the PLL.

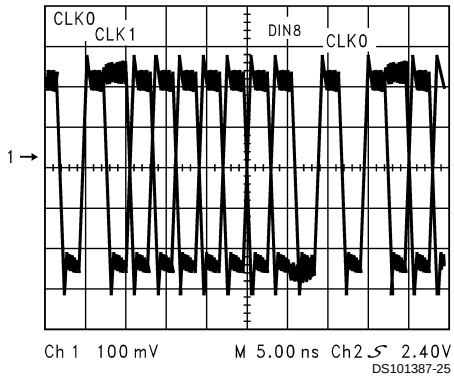
RMT Patterns



DIN0 Held Low-DIN1 Held High Creates an RMT Pattern



DIN4 Held Low-DIN5 Held High Creates an RMT Pattern



DIN8 Held Low-DIN9 Held High Creates an RMT Pattern

Order Numbers		
NSID	Function	Package
DS92LV1021TMSA	Serializer	MSA28
DS92LV1212AMSA	Deserializer	MSA28

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
CMOS/TTL Input Voltage	−0.3V to (V_{CC} +0.3V)
CMOS/TTL Output Voltage	−0.3V to (V_{CC} +0.3V)
Bus LVDS Receiver Input Voltage	−0.3V to +3.9V
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering, 4 seconds)	+260˚C
Maximum Package Power Dissipation Capacity @ 25˚C Package: 28L SSOP	1.27 W
Package Derating: 28L SSOP	10.3mW/˚C above +25˚C
ESD Rating (HBM)	>2kV

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+85	˚C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100 mV_{P-P}	

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DESERIALIZER LVCMOS/LVTTL DC SPECIFICATIONS (apply to pins $\overline{PWRDN}$, RCLK_R/ $\overline{F}$, REN, REFCLK = inputs; apply to pins ROUT, RCLK, $\overline{LOCK}$ = outputs)							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.62	−1.5	V
I_{IN}	Input Current	V_{IN} = 0V or 3.6V		−10	±2	+15	µA
V_{OH}	High Level Output Voltage	I_{OH} = −9 mA		2.1	2.93	V_{CC}	V
V_{OL}	Low Level Output Voltage	I_{OL} = 9 mA		GND	0.33	0.5	V
I_{OS}	Output Short Circuit Current	VOUT = 0V		−15	−38	−85	mA
I_{OZ}	TRI-STATE Output Current	$\overline{PWRDN}$ or REN = 0.8V, V_{OUT} = 0V or VCC		−10	±0.4	+10	µA
DESERIALIZER Bus LVDS DC SPECIFICATIONS (apply to pins RI+ and RI−)							
VTH	Differential Threshold High Voltage	VCM = +1.1V			+6	+50	mV
VTL	Differential Threshold Low Voltage			−50	−12		mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{CC} = 3.6V or 0V		−10	±1	+15	µA
		V_{IN} = 0V, V_{CC} = 3.6V or 0V		−10	±0.05	+10	µA
DESERIALIZER SUPPLY CURRENT (apply to pins DVCC and AVCC)							
I_{CCR}	Deserializer Supply Current	C_L = 15 pF	f = 40 MHz		58	75	mA
	Worst Case	*Figure 1*	f = 16 MHz		30	45	mA
I_{CCXR}	Deserializer Supply Current Powerdown	$\overline{PWRDN}$ = 0.8V, REN = 0.8V			0.36	1.0	mA

Deserializer Timing Requirements for REFCLK

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{RFCP}	REFCLK Period		25	T	62.5	ns
t_{RFDC}	REFCLK Duty Cycle			50		%
f_{Ref}	REFCLK Frequency		0.95/t_{RCP}	t_{RCP}	1.05/t_{RCP}	
t_{RFTT}	REFCLK Transition Time			3	6	ns

Deserializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{RCP}	Receiver out Clock Period	*Figure 3* $t_{RCP} = t_{TCP}$	RCLK	25		62.5	ns
t_{CLH}	CMOS/TTL Low-to-High Transition Time	CL = 15 pF *Figure 2*	Rout(0-9), $\overline{LOCK}$, RCLK		1.2	4	ns
t_{CHL}	CMOS/TTL High-to-Low Transition Time				1.1	4	ns
t_{DD}	Deserializer Delay	*Figure 4*	All Temp./All Freq.	$1.75*t_{RCP}+ 1.25$	$1.75*t_{RCP}+3.75$	$1.75*t_{RCP}+6.25$	ns
			Room Temp 3.3V/40MHz	$1.75*t_{RCP}+ 2.25$	$1.75*t_{RCP}+3.75$	$1.75*t_{RCP}+5.25$	
t_{ROS}	ROUT (0-9) Setup Data to RCLK	*Figure 5*	RCLK	$0.4*t_{RCP}$	$0.5*t_{RCP}$		ns
t_{ROH}	ROUT (0-9) Hold Data to RCLK			$-0.4*t_{RCP}$	$-0.5*t_{RCP}$		ns
t_{RDC}	RCLK Duty Cycle			45	50	55	%
t_{HZR}	HIGH to TRI-STATE Delay	*Figure 6*	Rout(0-9), $\overline{LOCK}$		$4.2+0.5*t_{RCP}$	$10+t_{RCP}$	ns
t_{LZR}	LOW to TRI-STATE Delay				$4.5+0.5*t_{RCP}$	$10+t_{RCP}$	ns
t_{ZHR}	TRI-STATE to HIGH Delay				$6+0.5*t_{RCP}$	$12+t_{RCP}$	ns
t_{ZLR}	TRI-STATE to LOW Delay				$6.0+0.5*t_{RCP}$	$12+t_{RCP}$	ns
t_{DSR1}	Deserializer PLL Lock Time from PWRDWN (with SYNCPAT)	*Figure 7* *Figure 8* (Note 4)	16MHz		4	10	µs
			40MHz		1.31	3	µs
t_{DSR2}	Deserializer PLL Lock time from SYNCPAT		16MHz		1.2	5	µs
			40MHz		0.47	1	µs
t_{ZHLK}	TRI-STATE to HIGH Delay (Power-up)		$\overline{LOCK}$		4.62	12	ns
t_{RNM}	Deserializer Noise Margin	*Figure 9* (Note 5)	16 MHz	900	1100		ps
			40 MHz	450	730		ps

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Typical values are given for V_{CC} = 3.3V and T_A = +25˚C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.

Note 4: For the purpose of specifying Deserializer PLL performance tDSR1 and tDSR2 are specified with the REFCLK running and stable, and specific conditions of the incoming data stream (SYNCPATs). It is recommended that the Deserializer be initialized using either tDSR1 timing or tDSR2 timing. tDSR1 is the time required for the Deserializer to indicate lock upon power-up or when leaving the power-down mode. Synchronization patterns should be sent to the device before initiating either condition. tDSR2 is the time required to indicate lock for the powered-up and enabled Deserializer when the input (RI+ and RI-) conditions change from not receiving data to receiving synchronization patterns (SYNCPATs).

Note 5: tRNM is a measure of how much phase noise (jitter) the Deserializer can tolerate in the incoming data stream before bit errors occur.

AC Timing Diagrams and Test Circuits

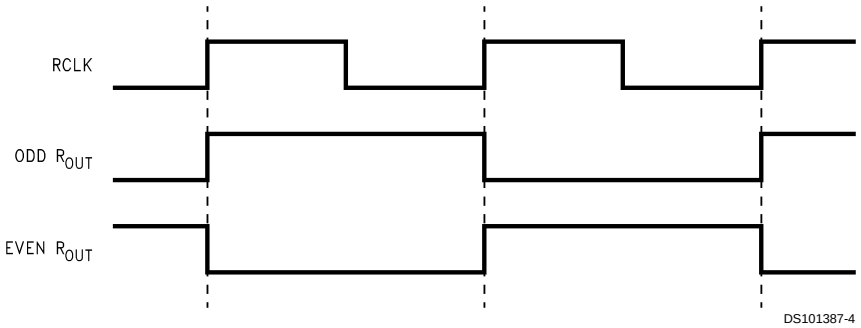


FIGURE 1. "Worst Case" Deserializer ICC Test Pattern

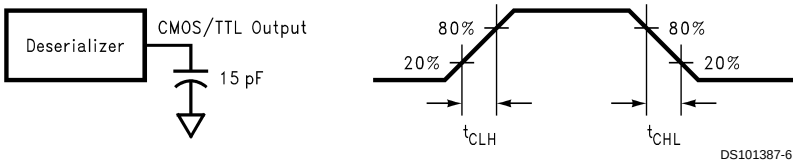


FIGURE 2. Deserializer CMOS/TTL Output Load and Transition Times

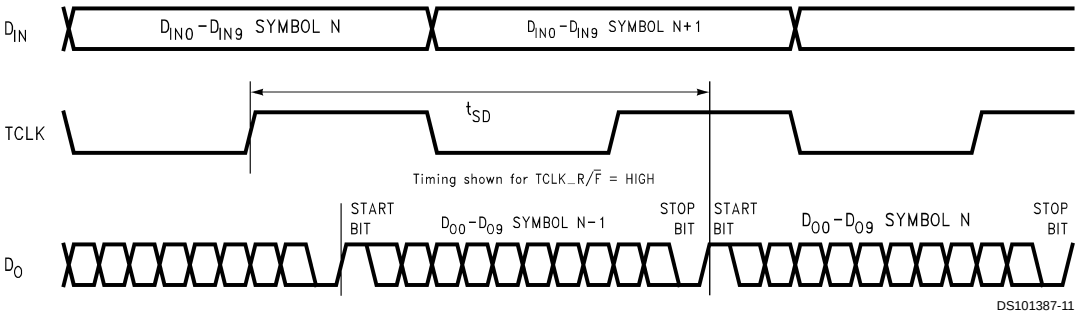


FIGURE 3. Serializer Delay

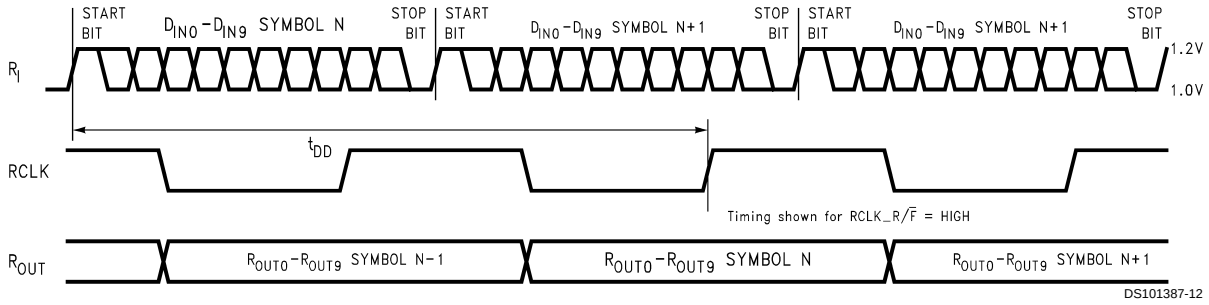
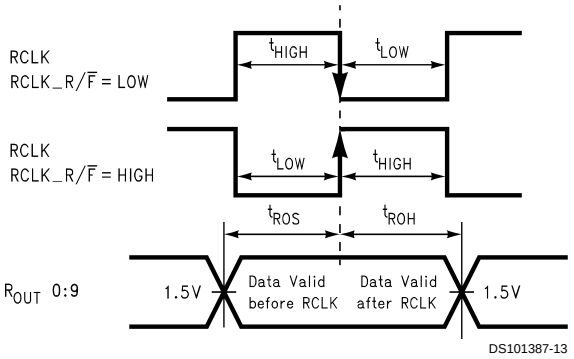


FIGURE 4. Deserializer Delay

AC Timing Diagrams and Test Circuits (Continued)



Timing shown for RCLK_R/$\overline{F}$ = LOW

Duty Cycle (t_{RDC}) = $\dfrac{t_{HIGH}}{t_{HIGH} + t_{LOW}}$

FIGURE 5. Deserializer Setup and Hold Times

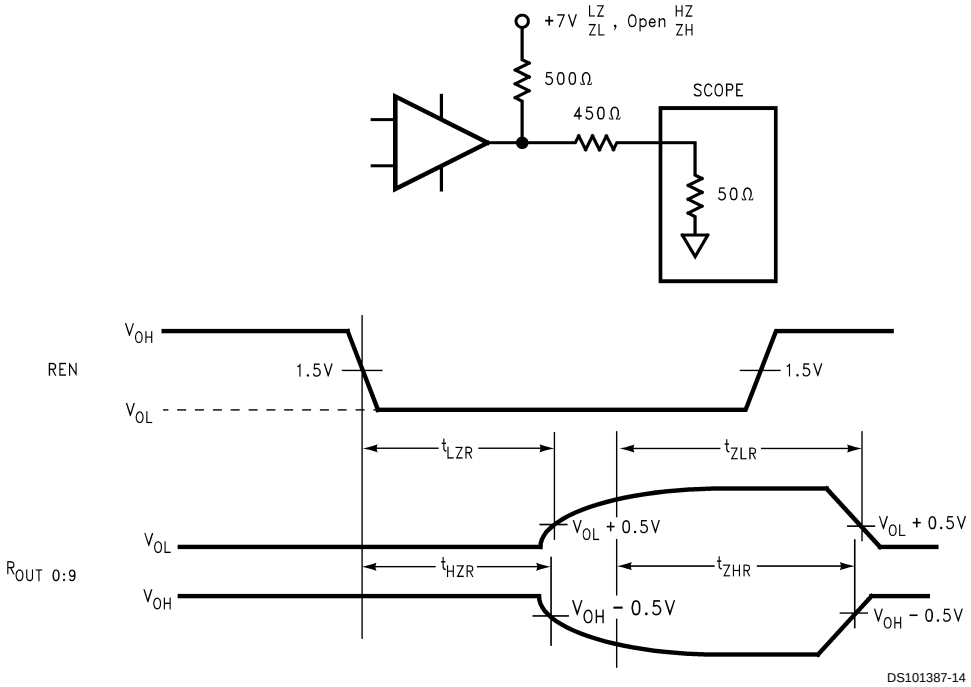


FIGURE 6. Deserializer TRI-STATE Test Circuit and Timing

AC Timing Diagrams and Test Circuits (Continued)

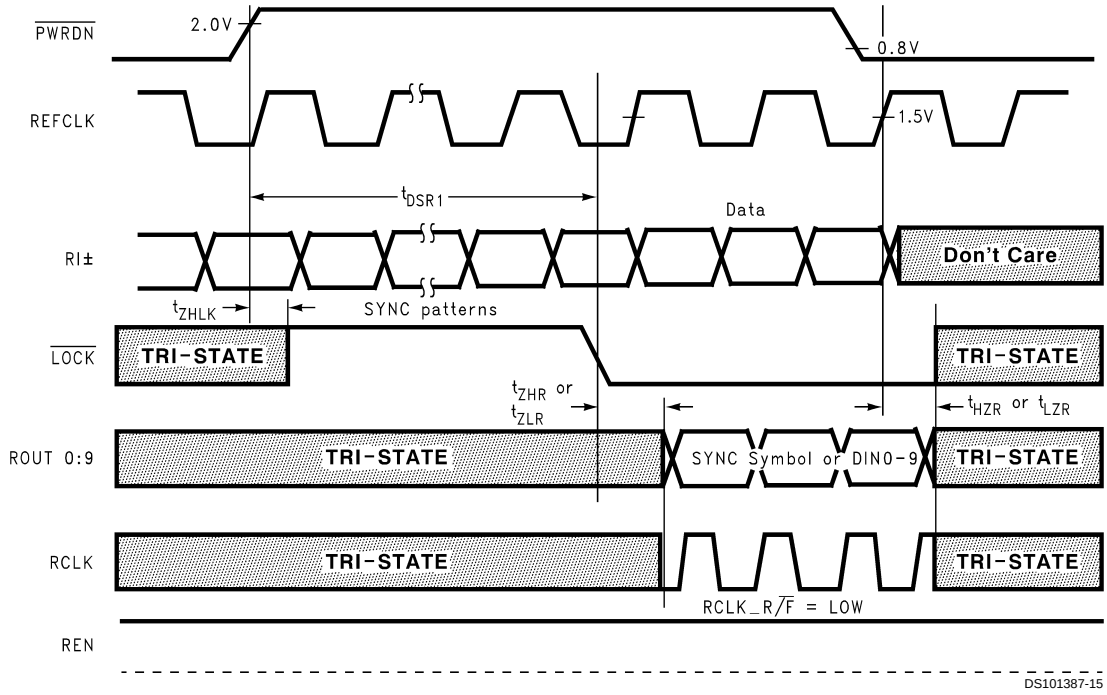


FIGURE 7. Deserializer PLL Lock Times and $\overline{\text{PWRDN}}$ TRI-STATE Delays

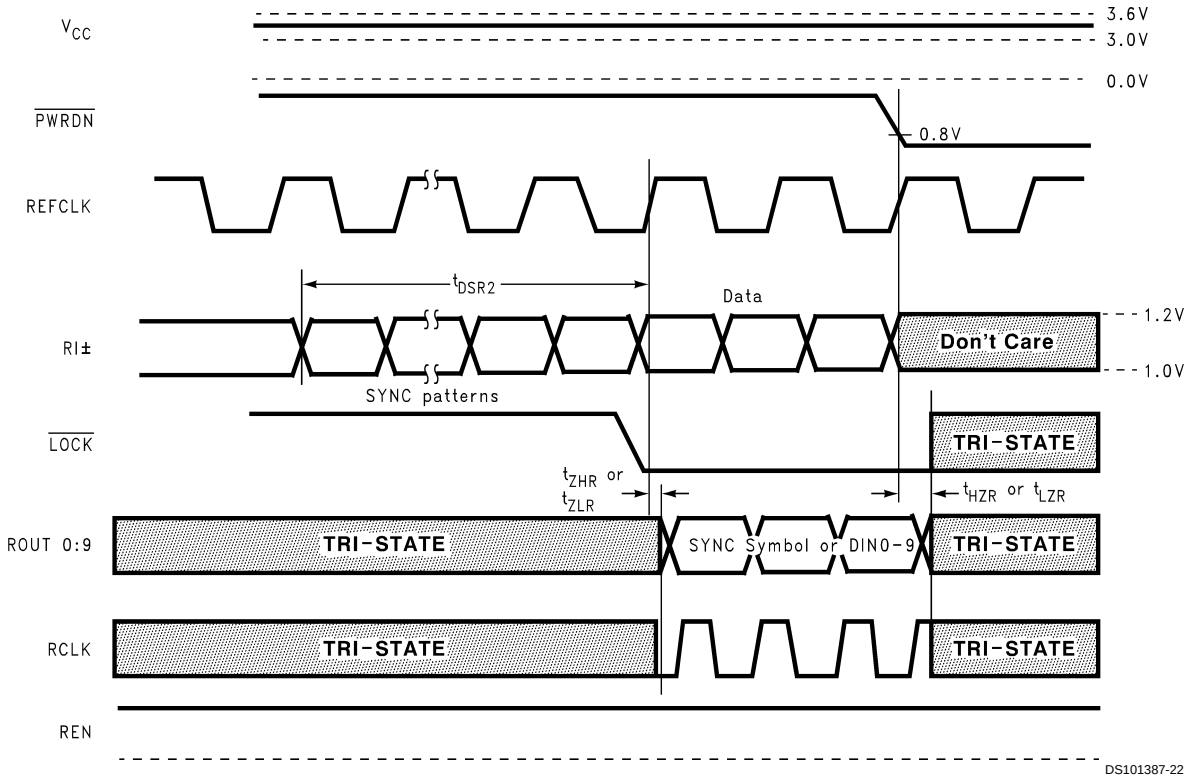
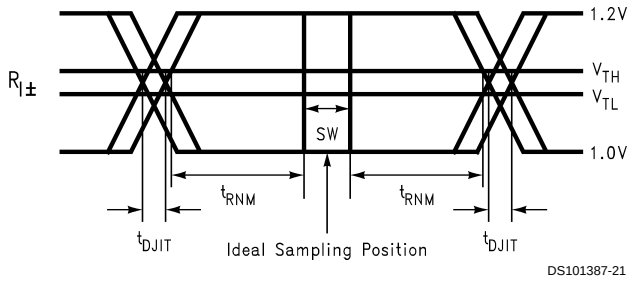


FIGURE 8. Deserializer PLL Lock Time from SyncPAT

AC Timing Diagrams and Test Circuits (Continued)



SW - Setup and Hold Time (Internal data sampling window)
t_{JIT}- Serializer Output Bit Position Jitter
t_{RSM} = Receiver Sampling Margin Time

FIGURE 9. Receiver Bus LVDS Input Skew Margin

Application Information

Using the DS92LV1021 and DS92LV1212A

The Serializer and Deserializer chipset is an easy to use transmitter and receiver pair that sends 10 bits of parallel LVTTL data over a serial Bus LVDS link up to 660 Mbps. An on-board PLL serializes the input data and embeds two clock bits within the data stream. The Deserializer uses a separate reference clock (REFCLK) and an onboard PLL to extract the clock information from the incoming data stream and then deserialize the data. The Deserializer monitors the incoming clock information, determines lock status, and asserts the $\overline{\text{LOCK}}$ output high when loss of lock occurs.

Power Considerations

An all CMOS design of the Serializer and Deserializer makes them inherently low power devices. In addition, the constant current source nature of the Bus LVDS outputs minimizes the slope of the speed vs. I_{CC} curve of conventional CMOS designs.

Powering Up the Deserializer

The DS92LV1212A can be powered up at any time by following the proper sequence. The REFCLK input can be running before the Deserializer powers up, and it must be running in order for the Deserializer to lock to incoming data. The Deserializer outputs will remain in TRI-STATE until the Deserializer detects data transmission at its inputs and locks to the incoming data stream.

Transmitting Data

Once you power up the Serializer and Deserializer, they must be phase locked to each other to transmit data. Phase locking occurs when the Deserializer locks to incoming data or when the Serializer sends patterns. The Serializer sends SYNC patterns whenever the SYNC1 or SYNC2 inputs are high. The $\overline{\text{LOCK}}$ output of the Deserializer remains high until it has locked to the incoming data stream. Connecting the $\overline{\text{LOCK}}$ output of the Deserializer to one of the SYNC inputs of the Serializer will guarantee that enough SYNC patterns are sent to achieve Deserializer lock.

The Deserializer can also lock to incoming data by simply powering up the device and allowing the “random lock” circuitry to find and lock to the data stream.

While the Deserializer $\overline{\text{LOCK}}$ output is low, data at the Deserializer outputs (ROUT0-9) is valid, except for the specific case of loss of lock during transmission which is further discussed in the 'Recovering from LOCK Loss' section below.

Noise Margin

The Deserializer noise margin is the amount of input jitter (phase noise) that the Deserializer can tolerate and still reliably receive data. Various environmental and systematic factors include:

Serializer: TCLK jitter, V_{CC} noise (noise bandwidth and out-of-band noise)

Media: ISI, Large V_{CM} shifts

Deserializer: V_{CC} noise

Recovering from LOCK Loss

In the case where the Deserializer loses lock during data transmission, up to 3 cycles of data that were previously received can be invalid. This is due to the delay in the lock detection circuit. The lock detect circuit requires that invalid clock information be received 4 times in a row to indicate loss of lock. Since clock information has been lost, it is possible that data was also lost during these cycles. Therefore, after the Deserializer relocks to the incoming data stream and the Deserializer $\overline{\text{LOCK}}$ pin goes low, at least three previous data cycles should be suspect for bit errors.

The Deserializer can relock to the incoming data stream by making the Serializer resend SYNC patterns, as described above, or by random locking, which can take more time, depending on the data patterns being received.

Hot Insertion

All the BLVDS devices are hot pluggable if you follow a few rules. When inserting, ensure the Ground pin(s) makes contact first, then the VCC pin(s), and then the I/O pins. When removing, the I/O pins should be unplugged first, then the VCC, then the Ground. Random lock hot insertion is illustrated in *Figure 10*.

PCB Considerations

The Bus LVDS Serializer and Deserializer should be placed as close to the edge connector as possible. In multiple Deserializer applications, the distance from the Deserializer to the slot connector appears as a stub to the Serializer driving the backplane traces. Longer stubs lower the impedance of the bus, increase the load on the Serializer, and lower the threshold margin at the Deserializers. Deserializer devices should be placed much less than one inch from slot connectors. Because transition times are very fast on the Serializer Bus LVDS outputs, reducing stub lengths as much as possible is the best method to ensure signal integrity.

Transmission Media

The Serializer and Deserializer can also be used in point-to-point configuration of a backplane, through a PCB trace, or through twisted pair cable. In point-to-point configuration, the transmission media need only be terminated at

Application Information (Continued)

the receiver end. Please note that in point-to-point configuration, the potential of offsetting the ground levels of the Serializer vs. the Deserializer must be considered. Also, Bus LVDS provides a +/− 1.2V common mode range at the receiver inputs.

Failsafe Biasing for the DS92LV1212A

The DS92LV1212A has an improved input threshold sensitivity of +/− 50mV versus +/− 100mV for the DS92LV1210 or DS92LV1212. This allows for greater differential noise margin in the DS92LV1212A. However, in cases where the receiver input is not being actively driven, the increased sensitivity of the DS92LV1212A can pickup noise as a signal and cause unintentional locking . For example, this can occur when the input cable is disconnected.

External resistors can be added to the receiver circuit board to prevent noise pick-up. Typically, the non-inverting receiver input is pulled up and the inverting receiver input is pulled down by high value resistors. the pull-up and pull-down resistors (R_1 and R_2) provide a current path through the termination resistor (R_L) which biases the receiver inputs when they are not connected to an active driver. The value of the pull-up and pull-down resistors should be chosen so that enough current is drawn to provide a +15mV drop across the termination resistor. Please see *Figure 11* for the Failsafe Biasing Setup.

Using t_{DJIT} and t_{RNM} to Validate Signal Quality

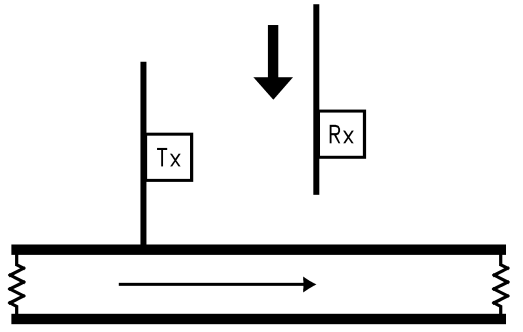
The parameters t_{DJIT} and t_{RNM} can be used to generate an eye pattern mask to validate signal quality in an actual application or in simulation.

The parameter t_{DJIT} measures the transmitter's ability to place data bits in the ideal position to be sampled by the receiver. The typical t_{DJIT} parameter of −80pS indicates that the crossing point of the Tx data is 80pS ahead of the ideal crossing point. The $t_{DJIT(min)}$ and $t_{DJIT(max)}$ parameters specify the earliest and latest, repectively, time that a crossing will occur relative to the ideal position.

The parameter t_{RNM} is calculated by first measuring how much of the ideal bit the receiver needs to ensure correct sampling. After determining this amount, what remains of the ideal bit that is available for external sources of noise is called t_{RNM}. It is the offset from $t_{DJIT(min\ or\ max)}$ for the test mask within the eye opening.

The vertical limits of the mask are determined by the DS92LV1212A receiver input threshold of +/− 50mV.

Please refer to the eye mask pattern of *Figure 12* for a graphic representation of t_{DJIT} and t_{RNM}.



The DS92LV1212A can be "Hot Inserted" into operating serial busses without interrupting bus communication. The random lock feature allows the DS92LV1212A to synchronize to the bus traffic and receive data.

FIGURE 10. Random Lock Allows Hot Insertion into Serial Busses

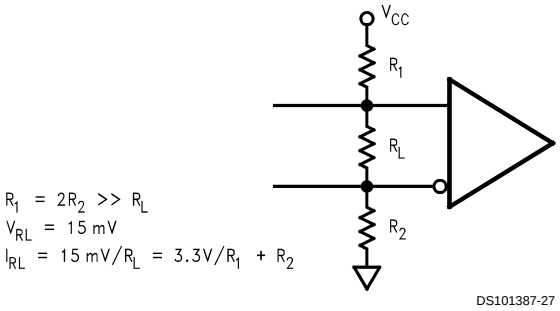
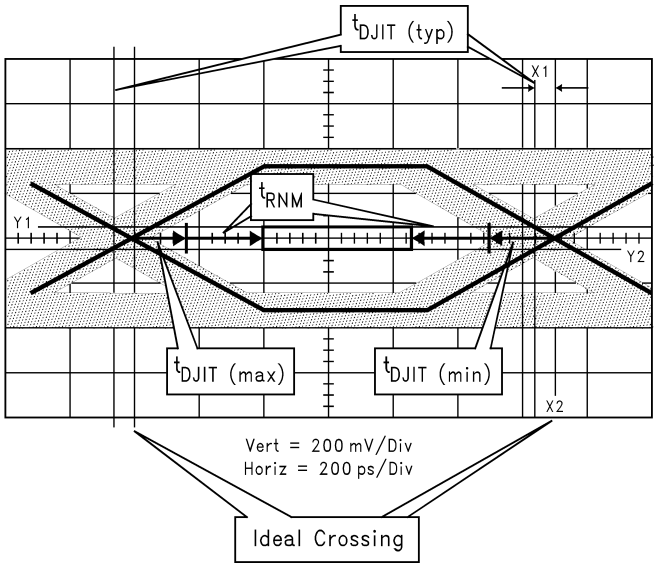


FIGURE 11. Failsafe Biasing Setup

Application Information (Continued)

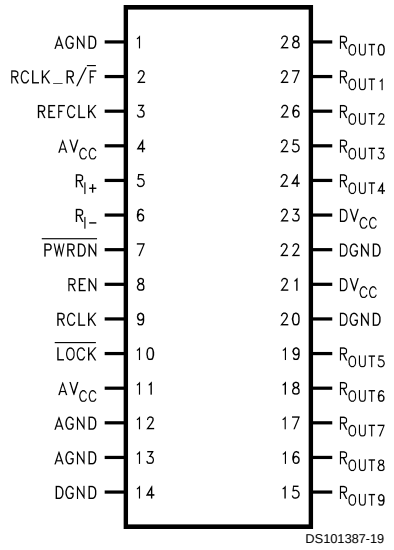


Note: For the DS92LV1021, t_{DJIT}(max) = 70pS and t_{DJIT}(min) = −300pS

FIGURE 12. Using t_{DJIT} and t_{RNM} to Generate an Eye Pattern Mask and Validate SIgnal Quality

Pin Diagram

DS92LV1212AMSA - Deserializer



DS101387-19

Deserializer Pin Description

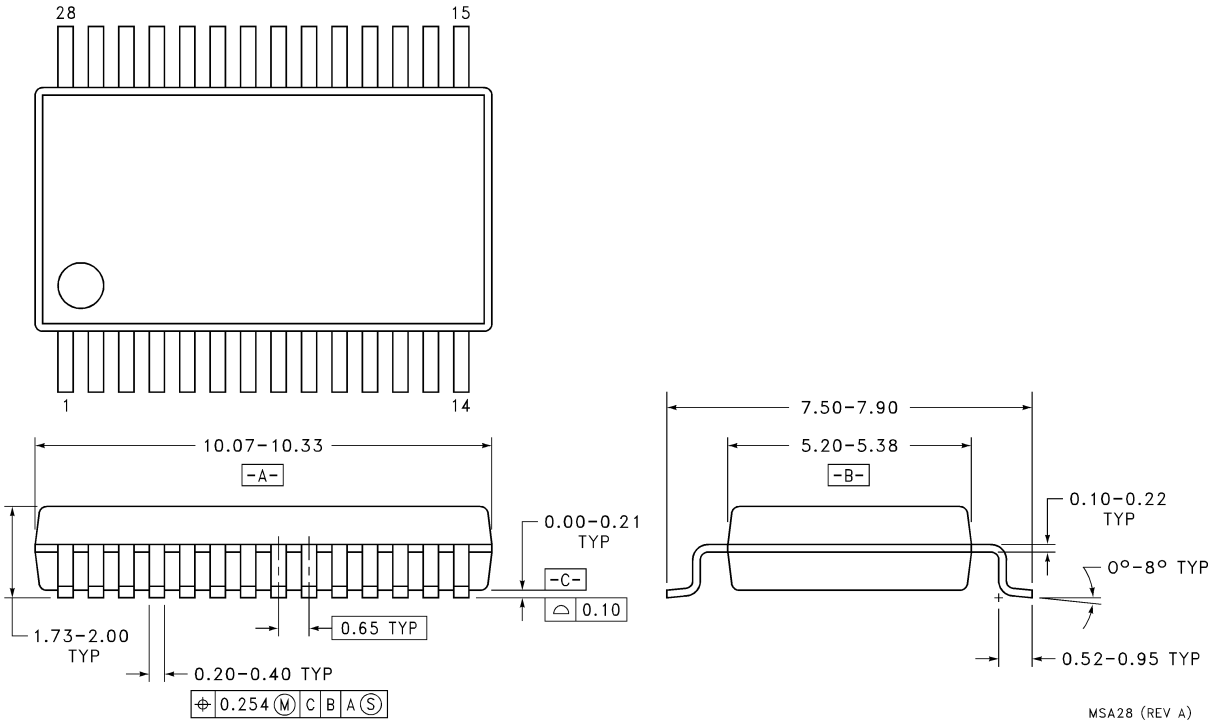
Pin Name	I/O	No.	Description
ROUT	O	15–19, 24–28	Data Output. ±9 mA CMOS level outputs.
RCLK_R/$\overline{F}$	I	2	Recovered Clock Rising/Falling strobe select. TTL level input. Selects RCLK active edge for strobing of ROUT data. High selects rising edge. Low selects falling edge.
RI+	I	5	+ Serial Data Input. Non-inverting Bus LVDS differential input.
RI−	I	6	− Serial Data Input. Inverting Bus LVDS differential input.
$\overline{PWRDN}$	I	7	Powerdown. TTL level input. $\overline{PWRDN}$ driven low shuts down the PLL.
$\overline{LOCK}$	O	10	$\overline{LOCK}$ goes low when the Deserializer PLL locks onto the embedded clock edge. CMOS level output. Totem pole output structure, does not directly support wire OR connection.
RCLK	O	9	Recovered Clock. Parallel data rate clock recovered from embedded clock. Used to strobe ROUT, CMOS level output.
REN	I	8	Output Enable. TTL level input. TRI-STATEs ROUT0–ROUT9, $\overline{LOCK}$ and RCLK when driven low.
DVCC	I	21, 23	Digital Circuit power supply.
DGND	I	14, 20, 22	Digital Circuit ground.
AVCC	I	4, 11	Analog power supply (PLL and Analog Circuits).
AGND	I	1, 12, 13	Analog ground (PLL and Analog Circuits).
REFCLK	I	3	Use this pin to supply a REFCLK signal for the internal PLL frequency.

Truth Table

INPUTS		OUTPUTS		
$\overline{\text{PWRDN}}$	REN	ROUT [0:9]	$\overline{\text{LOCK}}$	RCLK
H	H	Z	H	Z
H	H	Active	L	Active
L	X	Z	Z	Z
H	L	Z	Active	Z

1) $\overline{\text{LOCK}}$ Active indicates the $\overline{\text{LOCK}}$ output will reflect the state of the Deserializer with regard to the selected data stream.
2) RCLK Active indicates the RCLK will be running if the Deserializer is locked. The Timing of RCLK with respect to ROUT is determined by RCLK_R/$\overline{\text{F}}$.
3) ROUT and RCLK are TRI-STATED when $\overline{\text{LOCK}}$ is asserted High.

Physical Dimensions inches (millimeters) unless otherwise noted



Note: Package Dimensions are in millimeters only.
Order Number DS92LV1212AMSA
NS Package Number MSA28

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