

MC74HC245A

Octal 3-State Noninverting Bus Transceiver

High-Performance Silicon-Gate CMOS

The MC74HC245A is identical in pinout to the LS245. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

The HC245A is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

Features

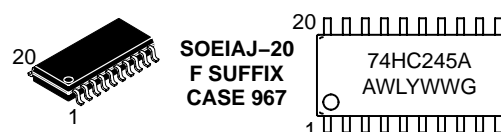
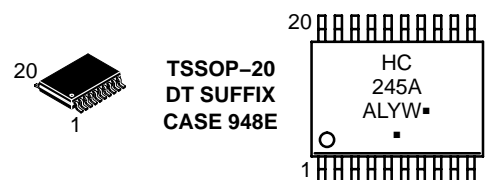
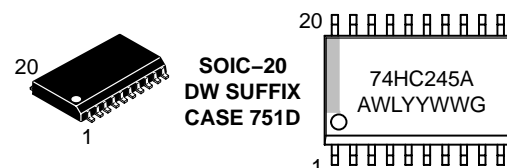
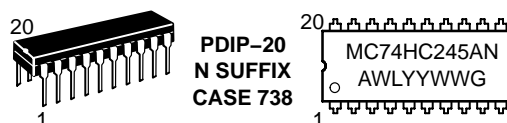
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Moisture Sensitivity: MSL1 for All Packages
- Chip Complexity: 308 FETs or 77 Equivalent Gates
- Pb-Free Packages are Available*



ON Semiconductor®

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MARKING DIAGRAMS



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package
▪ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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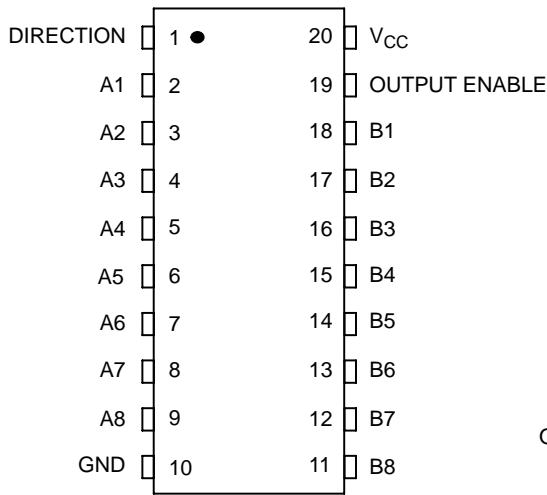


Figure 1. Pin Assignment

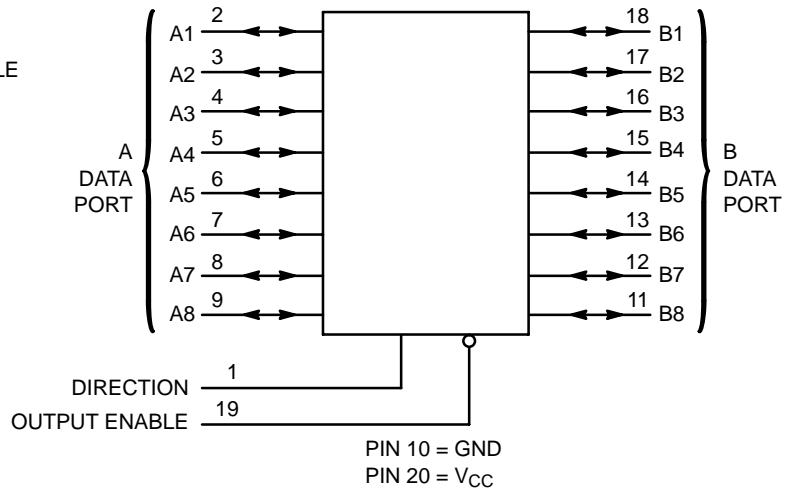


Figure 2. Logic Diagram

FUNCTION TABLE

| Control Inputs | | Operation |
|----------------|-----------|---------------------------------------|
| Output Enable | Direction | |
| L | L | Data Transmitted from Bus B to Bus A |
| L | H | Data Transmitted from Bus A to Bus B |
| H | X | Buses Isolated (High-Impedance State) |

X = don't care

ORDERING INFORMATION

| Device | Package | Shipping† |
|-----------------|---------------------------|------------------|
| MC74HC245AN | PDIP-20 | 18 Units / Rail |
| MC74HC245ANG | PDIP-20 (Pb-Free) | 18 Units / Rail |
| MC74HC245ADW | SOIC-20 WIDE | 38 Units / Rail |
| MC74HC245ADWG | SOIC-20 WIDE (Pb-Free) | 38 Units / Rail |
| MC74HC245ADWR2 | SOIC-20 WIDE | 1000 Tape & Reel |
| MC74HC245ADWR2G | SOIC-20 WIDE (Pb-Free) | 1000 Tape & Reel |
| MC74HC245ADT | TSSOP-20* | 75 Units / Rail |
| MC74HC245ADTG | TSSOP-20* | 75 Units / Rail |
| MC74HC245ADTR2 | TSSOP-20* | 2500 Tape & Reel |
| MC74HC245ADTR2G | TSSOP-20* | 2500 Tape & Reel |
| MC74HC245AF | SOEIAJ-20 | 40 Units / Rail |
| MC74HC245AFG | SOEIAJ-20 (Pb-Free) | 40 Units / Rail |
| MC74HC245AFEL | SOEIAJ-20 | 2000 Tape & Reel |
| MC74HC245AFELG | SOEIAJ-20 (Pb-Free) | 2000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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MAXIMUM RATINGS (Note 1)

| Symbol | Parameter | Value | Unit | |
|----------------------|---|--|---------------------------|------|
| V _{CC} | DC Supply Voltage | -0.5 to +7.0 | V | |
| V _{IN} | DC Input Voltage | -0.5 to V _{CC} +0.5 | V | |
| V _{OUT} | DC Output Voltage (Note 2) | -0.5 to V _{CC} +0.5 | V | |
| I _{IK} | DC Input Diode Current | ±20 | mA | |
| I _{OK} | DC Output Diode Current | ±35 | mA | |
| I _{OUT} | DC Output Sink Current | ±35 | mA | |
| I _{CC} | DC Supply Current per Supply Pin | ±75 | mA | |
| I _{GND} | DC Ground Current per Ground Pin | ±75 | mA | |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C | |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | °C | |
| T _J | Junction Temperature Under Bias | +150 | °C | |
| θ _{JA} | Thermal Resistance | PDIP SOIC TSSOP | 67 96 128 | °C/W |
| P _D | Power Dissipation in Still Air at 85°C | PDIP SOIC TSSOP | 750 500 450 | mW |
| MSL | Moisture Sensitivity | Level 1 | | |
| F _R | Flammability Rating | Oxygen Index: 30% to 35% | UL 94 V-0 @ 0.125 in | |
| V _{ESD} | ESD Withstand Voltage | Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5) | > 2000 > 200 > 1000 | V |
| I _{LATCHUP} | Latchup Performance | Above V _{CC} and Below GND at 85°C (Note 6) | ±300 | mA |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 20 ounce copper trace with no air flow.
2. I_O absolute maximum rating must be observed.
3. Tested to EIA/JESD22-A114-A.
4. Tested to EIA/JESD22-A115-A.
5. Tested to JESD22-C101-A.
6. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------------------------------|--|-------------------------|-----------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| V _{in} , V _{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V _{CC} | V |
| T _A | Operating Temperature, All Package Types | -55 | +125 | °C |
| t _r , t _f | Input Rise and Fall Time (Figure 3) | | | ns |
| | | V _{CC} = 2.0 V | 0 | 1000 |
| | | V _{CC} = 4.5 V | 0 | 500 |
| | | V _{CC} = 6.0 V | 0 | 400 |

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|--|---|----------------------|------------------|--------|---------|------|
| | | | | -55 to 25°C | ≤ 85°C | ≤ 125°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{out} = V _{CC} - 0.1 V I _{out} ≤ 20 μA | 2.0 | 1.5 | 1.5 | 1.5 | V |
| | | | 3.0 | 2.1 | 2.1 | 2.1 | |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.2 | 4.2 | 4.2 | |
| V _{IL} | Maximum Low-Level Input Voltage | V _{out} = 0.1 V I _{out} ≤ 20 μA | 2.0 | 0.5 | 0.5 | 0.5 | V |
| | | | 3.0 | 0.9 | 0.9 | 0.9 | |
| | | | 4.5 | 1.35 | 1.35 | 1.35 | |
| | | | 6.0 | 1.8 | 1.8 | 1.8 | |
| V _{OH} | Minimum High-Level Output Voltage | V _{in} = V _{IH} I _{out} ≤ 20 μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | V _{in} = V _{IH} I _{out} ≤ 2.4 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA | 3.0 | 2.48 | 2.34 | 2.2 | |
| | | | 4.5 | 3.98 | 3.84 | 3.7 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{in} = V _{IL} I _{out} ≤ 20 μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | V _{in} = V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA | 3.0 | 0.26 | 0.33 | 0.4 | |
| | | | 4.5 | 0.26 | 0.33 | 0.4 | |
| 6.0 | 0.26 | 0.33 | 0.4 | | | | |
| I _{in} | Maximum Input Leakage Current | V _{in} = V _{CC} or GND | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| I _{oZ} | Maximum Three-State Leakage Current | Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND | 6.0 | ± 0.5 | ± 5.0 | ± 10 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND I _{out} = 0 μA | 6.0 | 4.0 | 40 | 160 | μA |

7. Information on typical parametric values and high frequency or heavy load considerations can be found in the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|--|---|----------------------|------------------|--------|---------|------|
| | | | -55 to 25°C | ≤ 85°C | ≤ 125°C | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, A to B, B to A (Figures 1 and 3) | 2.0 | 75 | 95 | 110 | ns |
| | | 3.0 | 55 | 70 | 80 | |
| | | 4.5 | 15 | 19 | 22 | |
| | | 6.0 | 13 | 16 | 19 | |
| t _{PLZ} , t _{PHZ} | Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4) | 2.0 | 110 | 140 | 165 | ns |
| | | 3.0 | 90 | 110 | 130 | |
| | | 4.5 | 22 | 28 | 33 | |
| | | 6.0 | 19 | 24 | 28 | |
| t _{PZL} , t _{PZH} | Maximum Propagation Delay, Output Enable to A or B (Figures 2 and 4) | 2.0 | 110 | 140 | 165 | ns |
| | | 3.0 | 90 | 110 | 130 | |
| | | 4.5 | 22 | 28 | 33 | |
| | | 6.0 | 19 | 24 | 28 | |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figures 1 and 3) | 2.0 | 60 | 75 | 90 | ns |
| | | 3.0 | 23 | 27 | 32 | |
| | | 4.5 | 12 | 15 | 18 | |
| | | 6.0 | 10 | 13 | 15 | |
| C _{in} | Maximum Input Capacitance (Pin 1 or Pin 19) | - | 10 | 10 | 10 | pF |
| C _{out} | Maximum Three-State I/O Capacitance (I/O in High-Impedance State) | - | 15 | 15 | 15 | pF |

8. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

| C _{PD} | Power Dissipation Capacitance (Per Transceiver Channel) (Note 9) | Typical @ 25°C, V _{CC} = 5.0 V | |
|-----------------|--|---|----|
| | | 40 | pF |
| | | | |

9. Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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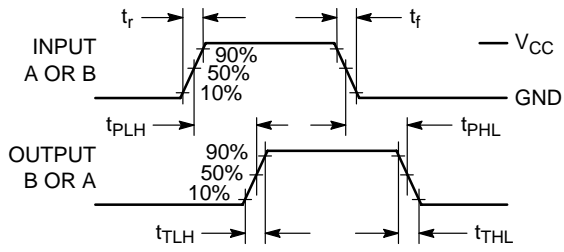


Figure 3. Switching Waveform

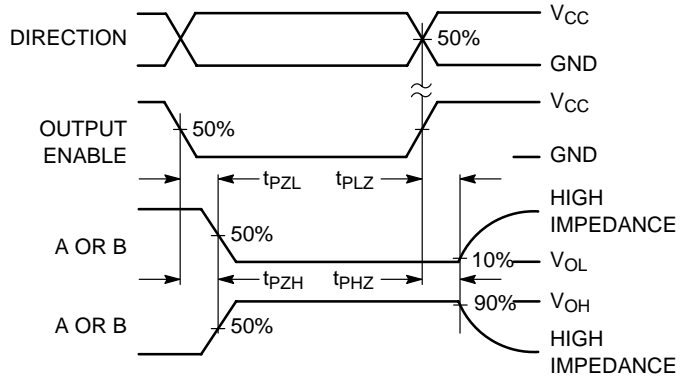
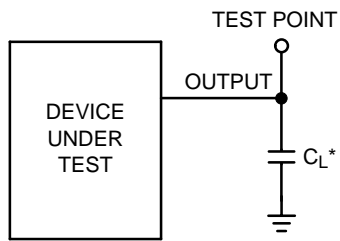
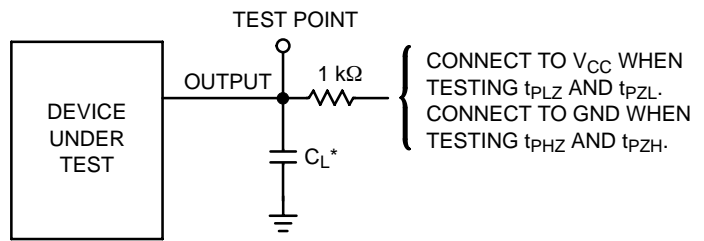


Figure 4. Switching Waveform



*Includes all probe and jig capacitance

Figure 5. Test Circuit



*Includes all probe and jig capacitance

Figure 6. Test Circuit

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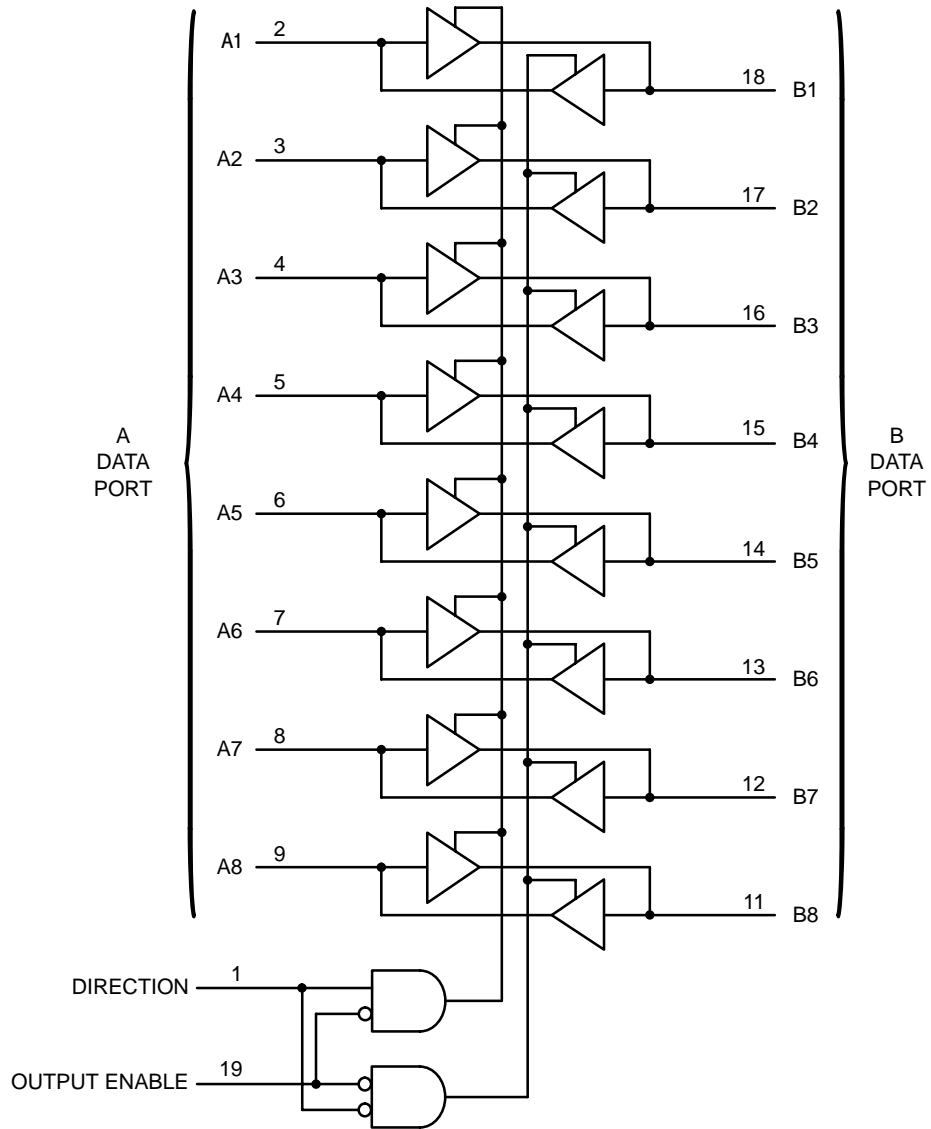
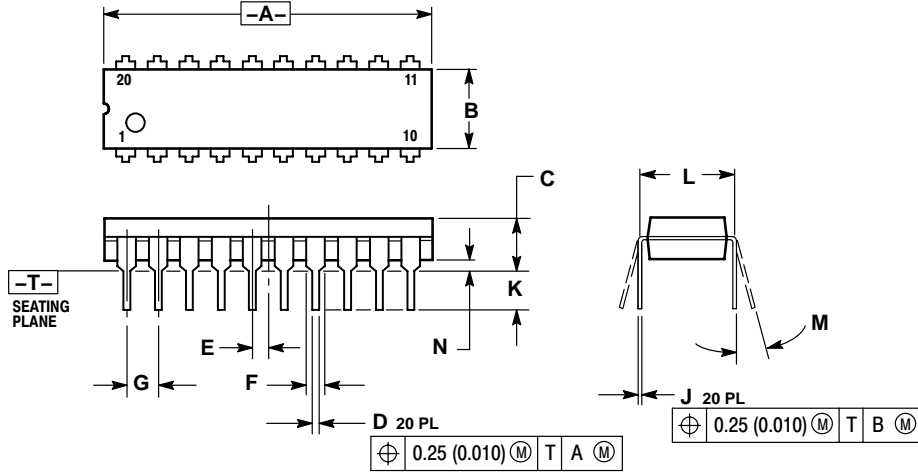


Figure 7. Expanded Logic Diagram

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PACKAGE DIMENSIONS

PDIP-20
N SUFFIX
PLASTIC DIP PACKAGE
CASE 738-03
ISSUE E

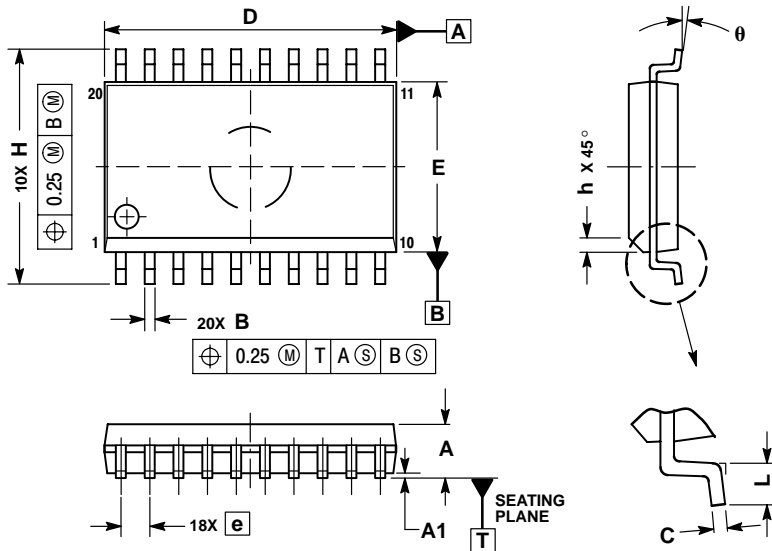


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.010 | 1.070 | 25.66 | 27.17 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.150 | 0.180 | 3.81 | 4.57 |
| D | 0.015 | 0.022 | 0.39 | 0.55 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.050 | 0.070 | 1.27 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.140 | 2.80 | 3.55 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° 15° | | 0° 15° | |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

SOIC-20
DW SUFFIX
CASE 751D-05
ISSUE G



NOTES:

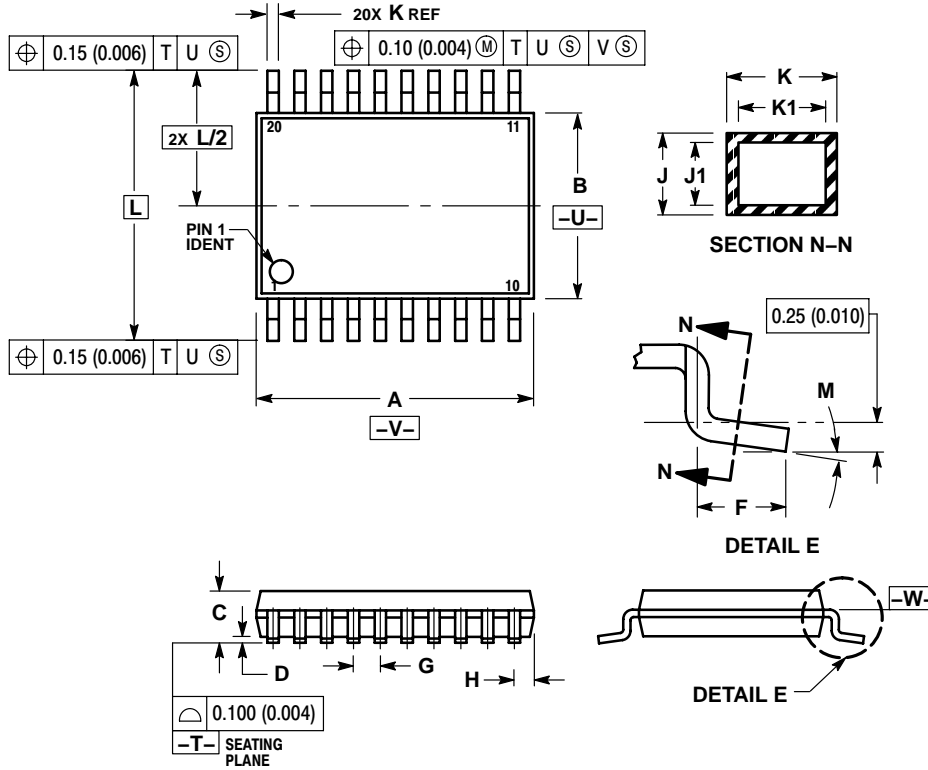
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|----------|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° 7° | |

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PACKAGE DIMENSIONS

TSSOP-20
DT SUFFIX
CASE 948E-02
ISSUE B



NOTES:

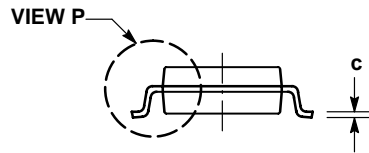
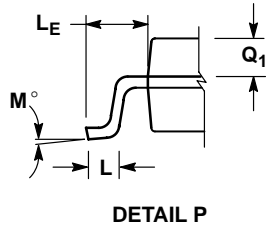
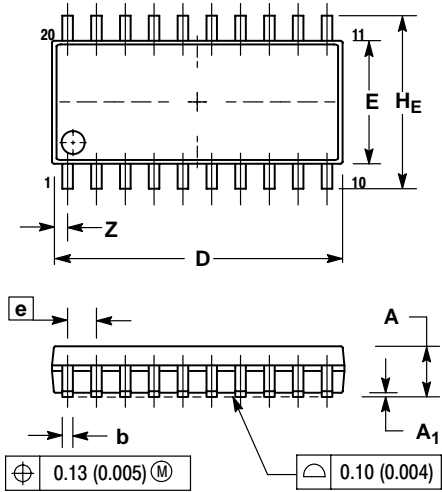
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

MC74HC245A

PACKAGE DIMENSIONS

SOEIAJ-20
F SUFFIX
CASE 967-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| A ₁ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.18 | 0.27 | 0.007 | 0.011 |
| D | 12.35 | 12.80 | 0.486 | 0.504 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| HE | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| LE | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0° | 10° | 0° | 10° |
| Q ₁ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.81 | --- | 0.032 |

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