

- Low Supply-Voltage Range, 1.8 V to 3.6 V
- Ultralow-Power Consumption:
  - Active Mode: 350  $\mu$ A at 1 MHz, 2.2 V
  - Standby Mode: 1.1  $\mu$ A
  - Off Mode (RAM Retention): 0.3  $\mu$ A
- Five Power Saving Modes
- Wake-Up From Standby Mode in less than 6  $\mu$ s
- 16-Bit RISC Architecture, Extended Memory, 125-ns Instruction Cycle Time
- Three Channel Internal DMA
- 12-Bit A/D Converter With Internal Reference, Sample-and-Hold and Autoscans Feature
- Three Configurable Operational Amplifiers
- Dual 12-Bit D/A Converters With Synchronization
- 16-Bit Timer\_A With Three Capture/Compare Registers
- 16-Bit Timer\_B With Seven Capture/Compare-With-Shadow Registers
- On-Chip Comparator
- Supply Voltage Supervisor/Monitor With Programmable Level Detection
- Serial Communication Interface (USART1), Select Asynchronous UART or Synchronous SPI by Software
- Universal Serial Communication Interface
  - Enhanced UART supporting auto-baudrate detection
  - IrDA Encoder and Decoder
  - Synchronous SPI
  - I2C™
- Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse
- Brownout Detector
- Basic Timer with Real Time Clock Feature
- Integrated LCD Driver up to 160 Segments With Regulated Charge Pump
- Family Members Include:
  - MSP430FG4616: 92KB+256B Flash Memory, 4KB RAM
  - MSP430FG4617: 92KB+256B Flash Memory, 8KB RAM
  - MSP430FG4618: 116KB+256B Flash Memory, 8KB RAM
  - MSP430FG4619: 120KB+256B Flash Memory, 4KB RAM
- For Complete Module Descriptions, Refer to the *MSP430x4xx Family User's Guide*

## description

The Texas Instruments MSP430 family of ultralow power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that attribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6 $\mu$ s.

The MSP430FG461x series are microcontroller configurations with two 16-bit timers, a high performance 12-bit A/D converter, dual 12-bit D/A converters, three configurable operational amplifiers, one universal serial communication interface (USCI), one universal synchronous/asynchronous communication interface (USART), DMA, 80 I/O pins, and a liquid crystal display (LCD) driver with regulated charge pump.

Typical applications for this device include analog and digital sensor systems, digital motor control, remote controls, thermostats, digital timers, hand-held meters, etc.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGED DEVICES
	PLASTIC 100-PIN TQFP (PZ)
-40°C to 85°C	MSP430FG4616IPZ
	MSP430FG4617IPZ
	MSP430FG4618IPZ
	MSP430FG4619IPZ

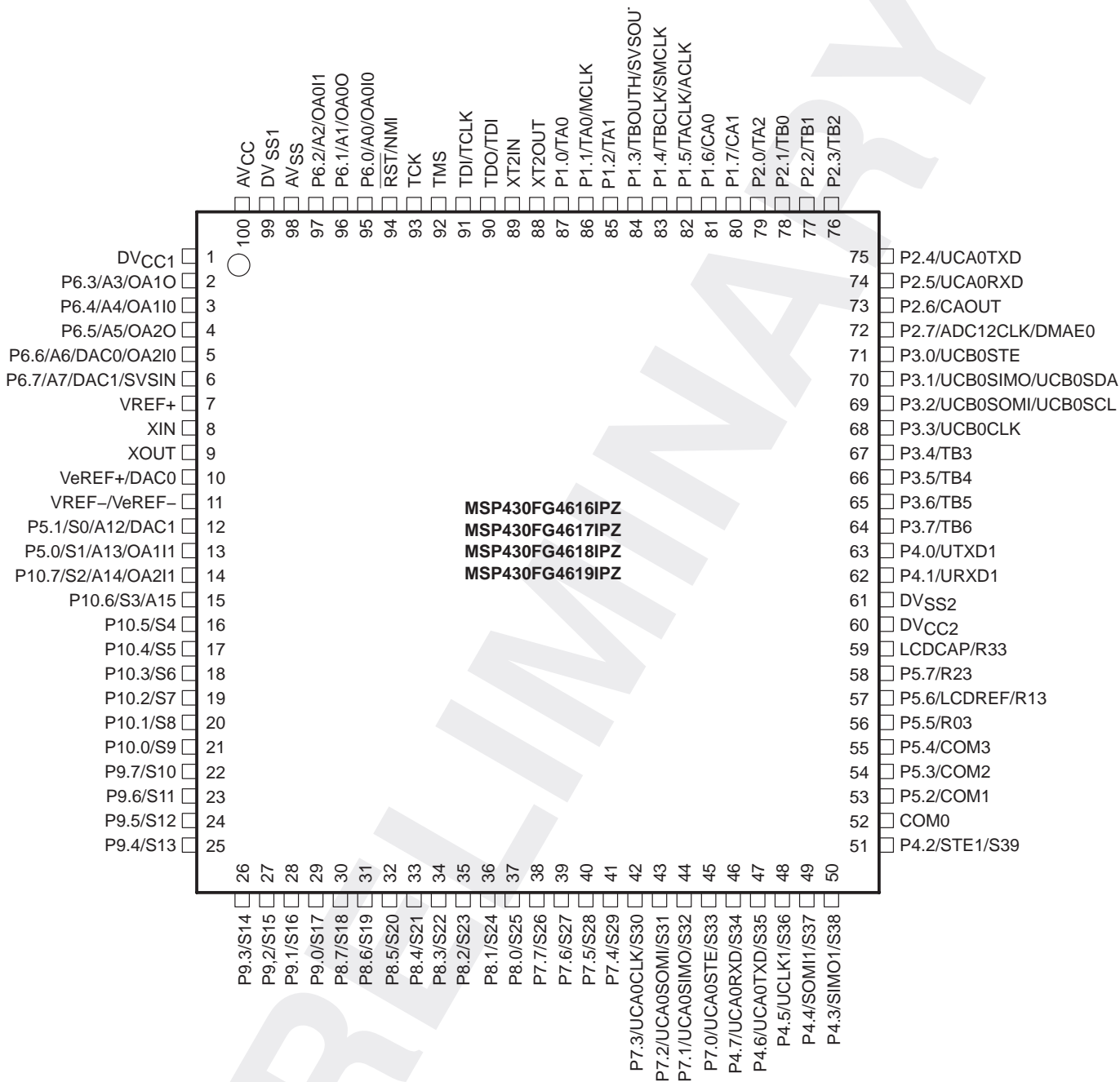
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PRELIMINARY



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**pin designation, MSP430FG461xIPZ**

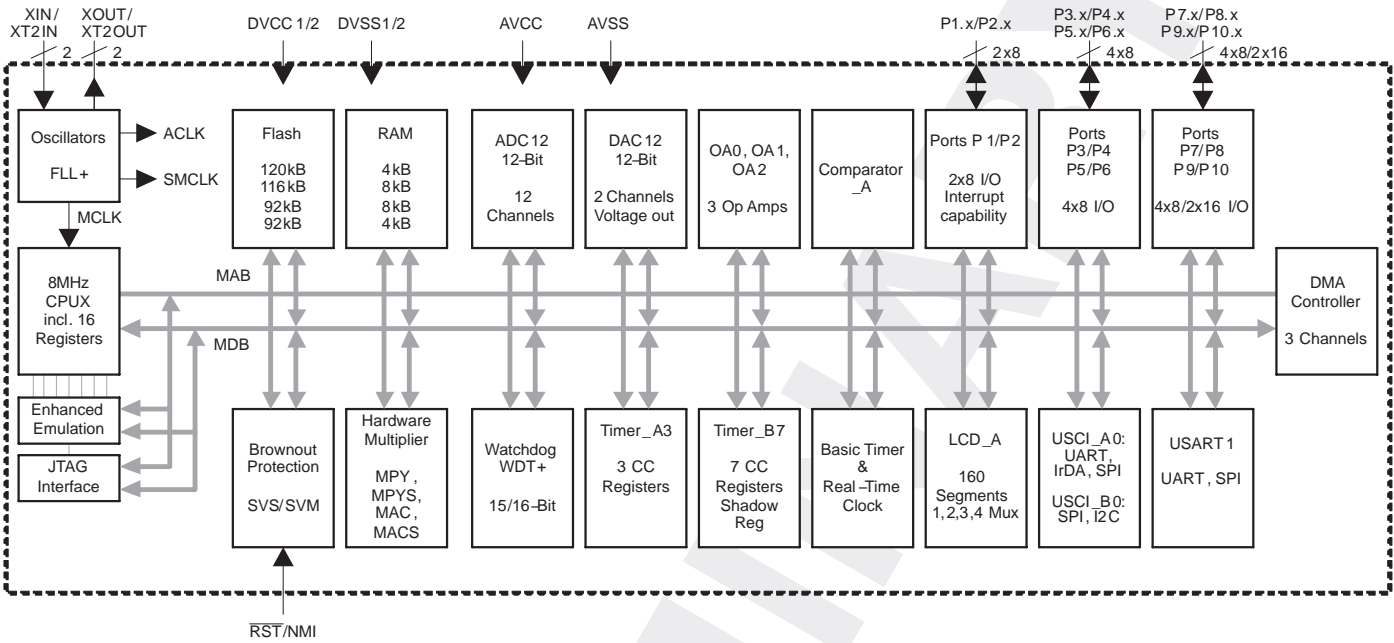


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# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## MSP430FG461x functional block diagram



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PRELIMINARY

**MSP430FG461x Terminal Functions**

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DV <sub>CC1</sub>	1		Digital supply voltage, positive terminal.
P6.3/A3/OA1O	2	I/O	General-purpose digital I/O / analog input a3—12-bit ADC / OA1 output
P6.4/A4/OA1I0	3	I/O	General-purpose digital I/O / analog input a4—12-bit ADC / OA1 input multiplexer on +terminal and –terminal
P6.5/A5/OA2O	4	I/O	General-purpose digital I/O / analog input a5—12-bit ADC / OA2 output
P6.6/A6/DAC0/OA2I0	5	I/O	General-purpose digital I/O / analog input a6—12-bit ADC / DAC12.0 output / OA2 input multiplexer on +terminal and –terminal
P6.7/A7/DAC1/SVSIN	6	I/O	General-purpose digital I/O / analog input a7—12-bit ADC / DAC12.1 output / analog input to brownout, supply voltage supervisor
V <sub>REF+</sub>	7	O	Output of positive terminal of the reference voltage in the ADC
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	O	Output terminal of crystal oscillator XT1
V <sub>REF+</sub> /DAC0	10	I/O	Input for an external reference voltage to the ADC / DAC12.0 output
V <sub>REF-</sub> /V <sub>REF-</sub>	11	I	Negative terminal for the ADC's reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
P5.1/S0/A12/DAC1 (see Note 1)	12	I/O	General-purpose digital I/O / LCD segment output 0 / analog input a12 – 12-bit ADC / DAC12.1 output
P5.0/S1/A13/OA1I1 (see Note 1)	13	I/O	General-purpose digital I/O / LCD segment output 1 / analog input a13 – 12-bit ADC/OA1 input multiplexer on +terminal and –terminal
P10.7/S2/A14/OA2I1 (see Note 1)	14	I/O	General-purpose digital I/O / LCD segment output 2 / analog input a14 – 12-bit ADC/OA2 input multiplexer on +terminal and –terminal
P10.6/S3/A15 (see Note 1)	15	I/O	General-purpose digital I/O / LCD segment output 3 / analog input a15 – 12-bit ADC
P10.5/S4	16	I/O	General-purpose digital I/O / LCD segment output 4
P10.4/S5	17	I/O	General-purpose digital I/O / LCD segment output 5
P10.3/S6	18	I/O	General-purpose digital I/O / LCD segment output 6
P10.2/S7	19	I/O	General-purpose digital I/O / LCD segment output 7
P10.1/S8	20	I/O	General-purpose digital I/O / LCD segment output 8
P10.0/S9	21	I/O	General-purpose digital I/O / LCD segment output 9
P9.7/S10	22	I/O	General-purpose digital I/O / LCD segment output 10
P9.6/S11	23	I/O	General-purpose digital I/O / LCD segment output 11
P9.5/S12	24	I/O	General-purpose digital I/O / LCD segment output 12
P9.4/S13	25	I/O	General-purpose digital I/O / LCD segment output 13
P9.3/S14	26	I/O	General-purpose digital I/O / LCD segment output 14
P9.2/S15	27	I/O	General-purpose digital I/O / LCD segment output 15
P9.1/S16	28	I/O	General-purpose digital I/O / LCD segment output 16
P9.0/S17	29	I/O	General-purpose digital I/O / LCD segment output 17
P8.7/S18	30	I/O	General-purpose digital I/O / LCD segment output 18
P8.6/S19	31	I/O	General-purpose digital I/O / LCD segment output 19
P8.5/S20	32	I/O	General-purpose digital I/O / LCD segment output 20
P8.4/S21	33	I/O	General-purpose digital I/O / LCD segment output 21
P8.3/S22	34	I/O	General-purpose digital I/O / LCD segment output 22

NOTES: 1. Segments S0 through S3 must be disabled and cannot be used when the LCD charge pump feature is enabled. In addition, when using segments S0 through S3 with an external LCD voltage supply,  $V_{LCD} \leq AV_{CC}$ .

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## MSP430FG461x Terminal Functions (Continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
P8.2/S23	35	I/O	General-purpose digital I/O / LCD segment output 23
P8.1/S24	36	I/O	General-purpose digital I/O / LCD segment output 24
P8.0/S25	37	I/O	General-purpose digital I/O / LCD segment output 25
P7.7/S26	38	I/O	General-purpose digital I/O / LCD segment output 26
P7.6/S27	39	I/O	General-purpose digital I/O / LCD segment output 27
P7.5/S28	40	I/O	General-purpose digital I/O / LCD segment output 28
P7.4/S29	41	I/O	General-purpose digital I/O / LCD segment output 29
P7.3/UCA0CLK/S30	42	I/O	General-purpose digital I/O / external clock input—USCI_A0/UART or SPI mode, clock output—USART1/SPI MODE / LCD segment output 30
P7.2/UCA0SOMI/S31	43	I/O	General-purpose digital I/O / slave out/master in of USCI_A0/SPI mode / LCD segment output 31
P7.1/UCA0SIMO/S32	44	I/O	General-purpose digital I/O / slave in/master out of USCI_A0/SPI mode / LCD segment output 32
P7.0/UCA0STE/S33	45	I/O	General-purpose digital I/O / slave transmit enable—USCI_A0/SPI mode / LCD segment output 33
P4.7/UCA0RXD/S34	46	I/O	General-purpose digital I/O / receive data in – USCI_A0/UART or IrDA mode / LCD segment output 34
P4.6/UCA0TXD/S35	47	I/O	General-purpose digital I/O / transmit data in – USCI_A0/UART or IrDA mode / LCD segment output 35
P4.5/UCLK1/S36	48	I/O	General-purpose digital I/O / external clock input—USART1/UART or SPI mode, clock output—USART1/SPI MODE / LCD segment output 36
P4.4/SOMI1/S37	49	I/O	General-purpose digital I/O / slave out/master in of USART1/SPI mode / LCD segment output 37
P4.3/SIMO1/S38	50	I/O	General-purpose digital I/O / slave in/master out of USART1/SPI mode / LCD segment output 38
P4.2/STE1/S39	51	I/O	General-purpose digital I/O / slave transmit enable—USART1/SPI mode / LCD segment output 39
COM0	52	O	COM0–3 are used for LCD backplanes.
P5.2/COM1	53	I/O	General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes.
P5.3/COM2	54	I/O	General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes.
P5.4/COM3	55	I/O	General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes.
P5.5/R03	56	I/O	General-purpose digital I/O / Input port of lowest analog LCD level (V5)
P5.6/LCDREF/R13	57	I/O	General-purpose digital I/O / External reference voltage input for regulated LCD voltage / Input port of third most positive analog LCD level (V4 or V3)
P5.7/R23	58	I/O	General-purpose digital I/O / Input port of second most positive analog LCD level (V2)
LDCAP/R33	59	I	LCD Capacitor connection / Input/output port of most positive analog LCD level (V1)
DV <sub>CC2</sub>	60		Digital supply voltage, positive terminal.
DV <sub>SS2</sub>	61		Digital supply voltage, negative terminal.
P4.1/URXD1	62	I/O	General-purpose digital I/O / receive data in—USART1/UART mode
P4.0/UTXD1	63	I/O	General-purpose digital I/O / transmit data out—USART1/UART mode
P3.7/TB6	64	I/O	General-purpose digital I/O / Timer_B7 CCR6. Capture: CCI6A/CCI6B input, compare: Out6 output
P3.6/TB5	65	I/O	General-purpose digital I/O / Timer_B7 CCR5. Capture: CCI5A/CCI5B input, compare: Out5 output
P3.5/TB4	66	I/O	General-purpose digital I/O / Timer_B7 CCR4. Capture: CCI4A/CCI4B input, compare: Out4 output

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**MSP430FG461x Terminal Functions (Continued)**

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
P3.4/TB3	67	I/O	General-purpose digital I/O / Timer_B7 CCR3. Capture: CCI3A/CCI3B input, compare: Out3 output
P3.3/UCB0CLK	68	I/O	General-purpose digital I/O / external clock input—USCI_B0/UART or SPI mode, clock output—USCI_B0/SPI mode
P3.2/UCB0SOMI/ UCB0SCL	69	I/O	General-purpose digital I/O / slave out/master in of USCI_B0/SPI mode /I2C clock USCI_B0/I2C mode
P3.1/UCB0SIMO/ UCB0SDA	70	I/O	General-purpose digital I/O / slave in/master out of USCI_B0/SPI mode, I2C data – USCI_B0/I2C mode
P3.0/UCB0STE	71	I/O	General-purpose digital I/O / slave transmit enable—USCI_B0/SPI mode
P2.7/ADC12CLK/ DMAE0	72	I/O	General-purpose digital I/O / conversion clock—12-bit ADC / DMA Channel 0 external trigger
P2.6/CAOUT	73	I/O	General-purpose digital I/O / Comparator_A output
P2.5/UCA0RXD	74	I/O	General-purpose digital I/O / receive data in—USCI_A0/UART or IrDA mode
P2.4/UCA0TXD	75	I/O	General-purpose digital I/O / transmit data out—USCI_A0/UART or IrDA mode
P2.3/TB2	76	I/O	General-purpose digital I/O / Timer_B7 CCR2. Capture: CCI2A/CCI2B input, compare: Out2 output
P2.2/TB1	77	I/O	General-purpose digital I/O / Timer_B7 CCR1. Capture: CCI1A/CCI1B input, compare: Out1 output
P2.1/TB0	78	I/O	General-purpose digital I/O / Timer_B7 CCR0. Capture: CCI0A/CCI0B input, compare: Out0 output
P2.0/TA2	79	I/O	General-purpose digital I/O / Timer_A Capture: CCI2A input, compare: Out2 output
P1.7/CA1	80	I/O	General-purpose digital I/O / Comparator_A input
P1.6/CA0	81	I/O	General-purpose digital I/O / Comparator_A input
P1.5/TACLK/ACLK	82	I/O	General-purpose digital I/O / Timer_A, clock signal TACLK input / ACLK output (divided by 1, 2, 4, or 8)
P1.4/TBCLK/SMCLK	83	I/O	General-purpose digital I/O / input clock TBCLK—Timer_B7 / submain system clock SMCLK output
P1.3/TBOUTH/SVSOUT	84	I/O	General-purpose digital I/O / switch all PWM digital output ports to high impedance—Timer_B7 TB0 to TB6 / SVS: output of SVS comparator
P1.2/TA1	85	I/O	General-purpose digital I/O / Timer_A, Capture: CCI1A input, compare: Out1 output
P1.1/TA0/MCLK	86	I/O	General-purpose digital I/O / Timer_A. Capture: CCI0B input / MCLK output. Note: TA0 is only an input on this pin / BSL receive
P1.0/TA0	87	I/O	General-purpose digital I/O / Timer_A. Capture: CCI0A input, compare: Out0 output / BSL transmit
XT2OUT	88	O	Output terminal of crystal oscillator XT2
XT2IN	89	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
TDO/TDI	90	I/O	Test data output port. TDO/TDI data output or programming data input terminal
TDI/TCLK	91	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TMS	92	I	Test mode select. TMS is used as an input port for device programming and test.
TCK	93	I	Test clock. TCK is the clock input port for device programming and test.
RST/NMI	94	I	Reset input or nonmaskable interrupt input port
P6.0/A0/OA0I0	95	I/O	General-purpose digital I/O / analog input a0 – 12-bit ADC / OA0 input multiplexer on +terminal and – terminal
P6.1/A1/OA0O	96	I/O	General-purpose digital I/O / analog input a1 – 12-bit ADC / OA0 output
P6.2/A2/OA0I1	97	I/O	General-purpose digital I/O / analog input a2 – 12-bit ADC / OA0 input multiplexer on + terminal and – terminal
AVSS	98		Analog supply voltage, negative terminal. Supplies SVS, brownout, oscillator, FLL+, comparator_A, port 1
DVSS1	99		Digital supply voltage, negative terminal.
AVCC	100		Analog supply voltage, positive terminal. Supplies SVS, brownout, oscillator, FLL+, comparator_A, port 1; must not power up prior to DVCC1/DVCC2.

# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## short-form description

### CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The MSP430FG461x device family utilizes the MSP430X CPU and is completely backwards compatible with the MSP430 CPU. For a complete description of the MSP430X CPU, refer to the *MSP430x4xx Family User's Guide*.

### instruction set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Program Counter	PC/R0
Stack Pointer	SP/R1
Status Register	SR/CG1/R2
Constant Generator	CG2/R3
General-Purpose Register	R4
General-Purpose Register	R5
General-Purpose Register	R6
General-Purpose Register	R7
General-Purpose Register	R8
General-Purpose Register	R9
General-Purpose Register	R10
General-Purpose Register	R11
General-Purpose Register	R12
General-Purpose Register	R13
General-Purpose Register	R14
General-Purpose Register	R15

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**Table 1. Instruction Word Formats**

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 ----> R5
Single operands, destination only	e.g. CALL R8	PC -->(TOS), R8--> PC
Relative jump, un/conditional	e.g. JNE	Jump-on-equal bit = 0

**Table 2. Address Mode Descriptions**

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)→ M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	●	●	MOV & MEM, & TCDAT		M(MEM) → M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2 → R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

NOTE: S = source    D = destination

# MSP430FG461x

## MIXED SIGNAL MICROCONTROLLER

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### operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode AM;
  - All clocks are active
- Low-power mode 0 (LPM0);
  - CPU is disabled  
ACLK and SMCLK remain active. MCLK is disabled  
FLL+ Loop control remains active
- Low-power mode 1 (LPM1);
  - CPU is disabled  
FLL+ Loop control is disabled  
ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 2 (LPM2);
  - CPU is disabled  
MCLK and FLL+ loop control and DCOCLK are disabled  
DCO's dc-generator remains enabled  
ACLK remains active
- Low-power mode 3 (LPM3);
  - CPU is disabled  
MCLK, FLL+ loop control, and DCOCLK are disabled  
DCO's dc-generator is disabled  
ACLK remains active
- Low-power mode 4 (LPM4);
  - CPU is disabled  
ACLK is disabled  
MCLK, FLL+ loop control, and DCOCLK are disabled  
DCO's dc-generator is disabled  
Crystal oscillator is stopped

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**interrupt vector addresses**

The interrupt vectors and the power-up start address are located in the address range 0FFFFh – 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

**Table 3. Interrupt Sources, Flags, and Vectors of MSP430FG461x Configurations**

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Flash Memory	WDTIFG KEYV (see Note 1)	Reset	0FFFEh	31, highest
NMI Oscillator Fault Flash Memory Access Violation	NMIIFG (see Notes 1 and 3) OFIFG (see Notes 1 and 3) ACCVIFG (see Notes 1 and 3)	(Non)maskable (Non)maskable (Non)maskable	0FFFCh	30
Timer_B7	TBCCR0 CCIFG0 (see Note 2)	Maskable	0FFFAh	29
Timer_B7	TBCCR1 CCIFG1 ... TBCCR6 CCIFG6, TBIFG (see Notes 1 and 2)	Maskable	0FFF8h	28
Comparator_A	CAIFG	Maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	Maskable	0FFF4h	26
USCI_A0/USCI_B0 Receive	UCA0RXIFG, UCB0RXIFG (see Notes 1)	Maskable	0FFF2h	25
USCI_A0/USCI_B0 Transmit	UCA0TXIFG, UCB0TXIFG (see Notes 1)	Maskable	0FFF0h	24
ADC12	ADC12IFG (see Notes 1 and 2)	Maskable	0FFEEh	23
Timer_A3	TACCR0 CCIFG0 (see Note 2)	Maskable	0FFECCh	22
Timer_A3	TACCR1 CCIFG1 and TACCR2 CCIFG2, TAIFG (see Notes 1 and 2)	Maskable	0FFEAh	21
I/O Port P1 (Eight Flags)	P1IFG.0 to P1IFG.7 (see Notes 1 and 2)	Maskable	0FFE8h	20
USART1 receive	URXIFG1	Maskable	0FFE6h	19
USART1 transmit	UTXIFG1	Maskable	0FFE4h	18
I/O Port P2 (Eight Flags)	P2IFG.0 to P2IFG.7 (see Notes 1 and 2)	Maskable	0FFE2h	17
Basic Timer1/RTC	BTIFG	Maskable	0FFE0h	16
DMA	DMA0IFG, DMA1IFG, DMA2IFG (see Notes 1 and 2)	Maskable	0FFDEh	15
DAC12	DAC12.0IFG, DAC12.1IFG (see Notes 1 and 2)	Maskable	0FFDCh	14
Reserved	Reserved (see Note 4)		0FFDAh	13
			...	...
			0FFC0h	0, lowest

- NOTES: 1. Multiple source flags  
 2. Interrupt flags are located in the module.  
 3. A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h–01FFh).  
 . (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.  
 4. The interrupt vectors at addresses 0FFDAh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

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# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## special function registers

The MSP430 special function registers(SFR) are located in the lowest address space, and are organized as byte mode registers. SFRs should be accessed with byte instructions.

### interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE Watchdog-timer interrupt enable. Inactive if watchdog mode is selected.  
Active if watchdog timer is configured as a general-purpose timer.

OFIE Oscillator-fault-interrupt enable

NMIIE Nonmaskable-interrupt enable

ACCVIE Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h	BTIE		UTXIE1	URXIE1	UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
	rw-0		rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

UCA0RXIE USCI\_A0 receive-interrupt enable

UCA0TXIE USCI\_A0 transmit-interrupt enable

UCB0RXIE USCI\_B0 receive-interrupt enable

UCB0TXIE USCI\_B0 transmit-interrupt enable

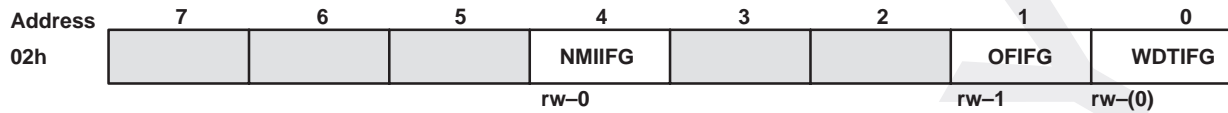
URXIE1 USART1 UART and SPI receive-interrupt enable

UTXIE1 USART1 UART and SPI transmit-interrupt enable

BTIE Basic timer interrupt enable

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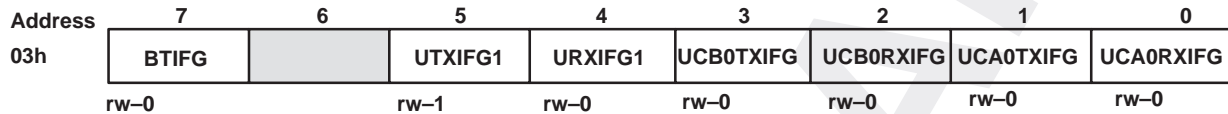
interrupt flag register 1 and 2



WDTIFG: Set on watchdog timer overflow (in watchdog mode) or security key violation  
Reset on V<sub>CC</sub> power-on or a reset condition at the  $\overline{\text{RST}}$ /NMI pin in reset mode

OFIFG: Flag set on oscillator fault

NMIIFG: Set via  $\overline{\text{RST}}$ /NMI pin



UCA0RXIFG USCI\_A0 receive-interrupt flag

UCA0TXIFG USCI\_A0 transmit-interrupt flag

UCB0RXIFG USCI\_B0 receive-interrupt flag

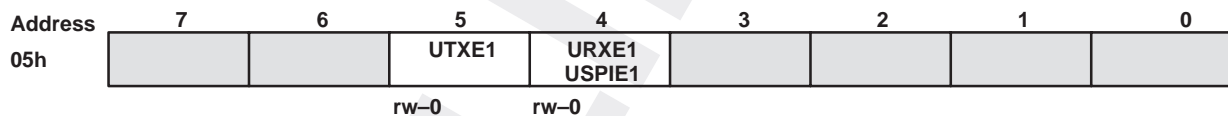
UCB0TXIFG USCI\_B0 transmit-interrupt flag

URXIFG0: USART1: UART and SPI receive flag

UTXIFG0: USART1: UART and SPI transmit flag

BTIFG: Basic timer flag


module enable registers 1 and 2



URXE1: USART1: UART mode receive enable

UTXE1: USART1: UART mode transmit enable

USPIE1: USART1: SPI mode transmit and receive enable

**Legend** rw: Bit can be read and written.  
 rw-0,1: Bit can be read and written. It is Reset or Set by PUC.  
 rw-(0,1): Bit can be read and written. It is Reset or Set by POR.  
 SFR bit is not present in device

# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## memory organization

		MSP430FG4616	MSP430FG4617	MSP430FG4618	MSP430FG4619
Memory Main: interrupt vector Main: code memory	Size	92KB	92KB	116KB	120KB
	Flash Flash	0FFFFh – 0FFC0h 018FFFh – 002100h	0FFFFh – 0FFC0h 019FFFh – 003100h	0FFFFh – 0FFC0h 01FFFFh – 003100h	0FFFFh – 0FFC0h 01FFFFh – 002100h
RAM (Total)	Size	4KB	8KB	8KB	4KB
	Extended	020FFh – 01100h	030FFh – 01100h	030FFh – 01100h	020FFh – 01100h
	Mirrored	Size 2KB 020FFh – 01900h	Size 6KB 030FFh – 01900h	Size 6KB 030FFh – 01900h	Size 2KB 020FFh – 01900h
Information memory	Size	256 Byte	256 Byte	256 Byte	256 Byte
	Flash	010FFh – 01000h	010FFh – 01000h	010FFh – 01000h	010FFh – 01000h
Boot memory	Size ROM	1KB 0FFFh – 0C00h	1KB 0FFFh – 0C00h	1KB 0FFFh – 0C00h	1KB 0FFFh – 0C00h
RAM (mirrored at 018FFh – 01100h)	Size	2KB 09FFh – 0200h	2KB 09FFh – 0200h	2KB 09FFh – 0200h	2KB 09FFh – 0200h
Peripherals	16-bit	01FFh – 0100h	01FFh – 0100h	01FFh – 0100h	01FFh – 0100h
	8-bit	0FFh – 010h	0FFh – 010h	0FFh – 010h	0FFh – 010h
	8-bit SFR	0Fh – 00h	0Fh – 00h	0Fh – 00h	0Fh – 00h

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## bootstrap loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. A bootstrap loader security key is provided at address 0FFBEh to disable the BSL completely or to disable the erasure of the flash if an invalid password is supplied. For complete description of the features of the BSL and its implementation, see the Application report *Features of the MSP430 Bootstrap Loader*, Literature Number SLAA089.

BSLKEY	Description
00000h	Erase of flash disabled if an invalid password is supplied
0AA55h	BSL disabled
any other value	BSL enabled

BSL Function	PZ Package Pins
Data Transmit	87 – P1.0
Data Receive	86 – P1.1

## flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0–n. Segments A and B are also called *information memory*.
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.



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## peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430x4xx Family User's Guide*.

## DMA controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12 conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode without having to awaken to move data to or from a peripheral.

## oscillator and system clock

The clock system in the MSP430FG461x family of devices is supported by the FLL+ module that includes support for a 32768 Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high frequency crystal oscillator. The FLL+ clock module is designed to meet the requirements of both low system cost and low-power consumption. The FLL+ features digital frequency locked loop (FLL) hardware which in conjunction with a digital modulator stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6  $\mu$ s. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768 Hz watch crystal or a high frequency crystal.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8.

## brownout, supply voltage supervisor

The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The supply voltage supervisor (SVS) circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However,  $V_{CC}$  may not have ramped to  $V_{CC(min)}$  at that time. The user must insure the default FLL+ settings are not changed until  $V_{CC}$  reaches  $V_{CC(min)}$ . If desired, the SVS circuit can be used to determine when  $V_{CC}$  reaches  $V_{CC(min)}$ .

## digital I/O

There are ten 8-bit I/O ports implemented—ports P1 through P10:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Ports P7/P8 and P9/P10 can be accessed word-wise as ports PA and PB respectively.

## Basic Timer1 and Real-Time Clock

The Basic Timer1 has two independent 8-bit timers which can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. The Basic Timer1 is extended to provide an integrated Real-Time Clock (RTC). An internal calendar compensates for months with less than 31 days and includes leap year correction.

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## **LCD\_A drive with regulated charge pump**

The LCD\_A driver generates the segment and common signals required to drive an LCD display. The LCD\_A controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral. The module can provide a LCD voltage independent of the supply voltage with its integrated charge pump. Furthermore it is possible to control the level of the LCD voltage and thus contrast by software.

## **WDT+ watchdog timer**

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

## **USCI**

The universal serial communication interface (USCI) modules are used for serial data communication. The USCI module supports synchronous communication protocols like SPI (3 or 4 pin), I2C and asynchronous communication protocols like UART, enhanced UART with automatic baudrate detection, and IrDA.

The USCI\_A0 module provides support for SPI (3 or 4 pin), UART, enhanced UART and IrDA.

The USCI\_B0 module provides support for SPI (3 or 4 pin) and I2C.

## **USART1**

The hardware universal synchronous/asynchronous receive transmit (USART) peripheral module is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels.

## **hardware multiplier**

The multiplication operation is supported by a dedicated peripheral module. The module performs  $16 \times 16$ ,  $16 \times 8$ ,  $8 \times 16$ , and  $8 \times 8$  bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

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## timer\_A3

Timer\_A3 is a 16-bit timer/counter with three capture/compare registers. Timer\_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer\_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_A3 Signal Connections					
Input Pin Number	Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number
PZ					PZ
82 - P1.5	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
82 - P1.5	$\overline{\text{TACLK}}$	INCLK			
87 - P1.0	TA0	CCI0A	CCR0	TA0	87 - P1.0
86 - P1.1	TA0	CCI0B			
	DVSS	GND			
	DVCC	VCC			
85 - P1.2	TA1	CCI1A	CCR1	TA1	85 - P1.2
	CAOUT (internal)	CCI1B			ADC12 (internal)
	DVSS	GND			
	DVCC	VCC			
79 - P2.0	TA2	CCI2A	CCR2	TA2	79 - P2.0
	ACLK (internal)	CCI2B			
	DVSS	GND			
	DVCC	VCC			

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**timer\_B7**

Timer\_B7 is a 16-bit timer/counter with seven capture/compare registers. Timer\_B7 can support multiple capture/compares, PWM outputs, and interval timing. Timer\_B7 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_B7 Signal Connections					
Input Pin Number	Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number
PZ					PZ
83 - P1.4	TBCLK	TBCLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
83 - P1.4	$\overline{\text{TBCLK}}$	INCLK			
78 - P2.1	TB0	CCI0A	CCR0	TB0	78 - P2.1
78 - P2.1	TB0	CCI0B			ADC12 (internal)
	DVSS	GND			
	DVCC	VCC			
77 - P2.2	TB1	CCI1A	CCR1	TB1	77 - P2.2
77 - P2.2	TB1	CCI1B			ADC12 (internal)
	DVSS	GND			
	DVCC	VCC			
76 - P2.3	TB2	CCI2A	CCR2	TB2	76 - P2.3
76 - P2.3	TB2	CCI2B			
	DVSS	GND			
	DVCC	VCC			
67 - P3.4	TB3	CCI3A	CCR3	TB3	67 - P3.4
67 - P3.4	TB3	CCI3B			
	DVSS	GND			
	DVCC	VCC			
66 - P3.5	TB4	CCI4A	CCR4	TB4	66 - P3.5
66 - P3.5	TB4	CCI4B			
	DVSS	GND			
	DVCC	VCC			
65 - P3.6	TB5	CCI5A	CCR5	TB5	65 - P3.6
65 - P3.6	TB5	CCI5B			
	DVSS	GND			
	DVCC	VCC			
64 - P3.7	TB6	CCI6A	CCR6	TB6	64 - P3.7
	ACLK (internal)	CCI6B			
	DVSS	GND			
	DVCC	VCC			

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## comparator\_A

The primary function of the comparator\_A module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

## ADC12

The ADC12 module supports fast, 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator and a 16 word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

## DAC12

The DAC12 module is a 12-bit, R-ladder, voltage output DAC. The DAC12 may be used in 8- or 12-bit mode, and may be used in conjunction with the DMA controller. When multiple DAC12 modules are present, they may be grouped together for synchronous operation.

## OA

The MSP430FG461x has three configurable low-current general-purpose operational amplifiers. Each OA input and output terminal is software-selectable and offer a flexible choice of connections for various applications. The OA op amps primarily support front-end analog signal conditioning prior to analog-to-digital conversion.

OA Signal Connections						
Input Pin Number	Device Input Signal	Module Input Name	Module Block	Module Output Signal	Device Output Signal	Output Pin Number
PZ						PZ
95 - P6.0	OA0I0	OA0I0	OA0	OA0OUT	OA0O	96 - P6.1
97 - P6.2	OA0I1	OA0I1			OA0O	ADC12 (internal)
	DAC12_0OUT (internal)	DAC12_0OUT				
	DAC12_1OUT (internal)	DAC12_1OUT				
3 - P6.4	OA1I0	OA1I0	OA1	OA1OUT	OA1O	2 - P6.3
13 - P5.0	OA1I1	OA1I1			OA1O	13- P5.0
	DAC12_0OUT (internal)	DAC12_0OUT			OA1O	ADC12 (internal)
	DAC12_1OUT (internal)	DAC12_1OUT				
5 - P6.6	OA2I0	OA2I0	OA2	OA2OUT	OA2O	4 - P6.5
14- P10.7	OA2I1	OA2I1			OA2O	14- P10.7
	DAC12_0OUT (internal)	DAC12_0OUT			OA2O	ADC12 (internal)
	DAC12_1OUT (internal)	DAC12_1OUT				

peripheral file map

PERIPHERALS WITH WORD ACCESS			
<b>Watchdog+</b>	Watchdog timer control	WDTCTL	0120h
<b>Timer_B7</b>	Capture/compare register 6	TBCCR6	019Eh
	Capture/compare register 5	TBCCR5	019Ch
	Capture/compare register 4	TBCCR4	019Ah
	Capture/compare register 3	TBCCR3	0198h
	Capture/compare register 2	TBCCR2	0196h
	Capture/compare register 1	TBCCR1	0194h
	Capture/compare register 0	TBCCR0	0192h
	Timer_B register	TBR	0190h
	Capture/compare control 6	TBCCTL6	018Eh
	Capture/compare control 5	TBCCTL5	018Ch
	Capture/compare control 4	TBCCTL4	018Ah
	Capture/compare control 3	TBCCTL3	0188h
	Capture/compare control 2	TBCCTL2	0186h
	Capture/compare control 1	TBCCTL1	0184h
	Capture/compare control 0	TBCCTL0	0182h
	Timer_B control	TBCTL	0180h
	Timer_B interrupt vector	TBIV	011Eh
<b>Timer_A3</b>	Capture/compare register 2	TACCR2	0176h
	Capture/compare register 1	TACCR1	0174h
	Capture/compare register 0	TACCR0	0172h
	Timer_A register	TAR	0170h
	Capture/compare control 2	TACCTL2	0166h
	Capture/compare control 1	TACCTL1	0164h
	Capture/compare control 0	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
<b>Hardware Multiplier</b>	Sum extend	SUMEXT	013Eh
	Result high word	RESHI	013Ch
	Result low word	RESLO	013Ah
	Second operand	OP2	0138h
	Multiply signed + accumulate/operand1	MACS	0136h
	Multiply + accumulate/operand1	MAC	0134h
	Multiply signed/operand1	MPYS	0132h
	Multiply unsigned/operand1	MPY	0130h
<b>Flash</b>	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h

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## peripheral file map (continued)

PERIPHERALS WITH WORD ACCESS (CONTINUED)			
<b>DMA</b>	DMA module control 0	DMACTL0	0122h
	DMA module control 1	DMACTL1	0124h
	DMA interrupt vector	DMAIV	0126h
<b>DMA Channel 0</b>	DMA channel 0 control	DMA0CTL	01D0h
	DMA channel 0 source address	DMA0SA	01D2h
	DMA channel 0 destination address	DMA0DA	01D6h
	DMA channel 0 transfer size	DMA0SZ	01DAh
<b>DMA Channel 1</b>	DMA channel 1 control	DMA1CTL	01DCh
	DMA channel 1 source address	DMA1SA	01DEh
	DMA channel 1 destination address	DMA1DA	01E2h
	DMA channel 1 transfer size	DMA1SZ	01E6h
<b>DMA Channel 2</b>	DMA channel 2 control	DMA2CTL	01E8h
	DMA channel 2 source address	DMA2SA	01EAh
	DMA channel 2 destination address	DMA2DA	01EEh
	DMA channel 2 transfer size	DMA2SZ	01F2h

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peripheral file map (continued)

PERIPHERALS WITH WORD ACCESS (CONTINUED)			
<b>ADC12</b> <i>See also Peripherals with Byte Access</i>	Conversion memory 15	ADC12MEM15	015Eh
	Conversion memory 14	ADC12MEM14	015Ch
	Conversion memory 13	ADC12MEM13	015Ah
	Conversion memory 12	ADC12MEM12	0158h
	Conversion memory 11	ADC12MEM11	0156h
	Conversion memory 10	ADC12MEM10	0154h
	Conversion memory 9	ADC12MEM9	0152h
	Conversion memory 8	ADC12MEM8	0150h
	Conversion memory 7	ADC12MEM7	014Eh
	Conversion memory 6	ADC12MEM6	014Ch
	Conversion memory 5	ADC12MEM5	014Ah
	Conversion memory 4	ADC12MEM4	0148h
	Conversion memory 3	ADC12MEM3	0146h
	Conversion memory 2	ADC12MEM2	0144h
	Conversion memory 1	ADC12MEM1	0142h
	Conversion memory 0	ADC12MEM0	0140h
	Interrupt-vector-word register	ADC12IV	01A8h
	Inerrupt-enable register	ADC12IE	01A6h
	Inerrupt-flag register	ADC12IFG	01A4h
	Control register 1	ADC12CTL1	01A2h
Control register 0	ADC12CTL0	01A0h	
<b>DAC12</b>	DAC12_1 data	DAC12_1DAT	01CAh
	DAC12_1 control	DAC12_1CTL	01C2h
	DAC12_0 data	DAC12_0DAT	01C8h
	DAC12_0 control	DAC12_0CTL	01C0h
<b>Port PA</b>	Port PA selection	PASEL	03Eh
	Port PA direction	PADIR	03Ch
	Port PA output	PAOUT	03Ah
	Port PA input	PAIN	038h
<b>Port PB</b>	Port PB selection	PBSEL	00Eh
	Port PB direction	PBDIR	00Ch
	Port PB output	PBOUT	00Ah
	Port PB input	PBIN	008h

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## peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS			
<b>OA2</b>	Operational Amplifier 2 control register 1	OA2CTL1	0C5h
	Operational Amplifier 2 control register 0	OA2CTL0	0C4h
<b>OA1</b>	Operational Amplifier 1 control register 1	OA1CTL1	0C3h
	Operational Amplifier 1 control register 0	OA1CTL0	0C2h
<b>OA0</b>	Operational Amplifier 0 control register 1	OA0CTL1	0C1h
	Operational Amplifier 0 control register 0	OA0CTL0	0C0h
<b>LCD_A</b>	LCD Voltage Control 1	LCDVAVCTL1	0AFh
	LCD Voltage Control 0	LCDVAVCTL0	0AEh
	LCD Voltage Port Control 1	LCDVAPCTL1	0ADh
	LCD Voltage Port Control 0	LCDVAPCTL0	0ACh
	LCD memory 20	LCDM20	0A4h
	:	:	:
	LCD memory 16	LCDM16	0A0h
	LCD memory 15	LCDM15	09Fh
	:	:	:
	LCD memory 1	LCDM1	091h
LCD control and mode	LCDCTL	090h	
<b>ADC12</b> (Memory control registers require byte access)	ADC memory-control register 15	ADC12MCTL15	08Fh
	ADC memory-control register 14	ADC12MCTL14	08Eh
	ADC memory-control register 13	ADC12MCTL13	08Dh
	ADC memory-control register 12	ADC12MCTL12	08Ch
	ADC memory-control register 11	ADC12MCTL11	08Bh
	ADC memory-control register 10	ADC12MCTL10	08Ah
	ADC memory-control register 9	ADC12MCTL9	089h
	ADC memory-control register 8	ADC12MCTL8	088h
	ADC memory-control register 7	ADC12MCTL7	087h
	ADC memory-control register 6	ADC12MCTL6	086h
	ADC memory-control register 5	ADC12MCTL5	085h
	ADC memory-control register 4	ADC12MCTL4	084h
	ADC memory-control register 3	ADC12MCTL3	083h
	ADC memory-control register 2	ADC12MCTL2	082h
	ADC memory-control register 1	ADC12MCTL1	081h
	ADC memory-control register 0	ADC12MCTL0	080h
<b>USART1</b>	Transmit buffer	U1TXBUF	07Fh
	Receive buffer	U1RXBUF	07Eh
	Baud rate	U1BR1	07Dh
	Baud rate	U1BR0	07Ch
	Modulation control	U1MCTL	07Bh
	Receive control	U1RCTL	07Ah
	Transmit control	U1TCTL	079h
	USART control	U1CTL	078h

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**peripheral file map (continued)**

<b>PERIPHERALS WITH BYTE ACCESS (CONTINUED)</b>			
<b>USCI</b>	USCI I2C Slave Address	UCBSA	011Ah
	USCI I2C Own Address	UCBOA	0118h
	USCI Synchronous Transmit Buffer	UCBTXBUF	06Fh
	USCI Synchronous Receive Buffer	UCBRXBUF	06Eh
	USCI Synchronous Status	UCBSTAT	06Dh
	USCI Synchronous Bit Rate 1	UCBBR1	06Bh
	USCI Synchronous Bit Rate 0	UCBBR0	06Ah
	USCI Synchronous Control 1	UCBCTL1	069h
	USCI Synchronous Control 0	UCBCTL0	068h
	USCI Transmit Buffer	UCATXBUF	067h
	USCI Receive Buffer	UCARXBUF	066h
	USCI Status	UCASTAT	065h
	USCI Modulation Control	UCAMCTL	064h
	USCI Baud Rate 1	UCABR1	063h
	USCI Baud Rate 0	UCABR0	062h
	USCI Control 1	UCACTL1	061h
	USCI Control 0	UCACTL0	060h
	USCI IrDA Receive Control	UCAIRRCTL	05Fh
	USCI IrDA Transmit Control	UCAIRTCTL	05Eh
	USCI LIN Control	UCAABCTL	05Dh
<b>Comparator_A</b>	Comparator_A port disable	CAPD	05Bh
	Comparator_A control 2	CACTL2	05Ah
	Comparator_A control 1	CACTL1	059h
<b>BrownOUT, SVS</b>	SVS control register (Reset by brownout signal)	SVSCTL	056h
<b>FLL+Clock</b>	FLL+ Control 1	FLL_CTL1	054h
	FLL+ Control 0	FLL_CTL0	053h
	System clock frequency control	SCFQCTL	052h
	System clock frequency integrator	SCFI1	051h
	System clock frequency integrator	SCFI0	050h
<b>RTC (Basic Timer 1)</b>	Real Time Clock Year High Byte	RTCYEARH	04Fh
	Real Time Clock Year Low Byte	RTCYEARL	04Eh
	Real Time Clock Month	RTCMON	04Dh
	Real Time Clock Day of Month	RTCDAAY	04Ch
	Basic Timer1 Counter 2	BTCNT2	047h
	Basic Timer1 Counter 1	BTCNT1	046h
	Real Time Counter 4	RTCNT4	045h
	(Real Time Clock Day of Week)	(RTCDOW)	
	Real Time Counter 3	RTCNT3	044h
	(Real Time Clock Hour)	(RTCHOUR)	
	Real Time Counter 2	RTCNT2	043h
	(Real Time Clock Minute)	(RTCMIN)	
	Real Time Counter 1	RTCNT1	042h
	(Real Time Clock Second)	(RTCSEC)	
	Real Time Clock Control	RTCCTL	041h
Basic Timer1 Control	BTCTL	040h	

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## peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
<b>Port P10</b>	Port P10 selection	P10SEL	00Fh
	Port P10 direction	P10DIR	00Dh
	Port P10 output	P10OUT	00Bh
	Port P10 input	P10IN	009h
<b>Port P9</b>	Port P9 selection	P9SEL	00Eh
	Port P9 direction	P9DIR	00Ch
	Port P9 output	P9OUT	00Ah
	Port P9 input	P9IN	008h
<b>Port P8</b>	Port P8 selection	P8SEL	03Fh
	Port P8 direction	P8DIR	03Dh
	Port P8 output	P8OUT	03Bh
	Port P8 input	P8IN	039h
<b>Port P7</b>	Port P7 selection	P7SEL	03Eh
	Port P7 direction	P7DIR	03Ch
	Port P7 output	P7OUT	03Ah
	Port P7 input	P7IN	038h
<b>Port P6</b>	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
<b>Port P5</b>	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
<b>Port P4</b>	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
<b>Port P3</b>	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
<b>Port P2</b>	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
<b>Port P1</b>	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h

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peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
Special functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

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# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage applied at $V_{CC}$ to $V_{SS}$ .....	-0.3 V to 4.1 V
Voltage applied to any pin (see Note) .....	-0.3 V to $V_{CC} + 0.3$ V
Diode current at any device terminal .....	$\pm 2$ mA
Storage temperature, $T_{stg}$ : (unprogrammed device) .....	-55°C to 150°C
(programmed device) .....	-40°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to  $V_{SS}$ . The JTAG fuse-blow voltage,  $V_{FB}$ , is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

## recommended operating conditions

		MIN	NOM	MAX	UNITS
Supply voltage during program execution, $V_{CC}$ ( $AV_{CC} = DV_{CC1/2} = V_{CC}$ )		1.8		3.6	V
Supply voltage during flash memory programming, $V_{CC}$ ( $AV_{CC} = DV_{CC1/2} = V_{CC}$ )		2.7		3.6	V
Supply voltage during program execution, SVS enabled and PORON = 1 (see Note 1), $V_{CC}$ ( $AV_{CC} = DV_{CC1/2} = V_{CC}$ )		2		3.6	V
Supply voltage, $V_{SS}$ ( $AV_{SS} = DV_{SS1/2} = V_{SS}$ )		0		0	V
Operating free-air temperature range, $T_A$		-40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Note 2)	LF selected, XTS_FLL=0 Watch crystal		32.768		kHz
	XT1 selected, XTS_FLL=1 Ceramic resonator	450		8000	kHz
	XT1 selected, XTS_FLL=1 Crystal	1000		8000	kHz
XT2 crystal frequency, $f_{(XT2)}$	Ceramic resonator	450		8000	kHz
	Crystal	1000		8000	
Processor frequency (signal MCLK), $f_{(System)}$	$V_{CC} = 1.8$ V	DC		3.0	MHz
	$V_{CC} = 2.0$ V	DC		4.6	
	$V_{CC} = 3.6$ V	DC		8.0	

- NOTES: 1. The minimum operating supply voltage is defined according to the trip point where POR is going active by decreasing the supply voltage. POR is going inactive when the supply voltage is raised above the minimum supply voltage plus the hysteresis of the SVS circuitry.  
2. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.

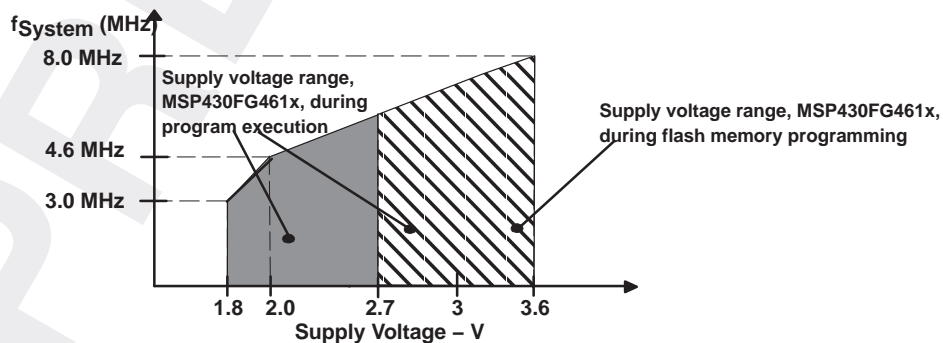


Figure 1. Frequency vs Supply Voltage, typical characteristic

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

supply current into AV<sub>CC</sub> + DV<sub>CC</sub> excluding external current

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
I <sub>(AM)</sub>	Active mode, (see Note 1 and Note 4) f <sub>(MCLK)</sub> = f <sub>(SMCLK)</sub> = 1 MHz, f <sub>(ACLK)</sub> = 32,768 Hz XTS=0, SELM=(0,1)	T <sub>A</sub> = -40°C to 85°C	V <sub>CC</sub> = 2.2 V	350	450		μA
			V <sub>CC</sub> = 3 V	550	700		
I <sub>(LPM0)</sub>	Low-power mode, (LPM0) (see Note 1 and Note 4)	T <sub>A</sub> = -40°C to 85°C	V <sub>CC</sub> = 2.2 V	55	70		μA
			V <sub>CC</sub> = 3 V	85	110		
I <sub>(LPM2)</sub>	Low-power mode, (LPM2), f <sub>(MCLK)</sub> = f <sub>(SMCLK)</sub> = 0 MHz, f <sub>(ACLK)</sub> = 32,768 Hz, SCG0 = 0 (see Note 2 and Note 4)	T <sub>A</sub> = -40°C to 85°C	V <sub>CC</sub> = 2.2 V	13	22		μA
			V <sub>CC</sub> = 3 V	18	30		
I <sub>(LPM3)</sub>	Low-power mode, (LPM3) f <sub>(MCLK)</sub> = f <sub>(SMCLK)</sub> = 0 MHz, f <sub>(ACLK)</sub> = 32,768 Hz, SCG0 = 1 Basic Timer1 enabled, ACLK selected LCD_A enabled, LCDCPEN = 0; (static mode; f <sub>LCD</sub> = f <sub>(ACLK)</sub> /32) (see Note 2 and Note 3 and Note 4)	T <sub>A</sub> = -40°C T <sub>A</sub> = 25°C T <sub>A</sub> = 60°C T <sub>A</sub> = 85°C	V <sub>CC</sub> = 2.2 V	1.0	2.0		μA
				1.1	2.0		
				2.0	5.0		
				7.0	15.0		
		T <sub>A</sub> = -40°C T <sub>A</sub> = 25°C T <sub>A</sub> = 60°C T <sub>A</sub> = 85°C	V <sub>CC</sub> = 3 V	1.8	2.8		μA
				1.6	2.7		
				2.5	7.0		
				8.5	21.0		
I <sub>(LPM3)</sub>	Low-power mode, (LPM3) f <sub>(MCLK)</sub> = f <sub>(SMCLK)</sub> = 0 MHz, f <sub>(ACLK)</sub> = 32,768 Hz, SCG0 = 1 Basic Timer1 enabled, ACLK selected LCD_A enabled, LCDCPEN = 0; (4-mux mode; f <sub>LCD</sub> = f <sub>(ACLK)</sub> /32) (see Note 2 and Note 3 and Note 4)	T <sub>A</sub> = -40°C T <sub>A</sub> = 25°C T <sub>A</sub> = 60°C T <sub>A</sub> = 85°C	V <sub>CC</sub> = 2.2 V	2.5	3.5		μA
				2.5	3.5		
				3.0	6.0		
				8.0	16.0		
		T <sub>A</sub> = -40°C T <sub>A</sub> = 25°C T <sub>A</sub> = 60°C T <sub>A</sub> = 85°C	V <sub>CC</sub> = 3 V	2.9	4.0		μA
				2.9	4.0		
				4.0	8.0		
				10.0	22.0		
I <sub>(LPM4)</sub>	Low-power mode, (LPM4) f <sub>(MCLK)</sub> = 0 MHz, f <sub>(SMCLK)</sub> = 0 MHz, f <sub>(ACLK)</sub> = 0 Hz, SCG0 = 1 (see Note 2 and Note 4)	T <sub>A</sub> = -40°C T <sub>A</sub> = 25°C T <sub>A</sub> = 60°C T <sub>A</sub> = 85°C	V <sub>CC</sub> = 2.2 V	0.1	0.5		μA
				0.3	0.7		
				1.7	5.0		
				7.0	15.0		
		T <sub>A</sub> = -40°C T <sub>A</sub> = 25°C T <sub>A</sub> = 60°C T <sub>A</sub> = 85°C	V <sub>CC</sub> = 3 V	0.1	0.8		μA
				0.4	0.9		
				2.0	7.0		
				8.0	21.0		

- NOTES: 1. Timer\_B is clocked by f<sub>(DCOCLK)</sub> = f<sub>(DCO)</sub> = 1 MHz. All inputs are tied to 0 V or to V<sub>CC</sub>. Outputs do not source or sink any current.  
2. All inputs are tied to 0 V or to V<sub>CC</sub>. Outputs do not source or sink any current.  
3. The LPM3 currents are characterized with a Micro Crystal CC4V-T1A (9 pF) crystal and OSCCAPx = 1h.  
4. Current for brownout included.

Current consumption of active mode versus system frequency, F-version:

$$I_{(AM)} = I_{(AM)} [1 \text{ MHz}] \times f_{(\text{System})} [\text{MHz}]$$

Current consumption of active mode versus supply voltage, F-version:

$$I_{(AM)} = I_{(AM)} [3 \text{ V}] + 200 \mu\text{A/V} \times (V_{\text{CC}} - 3 \text{ V})$$



# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

## SCHMITT-trigger inputs – Ports P1 to P10; $\overline{\text{RST}}/\text{NMI}$ ; JTAG: TCK, TMS, TDI/TCLK, TDO/TDI

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>CC</sub> = 2.2 V	1.1		1.55	V
		V <sub>CC</sub> = 3 V	1.5		1.98	
V <sub>IT-</sub>	Negative-going input threshold voltage	V <sub>CC</sub> = 2.2 V	0.4		0.9	V
		V <sub>CC</sub> = 3 V	0.9		1.3	
V <sub>hys</sub>	Input voltage hysteresis (V <sub>IT+</sub> – V <sub>IT-</sub> )	V <sub>CC</sub> = 2.2 V	0.3		1.1	V
		V <sub>CC</sub> = 3 V	0.5		1	

## inputs P<sub>x.x</sub>, T<sub>Ax</sub>, T<sub>Bx</sub>

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
t <sub>(int)</sub>	External interrupt timing	Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag, (see Note 1)	2.2 V	62			ns
			3 V	50			
t <sub>(cap)</sub>	Timer_A, Timer_B capture timing	TA0, TA1, TA2 TB0, TB1, TB2, TB3, TB4, TB5, TB6	2.2 V	62			ns
			3 V	50			
f <sub>(TAext)</sub>	Timer_A, Timer_B clock frequency externally applied to pin	TACLK, TBCLK, INCLK: t <sub>(H)</sub> = t <sub>(L)</sub>	2.2 V			8	MHz
f <sub>(TBext)</sub>			3 V			10	
f <sub>(TAint)</sub>	Timer_A, Timer_B clock frequency	SMCLK or ACLK signal selected	2.2 V			8	MHz
f <sub>(TBint)</sub>			3 V			10	

NOTES: 1. The external signal sets the interrupt flag every time the minimum t<sub>(int)</sub> parameters are met. It may be set even with trigger signals shorter than t<sub>(int)</sub>.

## leakage current – Ports P1 to P10 (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I <sub>lkg</sub> (P <sub>x.y</sub> )	Leakage current	Port P <sub>x</sub>	V <sub>(P<sub>x.y</sub>)</sub> (see Note 2) (1 ≤ x ≤ 10, 0 ≤ y ≤ 7)	V <sub>CC</sub> = 2.2 V/3 V		±50	nA

NOTES: 1. The leakage current is measured with V<sub>SS</sub> or V<sub>CC</sub> applied to the corresponding pin(s), unless otherwise noted.  
2. The port pin must be selected as input.

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs – Ports P1 to P10

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OH</sub> High-level output voltage	I <sub>OH(max)</sub> = -1.5 mA, V <sub>CC</sub> = 2.2 V, See Note 1	V <sub>CC</sub> -0.25		V <sub>CC</sub>	V
	I <sub>OH(max)</sub> = -6 mA, V <sub>CC</sub> = 2.2 V, See Note 2	V <sub>CC</sub> -0.6		V <sub>CC</sub>	
	I <sub>OH(max)</sub> = -1.5 mA, V <sub>CC</sub> = 3 V, See Note 1	V <sub>CC</sub> -0.25		V <sub>CC</sub>	
	I <sub>OH(max)</sub> = -6 mA, V <sub>CC</sub> = 3 V, See Note 2	V <sub>CC</sub> -0.6		V <sub>CC</sub>	
V <sub>OL</sub> Low-level output voltage	I <sub>OL(max)</sub> = 1.5 mA, V <sub>CC</sub> = 2.2 V, See Note 1	V <sub>SS</sub>		V <sub>SS</sub> +0.25	V
	I <sub>OL(max)</sub> = 6 mA, V <sub>CC</sub> = 2.2 V, See Note 2	V <sub>SS</sub>		V <sub>SS</sub> +0.6	
	I <sub>OL(max)</sub> = 1.5 mA, V <sub>CC</sub> = 3 V, See Note 1	V <sub>SS</sub>		V <sub>SS</sub> +0.25	
	I <sub>OL(max)</sub> = 6 mA, V <sub>CC</sub> = 3 V, See Note 2	V <sub>SS</sub>		V <sub>SS</sub> +0.6	

- NOTES: 1. The maximum total current, I<sub>OH(max)</sub> and I<sub>OL(max)</sub>, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.  
2. The maximum total current, I<sub>OH(max)</sub> and I<sub>OL(max)</sub>, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

output frequency

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>(Px,y)</sub> (1 ≤ x ≤ 10, 0 ≤ y ≤ 7)	C <sub>L</sub> = 20 pF, I <sub>L</sub> = ±1.5 mA	V <sub>CC</sub> = 2.2 V	DC	10	MHz
		V <sub>CC</sub> = 3 V	DC	12	MHz
f <sub>(MCLK)</sub> P1.1/TA0/MCLK, f <sub>(SMCLK)</sub> P1.4/TBCLK/SMCLK,	C <sub>L</sub> = 20 pF	V <sub>CC</sub> = 2.2 V		10	MHz
f <sub>(ACLK)</sub> P1.5/TACLK/ACLK		V <sub>CC</sub> = 3 V	DC	12	MHz
t <sub>(Xdc)</sub> Duty cycle of output frequency	P1.5/TACLK/ACLK, C <sub>L</sub> = 20 pF V <sub>CC</sub> = 2.2 V / 3 V	f <sub>(ACLK)</sub> = f <sub>(LFXT1)</sub> = f <sub>(XT1)</sub>	40%	60%	
		f <sub>(ACLK)</sub> = f <sub>(LFXT1)</sub> = f <sub>(LF)</sub>	30%	70%	
		f <sub>(ACLK)</sub> = f <sub>(LFXT1)</sub>		50%	
	P1.1/TA0/MCLK, C <sub>L</sub> = 20 pF, V <sub>CC</sub> = 2.2 V / 3 V	f <sub>(MCLK)</sub> = f <sub>(XT1)</sub>	40%	60%	
		f <sub>(MCLK)</sub> = f <sub>(DCOCLK)</sub>	50%- 15 ns	50%	50%+ 15 ns
	P1.4/TBCLK/SMCLK, C <sub>L</sub> = 20 pF, V <sub>CC</sub> = 2.2 V / 3 V	f <sub>(SMCLK)</sub> = f <sub>(XT2)</sub>	40%	60%	
f <sub>(SMCLK)</sub> = f <sub>(DCOCLK)</sub>		50%- 15 ns	50%	50%+ 15 ns	

# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics – outputs

TYPICAL LOW-LEVEL OUTPUT CURRENT  
vs  
LOW-LEVEL OUTPUT VOLTAGE

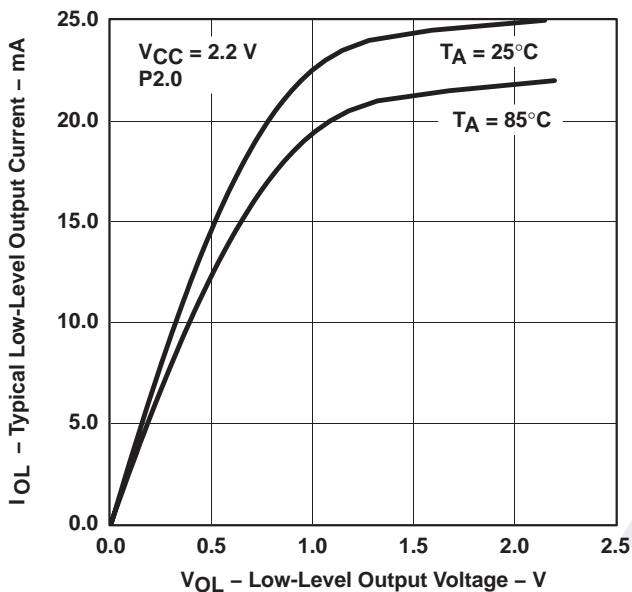


Figure 2

TYPICAL LOW-LEVEL OUTPUT CURRENT  
vs  
LOW-LEVEL OUTPUT VOLTAGE

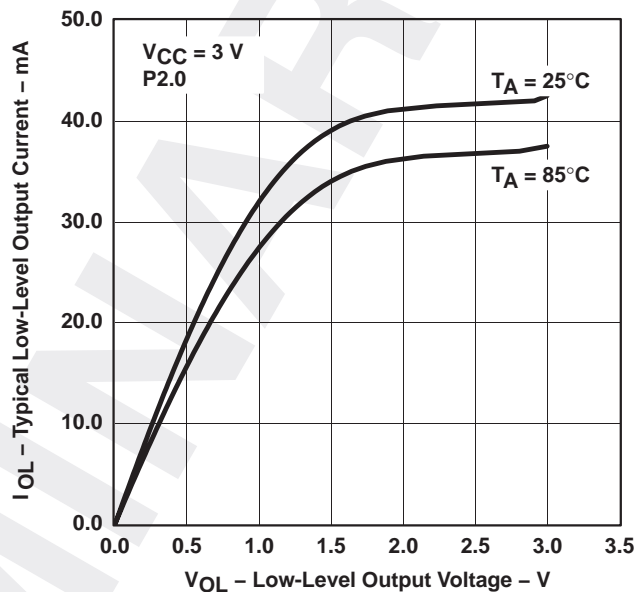


Figure 3

TYPICAL HIGH-LEVEL OUTPUT CURRENT  
vs  
HIGH-LEVEL OUTPUT VOLTAGE

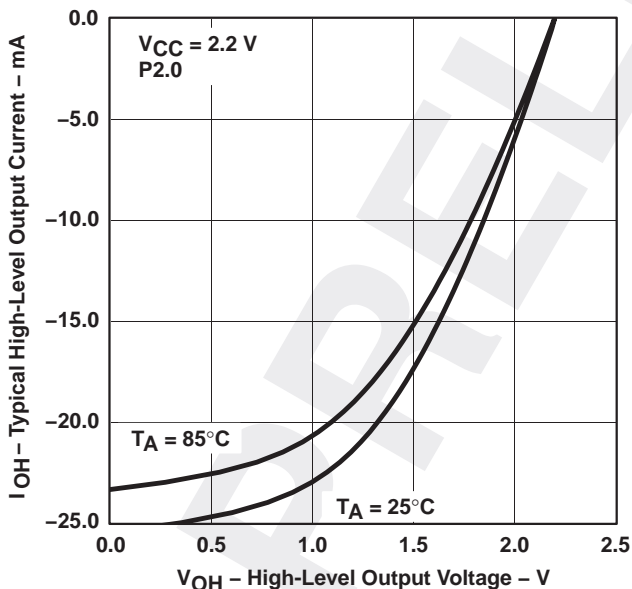


Figure 4

TYPICAL HIGH-LEVEL OUTPUT CURRENT  
vs  
HIGH-LEVEL OUTPUT VOLTAGE

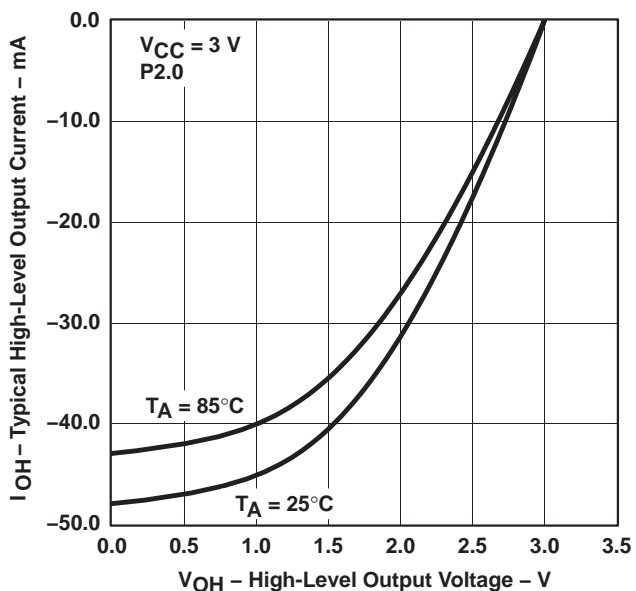


Figure 5

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

**wake-up LPM3**

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(LPM3)}$ Delay time	f = 1 MHz	$V_{CC} = 2.2\text{ V}/3\text{ V}$			6	$\mu\text{s}$
	f = 2 MHz				6	
	f = 3 MHz				6	

**RAM**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>RAMh</sub>	CPU halted (see Note 1)	1.6			V

NOTE 1: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

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# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

## LCD\_A

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>CC(LCD)</sub> Supply Voltage Range (see Note 2)	Charge pump enabled (LCDPEN = 1; VLCDx > 0000)		2.2		3.6	V
I <sub>CC(LCD)</sub> Supply Current (see Note 2)	V <sub>LCD(typ)</sub> =3V; LCDPEN = 1; VLCDx=1000; all segments on. f <sub>LCD</sub> = f <sub>ACLK</sub> /32 no LCD connected (see Note 4) T <sub>A</sub> = 25°C	2.2 V		3		μA
C <sub>LCD</sub> Capacitor on LCDCAP (see Note 1 and Note 3)	Charge pump enabled (LCDPEN = 1; VLCDx > 0000)		4.7			μF
f <sub>LCD</sub> LCD frequency					1.1	kHz
V <sub>LCD</sub> LCD voltage (see Note 3)	VLCDx = 0000			V <sub>CC</sub>		V
V <sub>LCD</sub> LCD voltage (see Note 3)	VLCDx = 0001			2.60		V
V <sub>LCD</sub> LCD voltage (see Note 3)	VLCDx = 0010			2.66		V
V <sub>LCD</sub> LCD voltage (see Note 3)	VLCDx = 0011			2.72		V
V <sub>LCD</sub> LCD voltage (see Note 3)	VLCDx = 0100			2.78		V
V <sub>LCD</sub> LCD voltage (see Note 3)	VLCDx = 0101			2.84		V
V <sub>LCD</sub> LCD voltage (see Note 3)	VLCDx = 0110			2.90		V
V <sub>LCD</sub> LCD voltage (see Note 3)	VLCDx = 0111			2.96		V
V <sub>LCD</sub> LCD voltage (see Note 3)	VLCDx = 1000			3.02		V
V <sub>LCD</sub> LCD voltage (see Note 3)	VLCDx = 1001			3.08		V
V <sub>LCD</sub> LCD voltage (see Note 3)	VLCDx = 1010			3.14		V
V <sub>LCD</sub> LCD voltage (see Note 3)	VLCDx = 1011			3.20		V
V <sub>LCD</sub> LCD voltage (see Note 3)	VLCDx = 1100			3.26		V
V <sub>LCD</sub> LCD voltage (see Note 3)	VLCDx = 1101			3.32		V
V <sub>LCD</sub> LCD voltage (see Note 3)	VLCDx = 1110			3.38		V
V <sub>LCD</sub> LCD voltage (see Note 3)	VLCDx = 1111			3.44	3.60	V
R <sub>LCD</sub> LCD Driver Output Impedance	V <sub>LCD</sub> =3V; CPEN = 1; VLCDx = 1000, I <sub>LOAD</sub> = ± 10 μA	2.2 V			10	kΩ

- NOTES: 1. Enabling the internal charge pump with an external capacitor smaller than the minimum specified might damage the device.  
 2. Refer to the supply current specifications I<sub>(LPM3)</sub> for additional current specifications with the LCD\_A module active.  
 3. Segments S0 through S3 must be disabled and cannot be used when the LCD charge pump feature is enabled. In addition, when using segments S0 through S3 with an external LCD voltage supply, V<sub>LCD</sub> ≤ AV<sub>CC</sub>.  
 4. Connecting an actual display will increase the current consumption depending on the size of the LCD.

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Comparator\_A (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
I <sub>(CC)</sub>		CAON=1, CARSEL=0, CAREF=0	V <sub>CC</sub> = 2.2 V	25	40	μA	
			V <sub>CC</sub> = 3 V	45	60		
I <sub>(Refladder/RefDiode)</sub>		CAON=1, CARSEL=0, CAREF=1/2/3, No load at P1.6/CA0 and P1.7/CA1	V <sub>CC</sub> = 2.2 V	30	50	μA	
			V <sub>CC</sub> = 3 V	45	71		
V <sub>(Ref025)</sub>	$\frac{\text{Voltage @ } 0.25 V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=1, No load at P1.6/CA0 and P1.7/CA1	V <sub>CC</sub> = 2.2 V / 3 V			0.23 0.24 0.25	
V <sub>(Ref050)</sub>	$\frac{\text{Voltage @ } 0.5 V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=2, No load at P1.6/CA0 and P1.7/CA1	V <sub>CC</sub> = 2.2V / 3 V			0.47 0.48 0.5	
V <sub>(RefVT)</sub>		PCA0=1, CARSEL=1, CAREF=3, No load at P1.6/CA0 and P1.7/CA1; T <sub>A</sub> = 85°C	V <sub>CC</sub> = 2.2 V	390	480	540	mV
			V <sub>CC</sub> = 3 V	400	490	550	
V <sub>IC</sub>	Common-mode input voltage range	CAON=1	V <sub>CC</sub> = 2.2 V / 3 V			0 V <sub>CC</sub> -1	V
V <sub>p-VS</sub>	Offset voltage	See Note 2	V <sub>CC</sub> = 2.2 V / 3 V			-30 30	mV
V <sub>hys</sub>	Input hysteresis	CAON = 1	V <sub>CC</sub> = 2.2 V / 3 V			0 0.7 1.4	mV
t <sub>(response LH)</sub>		T <sub>A</sub> = 25°C, Overdrive 10 mV, without filter: CAF = 0	V <sub>CC</sub> = 2.2 V	160	210	300	ns
			V <sub>CC</sub> = 3 V	80	150	240	
		T <sub>A</sub> = 25°C Overdrive 10 mV, with filter: CAF = 1	V <sub>CC</sub> = 2.2 V	1.4	1.9	3.4	μs
			V <sub>CC</sub> = 3 V	0.9	1.5	2.6	
t <sub>(response HL)</sub>		T <sub>A</sub> = 25°C Overdrive 10 mV, without filter: CAF = 0	V <sub>CC</sub> = 2.2 V	130	210	300	ns
			V <sub>CC</sub> = 3 V	80	150	240	
		T <sub>A</sub> = 25°C, Overdrive 10 mV, with filter: CAF = 1	V <sub>CC</sub> = 2.2 V	1.4	1.9	3.4	μs
			V <sub>CC</sub> = 3 V	0.9	1.5	2.6	

- NOTES: 1. The leakage current for the Comparator\_A terminals is identical to I<sub>lkg(Px.x)</sub> specification.  
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator\_A inputs on successive measurements. The two successive measurements are then summed together.

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typical characteristics

REFERENCE VOLTAGE  
 vs  
 FREE-AIR TEMPERATURE

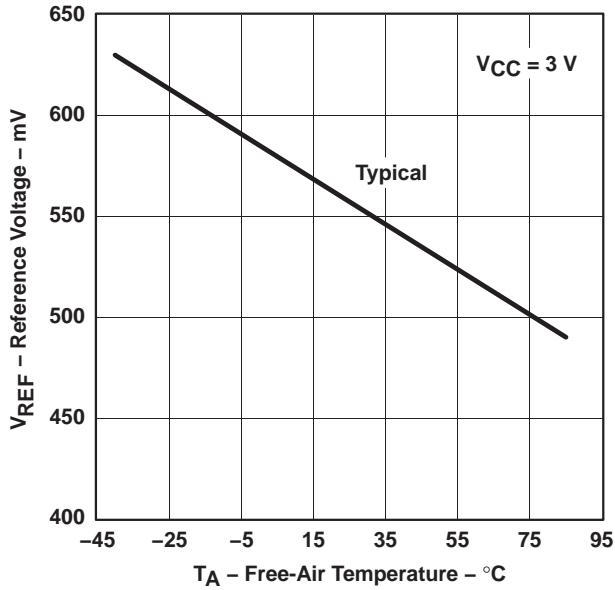


Figure 6.  $V_{(RefVT)}$  vs Temperature

REFERENCE VOLTAGE  
 vs  
 FREE-AIR TEMPERATURE

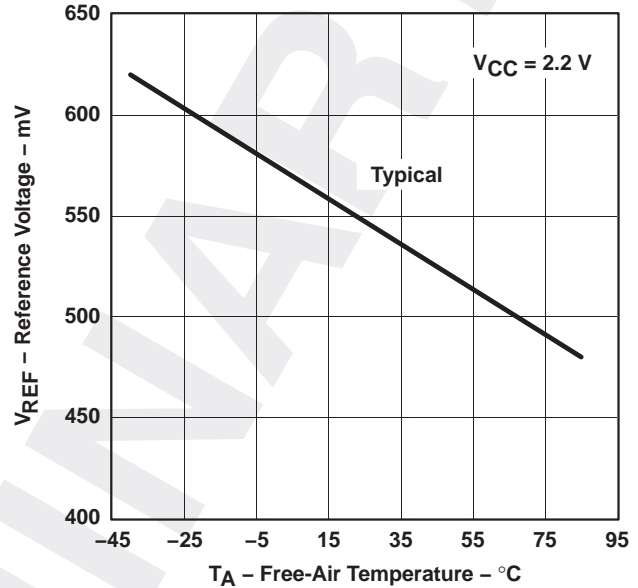


Figure 7.  $V_{(RefVT)}$  vs Temperature

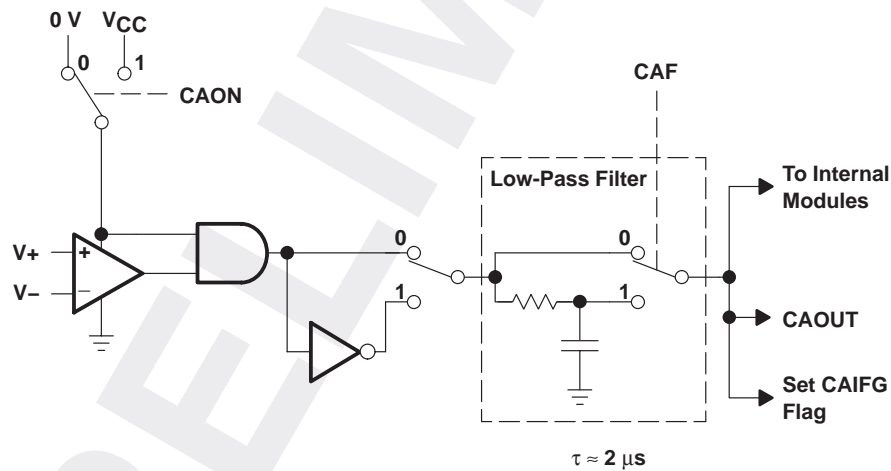


Figure 8. Block Diagram of Comparator\_A Module

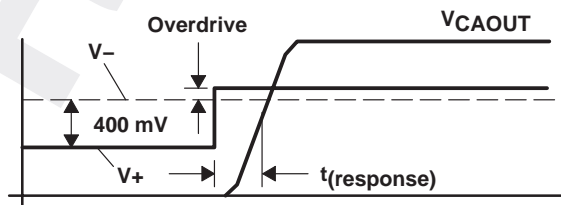


Figure 9. Overdrive Definition

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

**POR/brownout reset (BOR) (see Note 1)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_d(\text{BOR})$				2000	$\mu\text{s}$
$V_{\text{CC}}(\text{start})$	$dV_{\text{CC}}/dt \leq 3 \text{ V/s}$ (see Figure 10)		$0.7 \times V(\text{B\_IT-})$		V
$V(\text{B\_IT-})$	Brownout (see Note 2)			1.71	V
$V_{\text{hys}}(\text{B\_IT-})$	$dV_{\text{CC}}/dt \leq 3 \text{ V/s}$ (see Figure 10)	70	130	180	mV
$t(\text{reset})$	Pulse length needed at $\overline{\text{RST}}/\text{NMI}$ pin to accepted reset internally, $V_{\text{CC}} = 2.2 \text{ V}/3 \text{ V}$	2			$\mu\text{s}$

- NOTES: 1. The current consumption of the brownout module is already included in the  $I_{\text{CC}}$  current consumption data. The voltage level  $V(\text{B\_IT-}) + V_{\text{hys}}(\text{B\_IT-})$  is  $\leq 1.8\text{V}$ .  
2. During power up, the CPU begins code execution following a period of  $t_d(\text{BOR})$  after  $V_{\text{CC}} = V(\text{B\_IT-}) + V_{\text{hys}}(\text{B\_IT-})$ . The default FLL+ settings must not be changed until  $V_{\text{CC}} \geq V_{\text{CC}}(\text{min})$ , where  $V_{\text{CC}}(\text{min})$  is the minimum supply voltage for the desired operating frequency. See the *MSP430x4xx Family User's Guide* for more information on the brownout/SVS circuit.

**typical characteristics**

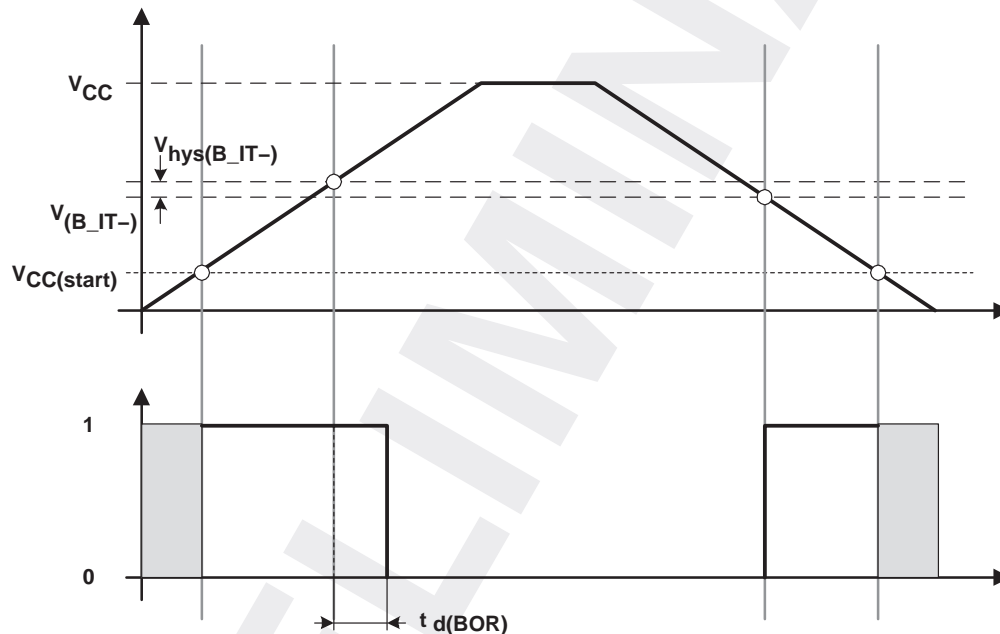


Figure 10. POR/Brownout Reset (BOR) vs Supply Voltage

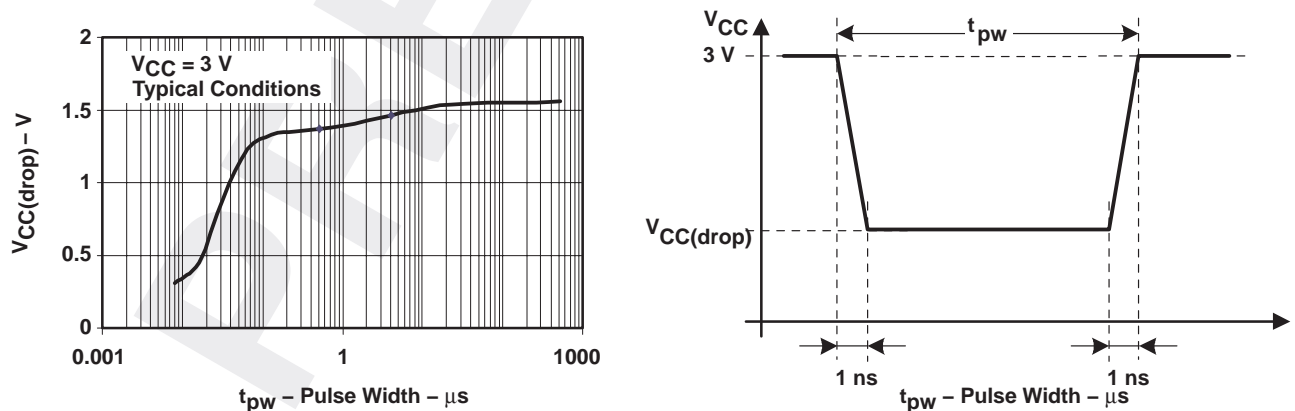


Figure 11.  $V_{\text{CC}}(\text{drop})$  Level With a Square Voltage Drop to Generate a POR/Brownout Signal

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## typical characteristics

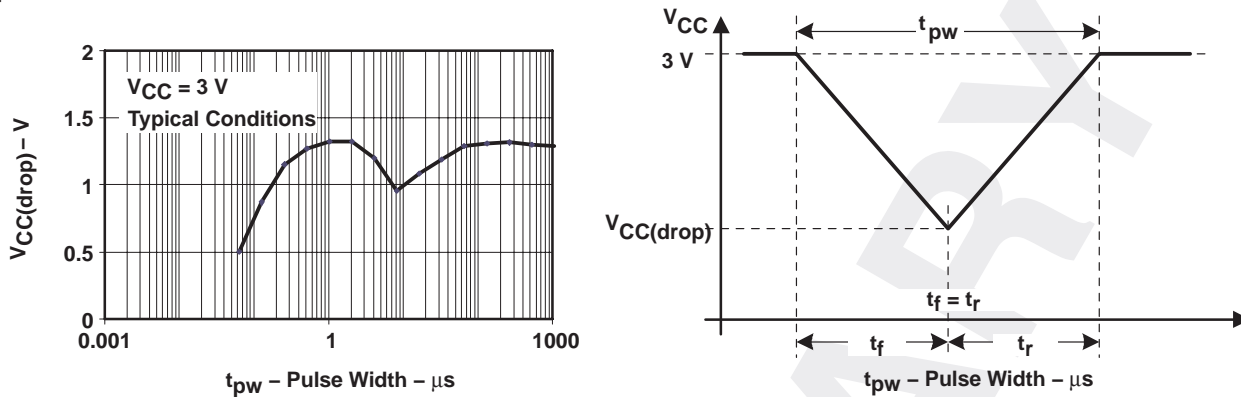


Figure 12.  $V_{CC(drop)}$  Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

SVS (supply voltage supervisor/monitor) (see Note 1)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT	
$t_{(SVSR)}$	$dV_{CC}/dt > 30 \text{ V/ms}$ (see Figure 13)	5		150	$\mu\text{s}$	
	$dV_{CC}/dt \leq 30 \text{ V/ms}$			2000	$\mu\text{s}$	
$t_{d(SVSON)}$	SVSON, switch from VLD=0 to VLD $\neq$ 0, $V_{CC} = 3 \text{ V}$	20		150	$\mu\text{s}$	
$t_{settle}$	VLD $\neq$ 0 <sup>†</sup>			12	$\mu\text{s}$	
$V_{(SVSstart)}$	VLD $\neq$ 0, $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 13)		1.55	1.7	V	
$V_{hys(SVS\_IT-)}$	$V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 13)	VLD = 1	70	120	155	mV
		VLD = 2 .. 14	$V_{(SVS\_IT-)} \times 0.001$		$V_{(SVS\_IT-)} \times 0.016$	
	$V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 13), external voltage applied on A7	VLD = 15	4.4		20	mV
$V_{(SVS\_IT-)}$	$V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 13)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.23	
		VLD = 3	2.05	2.2	2.35	
		VLD = 4	2.14	2.3	2.46	
		VLD = 5	2.24	2.4	2.58	
		VLD = 6	2.33	2.5	2.69	
		VLD = 7	2.46	2.65	2.84	
		VLD = 8	2.58	2.8	2.97	
		VLD = 9	2.69	2.9	3.10	
		VLD = 10	2.83	3.05	3.26	
		VLD = 11	2.94	3.2	3.39	
		VLD = 12	3.11	3.35	3.58 <sup>†</sup>	
		VLD = 13	3.24	3.5	3.73 <sup>†</sup>	
		VLD = 14	3.43	3.7 <sup>†</sup>	3.96 <sup>†</sup>	
	$V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 13), external voltage applied on A7	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$ (see Note 1)	VLD $\neq$ 0, $V_{CC} = 2.2 \text{ V}/3 \text{ V}$		10	15	$\mu\text{A}$	

<sup>†</sup> The recommended operating voltage range is limited to 3.6 V.

<sup>‡</sup>  $t_{settle}$  is the settling time that the comparator o/p needs to have a stable level after VLD is switched VLD  $\neq$  0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be  $> 50 \text{ mV}$ .

NOTE 1: The current consumption of the SVS module is not included in the  $I_{CC}$  current consumption data.

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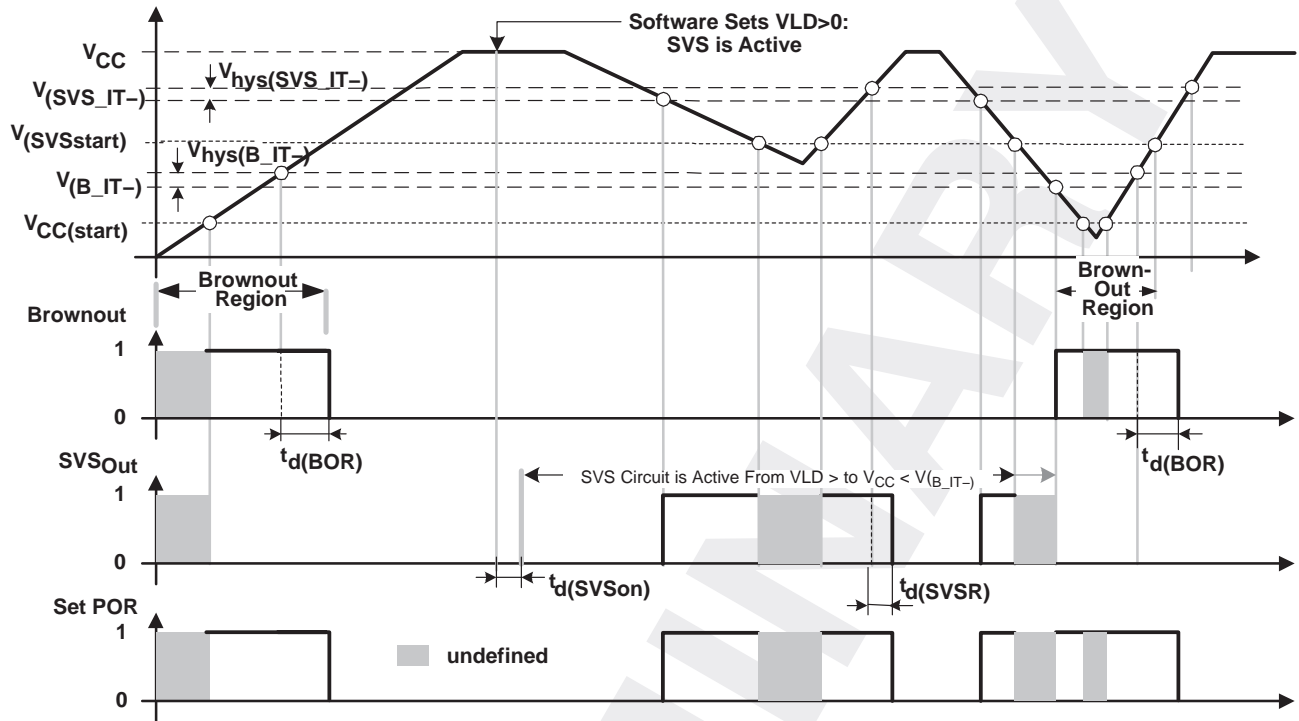


Figure 13. SVS Reset (SVSR) vs Supply Voltage

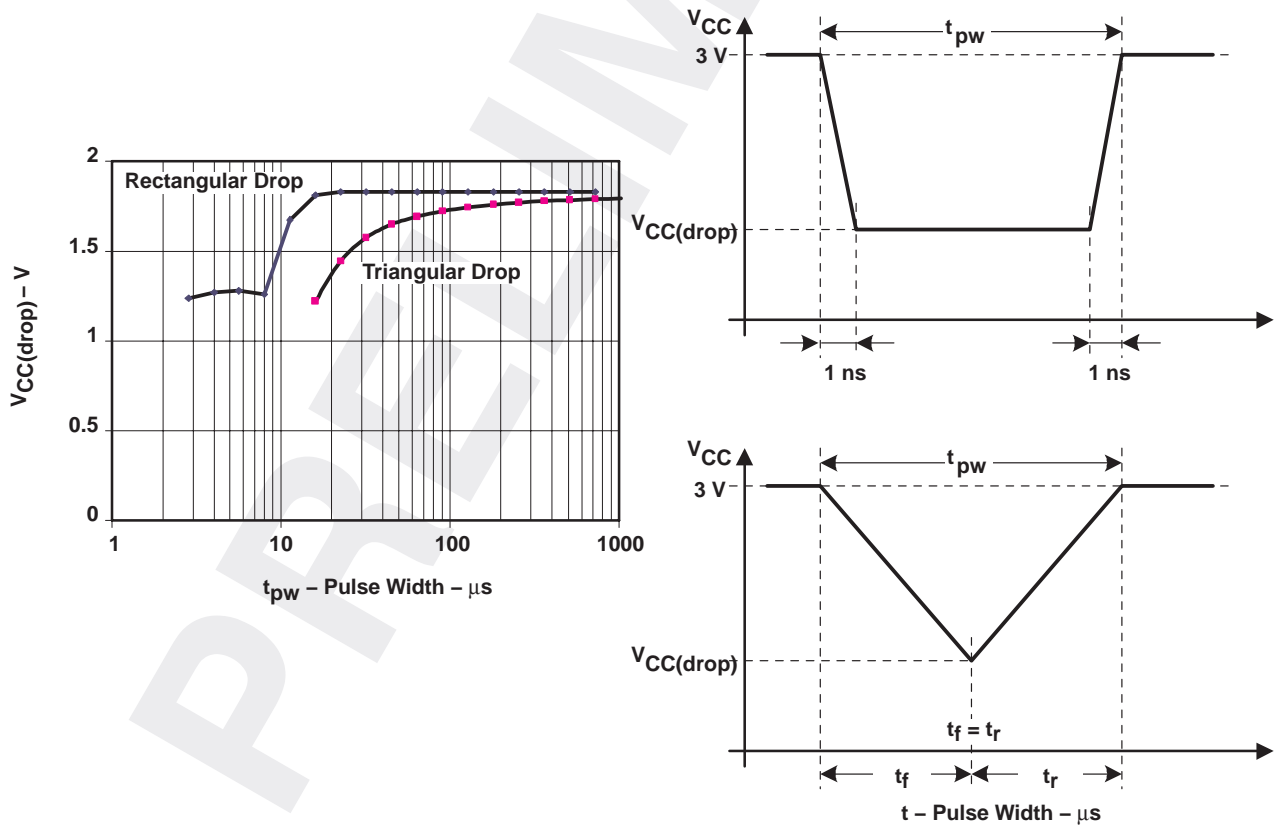


Figure 14. V<sub>CC(drop)</sub> With a Square Voltage Drop and a Triangle Voltage Drop to Generate an SVS Signal

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## DCO

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
f <sub>(DCOCLK)</sub>	N <sub>(DCO)</sub> =01E0h, FN <sub>8</sub> =FN <sub>4</sub> =FN <sub>3</sub> =FN <sub>2</sub> =0, D = 2; DCOPLUS = 0	2.2 V/3 V		1		MHz
f <sub>(DCO2)</sub>	FN <sub>8</sub> =FN <sub>4</sub> =FN <sub>3</sub> =FN <sub>2</sub> =0; DCOPLUS = 1	2.2 V	0.3	0.65	1.25	MHz
		3 V	0.3	0.7	1.3	
f <sub>(DCO27)</sub>	FN <sub>8</sub> =FN <sub>4</sub> =FN <sub>3</sub> =FN <sub>2</sub> =0; DCOPLUS = 1, (see Note 1)	2.2 V	2.5	5.6	10.5	MHz
		3 V	2.7	6.1	11.3	
f <sub>(DCO2)</sub>	FN <sub>8</sub> =FN <sub>4</sub> =FN <sub>3</sub> =0, FN <sub>2</sub> =1; DCOPLUS = 1	2.2 V	0.7	1.3	2.3	MHz
		3 V	0.8	1.5	2.5	
f <sub>(DCO27)</sub>	FN <sub>8</sub> =FN <sub>4</sub> =FN <sub>3</sub> =0, FN <sub>2</sub> =1; DCOPLUS = 1, (see Note 1)	2.2 V	5.7	10.8	18	MHz
		3 V	6.5	12.1	20	
f <sub>(DCO2)</sub>	FN <sub>8</sub> =FN <sub>4</sub> =0, FN <sub>3</sub> =1, FN <sub>2</sub> =x; DCOPLUS = 1	2.2 V	1.2	2	3	MHz
		3 V	1.3	2.2	3.5	
f <sub>(DCO27)</sub>	FN <sub>8</sub> =FN <sub>4</sub> =0, FN <sub>3</sub> =1, FN <sub>2</sub> =x; DCOPLUS = 1, (see Note 1)	2.2 V	9	15.5	25	MHz
		3 V	10.3	17.9	28.5	
f <sub>(DCO2)</sub>	FN <sub>8</sub> =0, FN <sub>4</sub> =1, FN <sub>3</sub> =FN <sub>2</sub> =x; DCOPLUS = 1	2.2 V	1.8	2.8	4.2	MHz
		3 V	2.1	3.4	5.2	
f <sub>(DCO27)</sub>	FN <sub>8</sub> =0, FN <sub>4</sub> =1, FN <sub>3</sub> =FN <sub>2</sub> =x; DCOPLUS = 1, (see Note 1)	2.2 V	13.5	21.5	33	MHz
		3 V	16	26.6	41	
f <sub>(DCO2)</sub>	FN <sub>8</sub> =1, FN <sub>4</sub> =FN <sub>3</sub> =FN <sub>2</sub> =x; DCOPLUS = 1	2.2 V	2.8	4.2	6.2	MHz
		3 V	4.2	6.3	9.2	
f <sub>(DCO27)</sub>	FN <sub>8</sub> =1, FN <sub>4</sub> =FN <sub>3</sub> =FN <sub>2</sub> =x; DCOPLUS = 1, (see Note 1)	2.2 V	21	32	46	MHz
		3 V	30	46	70	
S <sub>n</sub>	Step size between adjacent DCO taps: S <sub>n</sub> = f <sub>DCO</sub> (Tap n+1) / f <sub>DCO</sub> (Tap n), (see Figure 16 for taps 21 to 27)	1 < TAP ≤ 20			1.06	1.11
		TAP = 27			1.07	1.17
D <sub>t</sub>	Temperature drift, N <sub>(DCO)</sub> = 01E0h, FN <sub>8</sub> =FN <sub>4</sub> =FN <sub>3</sub> =FN <sub>2</sub> =0 D = 2; DCOPLUS = 0	2.2 V	-0.2	-0.3	-0.4	%/ <sup>o</sup> C
		3 V	-0.2	-0.3	-0.4	
D <sub>V</sub>	Drift with V <sub>CC</sub> variation, N <sub>(DCO)</sub> = 01E0h, FN <sub>8</sub> =FN <sub>4</sub> =FN <sub>3</sub> =FN <sub>2</sub> =0 D = 2; DCOPLUS = 0		0	5	15	%/V

NOTES: 1. Do not exceed the maximum system frequency.

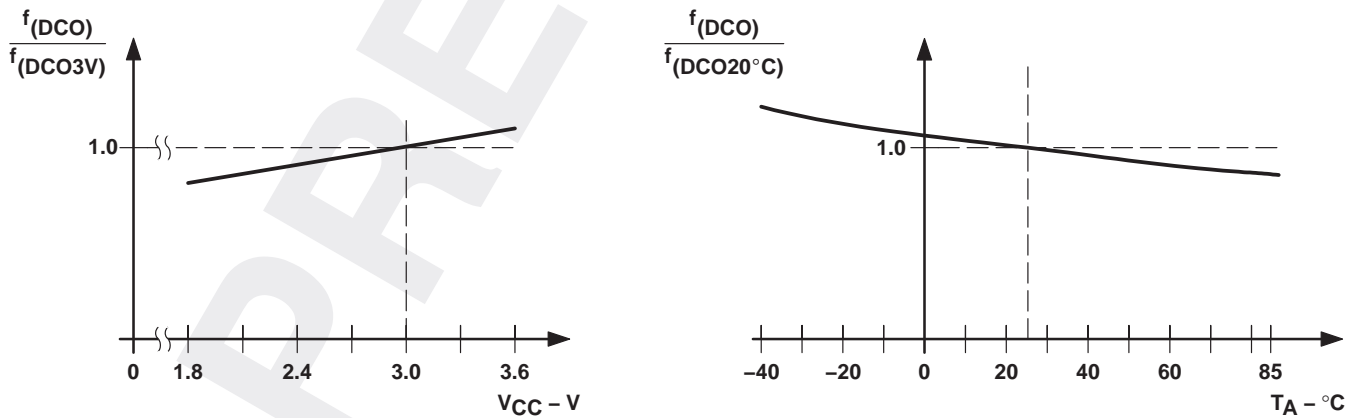


Figure 15. DCO Frequency vs Supply Voltage V<sub>CC</sub> and vs Ambient Temperature

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

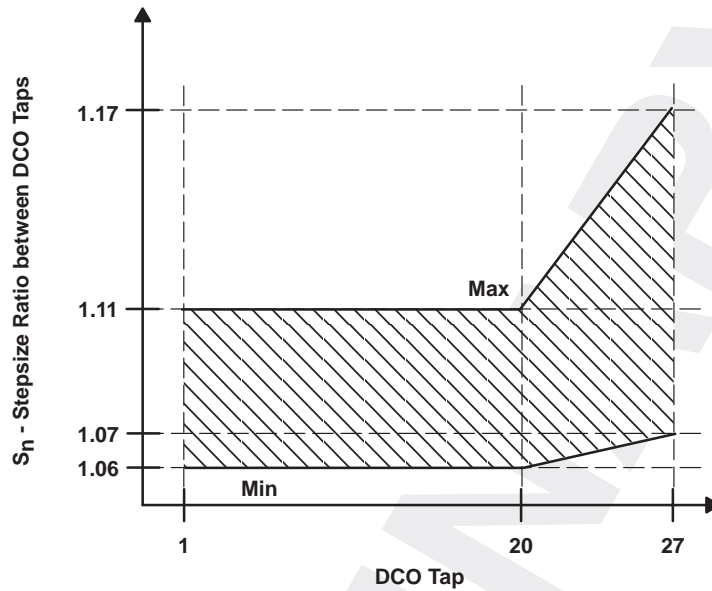


Figure 16. DCO Tap Step Size

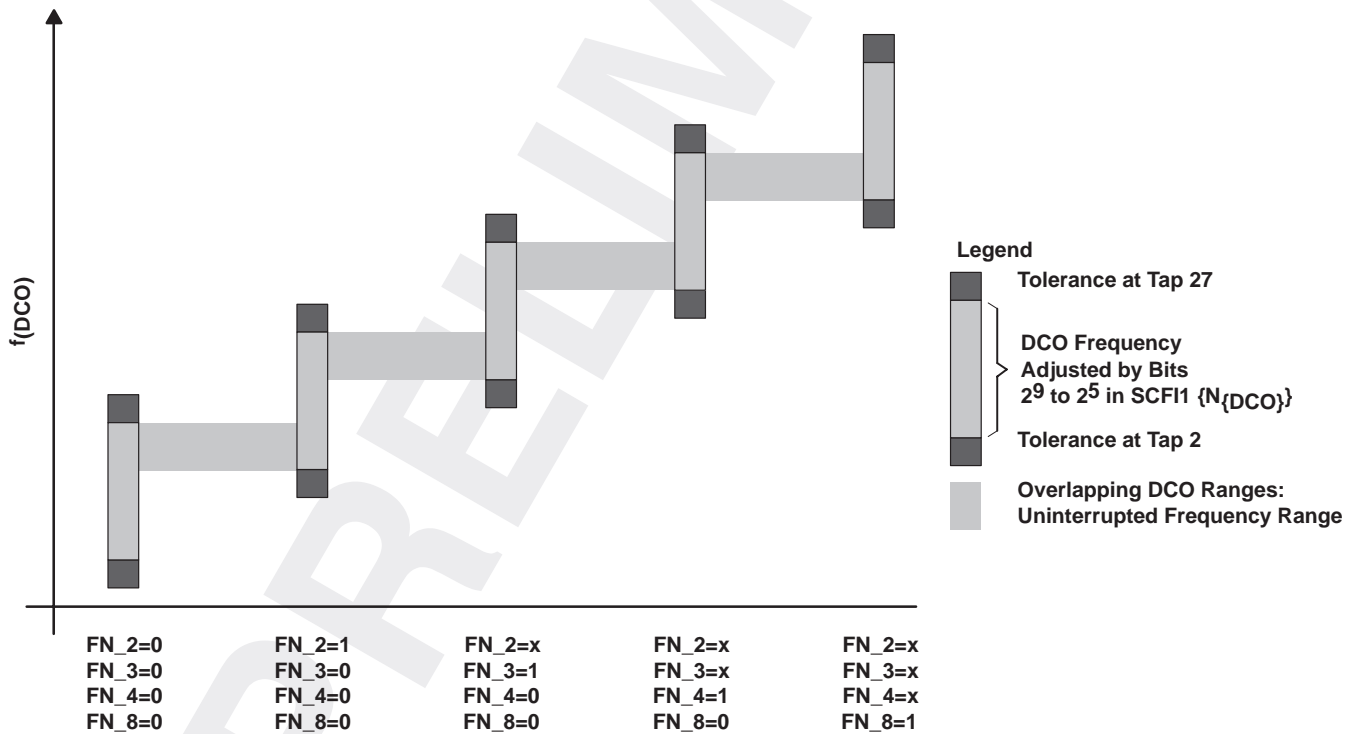


Figure 17. Five Overlapping DCO Ranges Controlled by FN\_x Bits

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

crystal oscillator, LFXT1 oscillator (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C <sub>XIN</sub>	Integrated input capacitance (see Note 4)	OSCCAPx = 0h, V <sub>CC</sub> = 2.2 V / 3 V		0		pF
		OSCCAPx = 1h, V <sub>CC</sub> = 2.2 V / 3 V		10		
		OSCCAPx = 2h, V <sub>CC</sub> = 2.2 V / 3 V		14		
		OSCCAPx = 3h, V <sub>CC</sub> = 2.2 V / 3 V		18		
C <sub>XOUT</sub>	Integrated output capacitance (see Note 4)	OSCCAPx = 0h, V <sub>CC</sub> = 2.2 V / 3 V		0		pF
		OSCCAPx = 1h, V <sub>CC</sub> = 2.2 V / 3 V		10		
		OSCCAPx = 2h, V <sub>CC</sub> = 2.2 V / 3 V		14		
		OSCCAPx = 3h, V <sub>CC</sub> = 2.2 V / 3 V		18		
V <sub>IL</sub>	Input levels at XIN	V <sub>CC</sub> = 2.2 V/3 V (see Note 3)	V <sub>SS</sub>		0.2×V <sub>CC</sub>	V
V <sub>IH</sub>			0.8×V <sub>CC</sub>		V <sub>CC</sub>	

- NOTES:
- The parasitic capacitance from the package and board may be estimated to be 2 pF. The effective load capacitor for the crystal is  $(C_{XIN} \times C_{XOUT}) / (C_{XIN} + C_{XOUT})$ . This is independent of XTS\_FLL.
  - To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines should be observed.
    - Keep as short of a trace as possible between the 'FG461x and the crystal.
    - Design a good ground plane around the oscillator pins.
    - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
    - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
    - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
    - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
    - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
  - Applies only when using an external logic-level clock source. XTS\_FLL must be set. Not applicable when using a crystal or resonator.
  - External capacitance is recommended for precision real-time clock applications; OSCCAPx = 0h.

crystal oscillator, XT2 oscillator (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
C <sub>XT2IN</sub>	Integrated input capacitance	V <sub>CC</sub> = 2.2 V/3 V		2		pF
C <sub>XT2OUT</sub>	Integrated output capacitance	V <sub>CC</sub> = 2.2 V/3 V		2		pF
V <sub>IL</sub>	Input levels at XT2IN	V <sub>CC</sub> = 2.2 V/3 V (see Note 2)	V <sub>SS</sub>		0.2 × V <sub>CC</sub>	V
V <sub>IH</sub>			0.8 × V <sub>CC</sub>		V <sub>CC</sub>	V

- NOTES:
- The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.
  - Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

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**USCI (UART Mode)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
f <sub>USCI</sub>	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty Cycle = 50% ± 10%			f <sub>SYSTEM</sub>		MHz
f <sub>BITCLK</sub>	BITCLK clock frequency (equals Baudrate in MBaud)		2.2 V /3.0 V			1	MHz
t <sub>τ</sub>	UART receive deglitch time (see Note 1)		2.2 V	50	150	600	ns
			3.0 V	50	100	600	ns

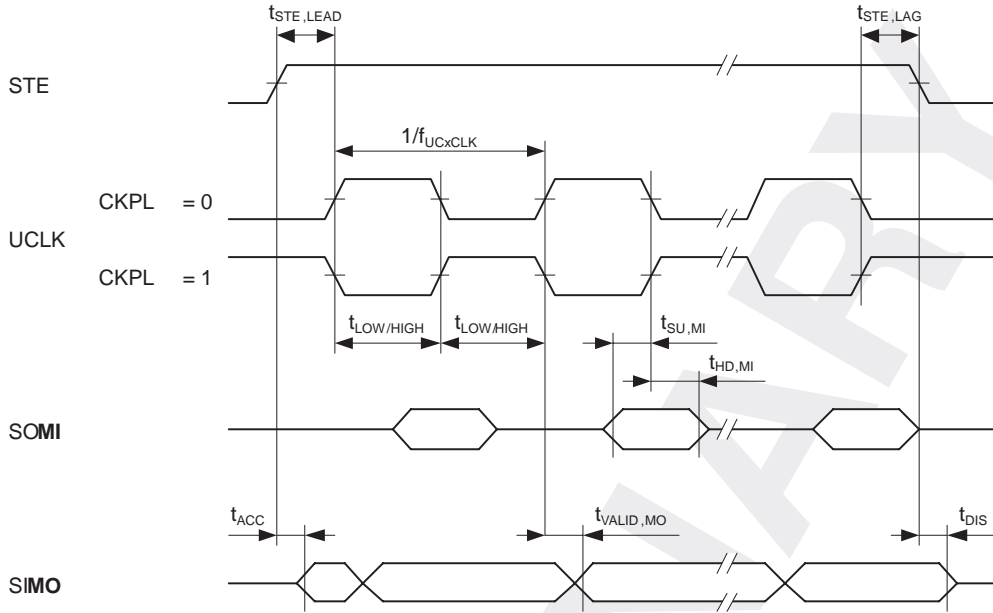
NOTES: 1. Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

**USCI (SPI Master Mode, see Figure 18 and Figure 19)**

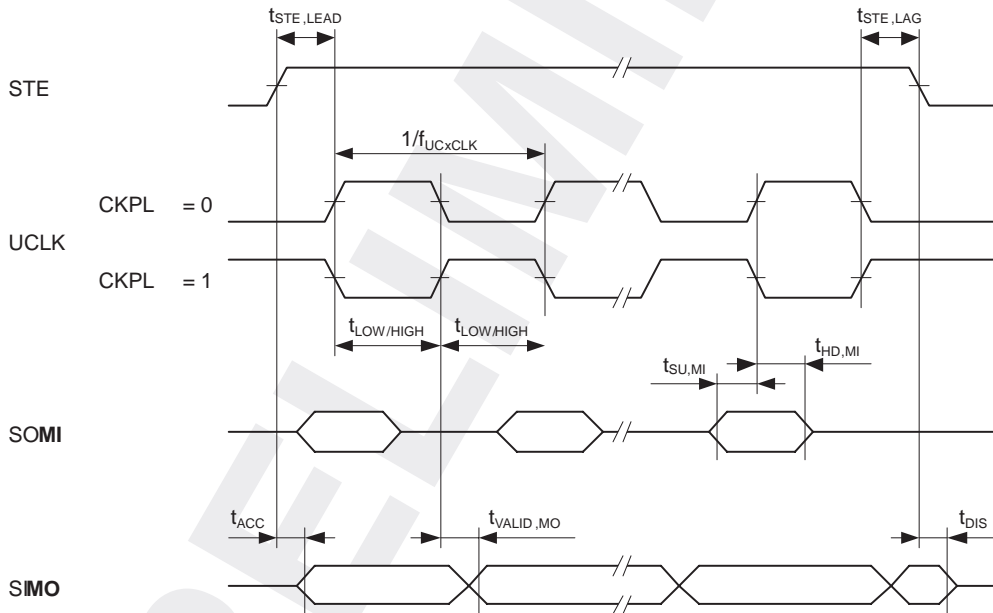
PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
f <sub>USCI</sub>	USCI input clock frequency	SMCLK, ACLK Duty Cycle = 50% ± 10%			f <sub>SYSTEM</sub>		MHz
t <sub>SU,MI</sub>	SOMI input data setup time		2.2 V	TBD			ns
			3.0 V	TBD			ns
t <sub>HD,MI</sub>	SOMI input data hold time		2.2 V	0			ns
			3.0 V	0			ns
t <sub>VALID,MO</sub>	SIMO output data valid time	UCLK edge to SIMO valid; C <sub>L</sub> = 20 pF	2.2 V		30	TBD	ns
			3.0 V		30	TBD	ns

**USCI (SPI Slave Mode, see Figure 20 and Figure 21)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
t <sub>STE,LEAD</sub>	STE lead time STE low to clock		2.2 V/3.0 V		50		ns
t <sub>STE,LAG</sub>	STE lag time Last clock to STE high		2.2 V/3.0 V	10			ns
t <sub>STE,ACC</sub>	STE access time STE low to SOMI data out	C <sub>L</sub> = 20 pF	2.2 V/3.0 V		50		ns
t <sub>STE,DIS</sub>	STE disable time STE high to SOMI high impedance		2.2 V/3.0 V		50		ns
t <sub>SU,SI</sub>	SIMO input data setup time		2.2 V	TBD			ns
			3.0 V	TBD			ns
t <sub>HD,SI</sub>	SIMO input data hold time		2.2 V	0			ns
			3.0 V	0			ns
t <sub>VALID,SO</sub>	SOMI output data valid time	UCLK edge to SOMI valid; C <sub>L</sub> = 20 pF	2.2 V		50	TBD	ns
			3.0 V		50	TBD	ns



**Figure 18. SPI Master Mode, CKPH = 0**



**Figure 19. SPI Master Mode, CKPH = 1**



electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

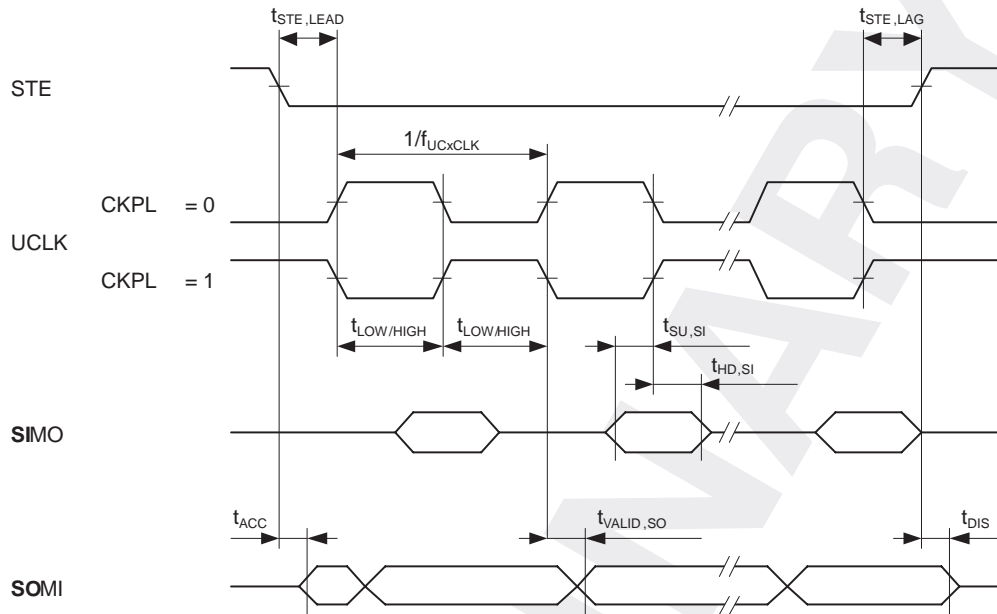


Figure 20. SPI Slave Mode, CKPH = 0

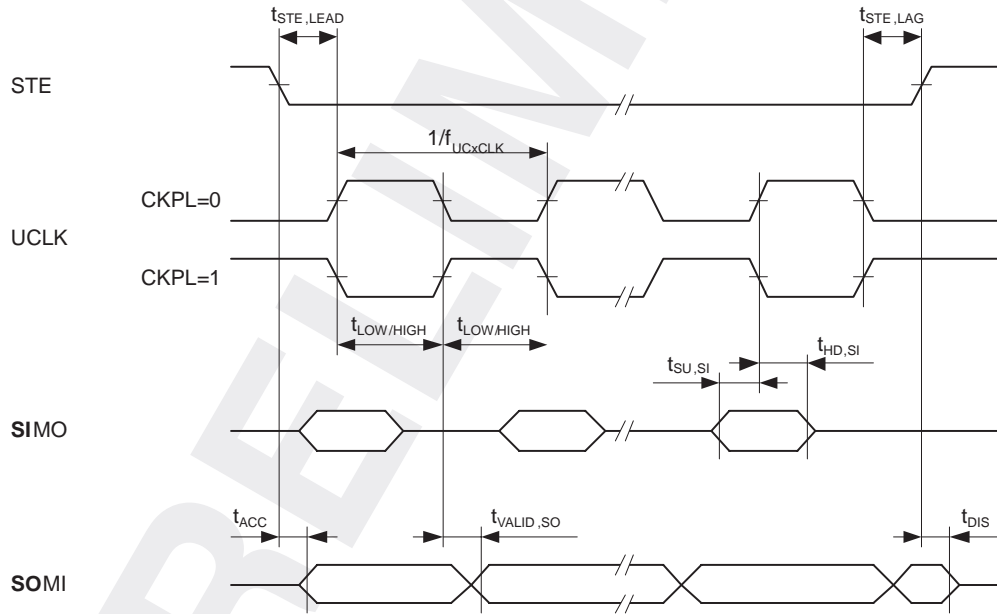


Figure 21. SPI Slave Mode, CKPH = 1

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## USCI (I2C Mode, see Figure 22)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
f <sub>USCI</sub>	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty Cycle = 50% ± 10%		f <sub>SYSTEM</sub>			MHz
f <sub>SCL</sub>	SCL clock frequency		2.2 V/3.0 V	0		400	kHz
t <sub>HD,STA</sub>	Hold time (repeated) START	f <sub>SCL</sub> ≤ 100kHz	2.2 V/3.0 V	4.0			us
		f <sub>SCL</sub> > 100kHz	2.2 V/3.0 V	0.6			us
t <sub>SU,STA</sub>	Set-up time for a repeated START	f <sub>SCL</sub> ≤ 100kHz	2.2 V/3.0 V	4.7			us
		f <sub>SCL</sub> > 100kHz	2.2 V/3.0 V	0.6			us
t <sub>HD,DAT</sub>	Data hold time		2.2 V/3.0 V	0			ns
t <sub>SU,DAT</sub>	Data set-up time		2.2 V/3.0 V	250			ns
t <sub>SU,STO</sub>	Set-up time for STOP		2.2 V/3.0 V	4.0			us
t <sub>SP</sub>	Pulse width of spikes suppressed by input filter		2.2 V	50	150	600	ns
			3.0 V	50	100	600	ns

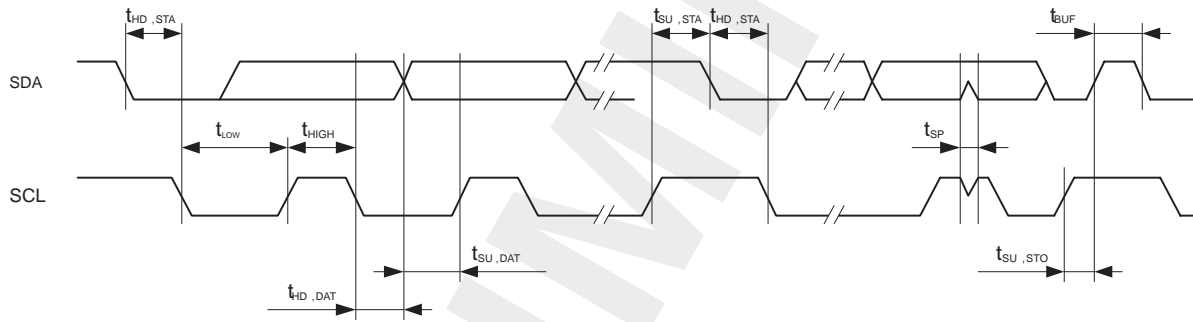


Figure 22. I2C Mode Timing

## USART1 (see Note 1)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t <sub>(τ)</sub>	V <sub>CC</sub> = 2.2 V	200	430	800	ns
	V <sub>CC</sub> = 3 V	150	280	500	

NOTES: 1. The signal applied to the USART1 receive signal terminal (URXD1) should meet the timing requirements of t<sub>(τ)</sub> to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of t<sub>(τ)</sub>. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD1 line.

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, power supply and input range conditions (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$V_{AVCC}$	Analog supply voltage	AVCC and DVCC are connected together AVSS and DVSS are connected together $V_{(AVSS)} = V_{(DVSS)} = 0\text{ V}$		2.2		3.6	V
$V_{(P6.x/Ax)}$	Analog input voltage range (see Note 2)	All external Ax terminals. Analog inputs selected in ADC12MCTLx register and P6Sel.x=1 $V_{(AVSS)} \leq V_{Ax} \leq V_{(AVCC)}$		0		$V_{AVCC}$	V
$I_{ADC12}$	Operating supply current into AVCC terminal (see Note 3)	$f_{ADC12CLK} = 5.0\text{ MHz}$ ADC12ON = 1, REFON = 0 SHT0=0, SHT1=0, ADC12DIV=0	$V_{CC} = 2.2\text{ V}$	0.65	1.3	mA	
			$V_{CC} = 3\text{ V}$	0.8	1.6		
$I_{REF+}$	Operating supply current into AVCC terminal (see Note 4)	$f_{ADC12CLK} = 5.0\text{ MHz}$ ADC12ON = 0, REFON = 1, REF2_5V = 1	$V_{CC} = 3\text{ V}$	0.5	0.8	mA	
			$V_{CC} = 2.2\text{ V}$	0.5	0.8		
		$f_{ADC12CLK} = 5.0\text{ MHz}$ ADC12ON = 0, REFON = 1, REF2_5V = 0	$V_{CC} = 2.2\text{ V}$	0.5	0.8	mA	
			$V_{CC} = 3\text{ V}$	0.5	0.8		
$C_I$	Input capacitance	Only one terminal can be selected at one time, Ax				40	pF
$R_I$	Input MUX ON resistance	$0V \leq V_{Ax} \leq V_{AVCC}$				2000	$\Omega$

- NOTES: 1. The leakage current is defined in the leakage current table with Ax parameter.  
2. The analog input voltage range must be within the selected reference voltage range  $V_{R+}$  to  $V_{R-}$  for valid conversion results.  
3. The internal reference supply current is not included in current consumption parameter  $I_{ADC12}$ .  
4. The internal reference current is supplied via terminal AVCC. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

12-bit ADC, external reference (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$V_{eREF+}$	Positive external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 2)		1.4		$V_{AVCC}$	V
$V_{REF-}/V_{eREF-}$	Negative external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 3)		0		1.2	V
$(V_{eREF+} - V_{REF-}/V_{eREF-})$	Differential external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 4)		1.4		$V_{AVCC}$	V
$I_{VeREF+}$	Input leakage current	$0V \leq V_{eREF+} \leq V_{AVCC}$	$V_{CC} = 2.2\text{ V}/3\text{ V}$			$\pm 1$	$\mu\text{A}$
$I_{VREF-}/V_{eREF-}$	Input leakage current	$0V \leq V_{eREF-} \leq V_{AVCC}$	$V_{CC} = 2.2\text{ V}/3\text{ V}$			$\pm 1$	$\mu\text{A}$

- NOTES: 1. The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance,  $C_I$ , is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.  
2. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.  
3. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.  
4. The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

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## 12-bit ADC, built-in reference

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT		
V <sub>REF+</sub>	Positive built-in reference voltage output	REF2_5V = 1 for 2.5 V I <sub>VREF+</sub> max ≤ I <sub>VREF+</sub> ≤ I <sub>VREF+</sub> min	V <sub>CC</sub> = 3 V		2.4	2.5	2.6	V
		REF2_5V = 0 for 1.5 V I <sub>VREF+</sub> max ≤ I <sub>VREF+</sub> ≤ I <sub>VREF+</sub> min	V <sub>CC</sub> = 2.2 V/3 V		1.44	1.5	1.56	
AV <sub>CC(min)</sub>	AV <sub>CC</sub> minimum voltage, Positive built-in reference active	REF2_5V = 0, I <sub>VREF+</sub> max ≤ I <sub>VREF+</sub> ≤ I <sub>VREF+</sub> min			2.2		V	
		REF2_5V = 1, I <sub>VREF+</sub> min ≥ I <sub>VREF+</sub> ≥ -0.5mA			2.8			
		REF2_5V = 1, I <sub>VREF+</sub> min ≥ I <sub>VREF+</sub> ≥ -1mA			2.9			
I <sub>VREF+</sub>	Load current out of V <sub>REF+</sub> terminal		V <sub>CC</sub> = 2.2 V		0.01	-0.5	mA	
			V <sub>CC</sub> = 3 V		0.01	-1		
I <sub>L(VREF+)</sub>	Load-current regulation V <sub>REF+</sub> terminal	I <sub>VREF+</sub> = 500 μA +/- 100 μA Analog input voltage ~0.75 V; REF2_5V = 0	V <sub>CC</sub> = 2.2 V		±2		LSB	
			V <sub>CC</sub> = 3 V		±2			
		I <sub>VREF+</sub> = 500 μA ± 100 μA Analog input voltage ~1.25 V; REF2_5V = 1	V <sub>CC</sub> = 3 V		±2		LSB	
I <sub>DL(VREF+)</sub>	Load current regulation V <sub>REF+</sub> terminal	I <sub>VREF+</sub> = 100 μA → 900 μA, C <sub>VREF+</sub> = 5 μF, ax ~0.5 x V <sub>REF+</sub> Error of conversion result ≤ 1 LSB	V <sub>CC</sub> = 3 V		20		ns	
C <sub>VREF+</sub>	Capacitance at pin V <sub>REF+</sub> (see Note 1)	REFON = 1, 0 mA ≤ I <sub>VREF+</sub> ≤ I <sub>VREF+</sub> max	V <sub>CC</sub> = 2.2 V/3 V		5	10	μF	
T <sub>REF+</sub>	Temperature coefficient of built-in reference	I <sub>VREF+</sub> is a constant in the range of 0 mA ≤ I <sub>VREF+</sub> ≤ 1 mA	V <sub>CC</sub> = 2.2 V/3 V		±100		ppm/°C	
t <sub>REFON</sub>	Settle time of internal reference voltage (see Figure 23 and Note 2)	I <sub>VREF+</sub> = 0.5 mA, C <sub>VREF+</sub> = 10 μF, V <sub>REF+</sub> = 1.5 V, V <sub>AVCC</sub> = 2.2 V			17		ms	

- NOTES: 1. The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests uses two capacitors between pins V<sub>REF+</sub> and AV<sub>SS</sub> and V<sub>REF-</sub>/V<sub>eREF-</sub> and AV<sub>SS</sub>: 10 μF tantalum and 100 nF ceramic.  
2. The condition is that the error in a conversion started after t<sub>REFON</sub> is less than ±0.5 LSB. The settling time depends on the external capacitive load.

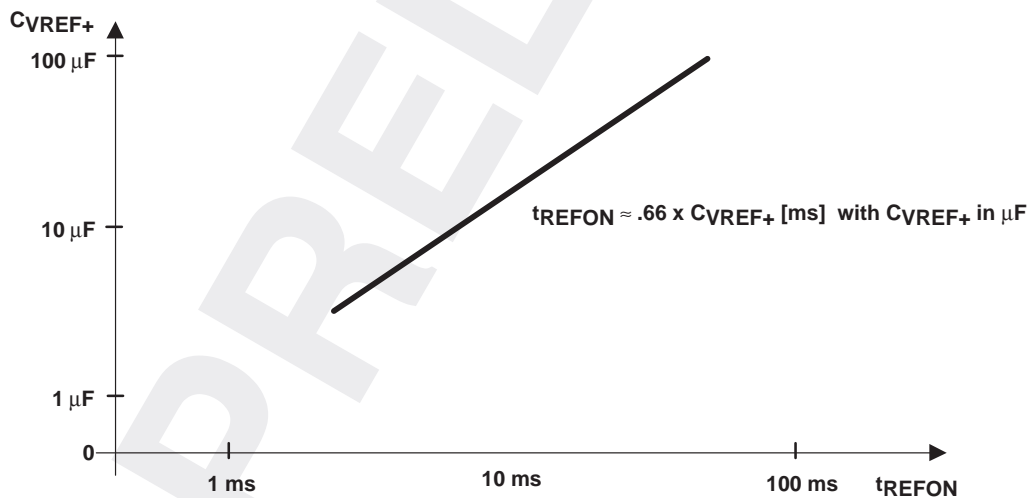


Figure 23. Typical Settling Time of Internal Reference t<sub>REFON</sub> vs External Capacitor on V<sub>REF+</sub>

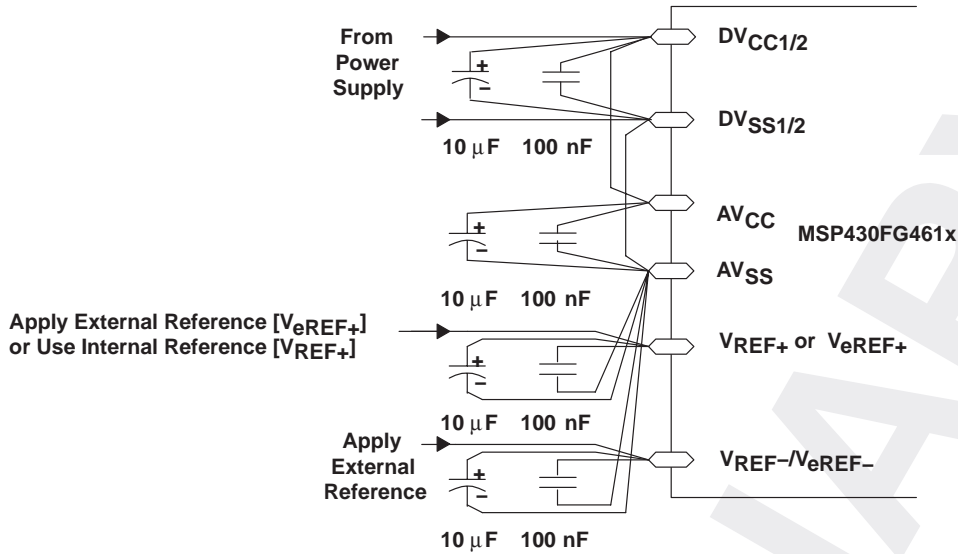


Figure 24. Supply Voltage and Reference Voltage Design  $V_{REF-}/V_{REF+}$  External Supply

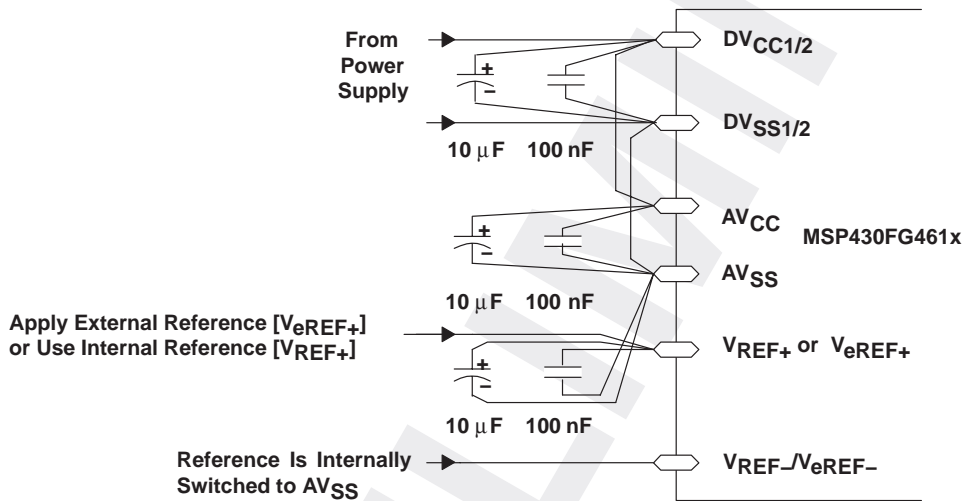


Figure 25. Supply Voltage and Reference Voltage Design  $V_{REF-}/V_{REF+} = AV_{SS}$ , Internally Connected

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## 12-bit ADC, timing parameters

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
f <sub>ADC12CLK</sub>	For specified performance of ADC12 linearity parameters V <sub>CC</sub> = 2.2V/3 V	0.45	5	6.3	MHz
f <sub>ADC12OSC</sub>	Internal ADC12 oscillator ADC12DIV=0, f <sub>ADC12CLK</sub> =f <sub>ADC12OSC</sub> V <sub>CC</sub> = 2.2 V/ 3 V	3.7	5	6.3	MHz
t <sub>CONVERT</sub>	Conversion time C <sub>VREF+</sub> ≥ 5 μF, Internal oscillator, f <sub>ADC12OSC</sub> = 3.7 MHz to 6.3 MHz V <sub>CC</sub> = 2.2 V/ 3 V	2.06		3.51	μs
	External f <sub>ADC12CLK</sub> from ACLK, MCLK or SMCLK: ADC12SSEL ≠ 0		13×ADC12DIV× 1/f <sub>ADC12CLK</sub>		μs
t <sub>ADC12ON</sub>	Turn on settling time of the ADC (see Note 1)			100	ns
t <sub>Sample</sub>	Sampling time R <sub>S</sub> = 400 Ω, R <sub>I</sub> = 1000 Ω, C <sub>I</sub> = 30 pF, τ = [R <sub>S</sub> + R <sub>I</sub> ] × C <sub>I</sub> (see Note 2)	V <sub>CC</sub> = 3 V	1220		ns
		V <sub>CC</sub> = 2.2 V	1400		

- NOTES: 1. The condition is that the error in a conversion started after t<sub>ADC12ON</sub> is less than ±0.5 LSB. The reference and input signal are already settled.  
2. Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:  
t<sub>Sample</sub> = ln(2<sup>n+1</sup>) × (R<sub>S</sub> + R<sub>I</sub>) × C<sub>I</sub> + 800 ns where n = ADC resolution = 12, R<sub>S</sub> = external source resistance.

## 12-bit ADC, linearity parameters

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT	
E <sub>I</sub>	Integral linearity error 1.4 V ≤ (V <sub>eREF+</sub> - V <sub>REF-</sub> - V <sub>eREF-</sub> ) min ≤ 1.6 V	V <sub>CC</sub> = 2.2 V/3 V		±2	LSB	
	1.6 V < (V <sub>eREF+</sub> - V <sub>REF-</sub> - V <sub>eREF-</sub> ) min ≤ [V <sub>AVCC</sub> ]			±1.7		
E <sub>D</sub>	Differential linearity error (V <sub>eREF+</sub> - V <sub>REF-</sub> - V <sub>eREF-</sub> ) min ≤ (V <sub>eREF+</sub> - V <sub>REF-</sub> - V <sub>eREF-</sub> ), C <sub>VREF+</sub> = 10 μF (tantalum) and 100 nF (ceramic)	V <sub>CC</sub> = 2.2 V/3 V		±1	LSB	
E <sub>O</sub>	Offset error (V <sub>eREF+</sub> - V <sub>REF-</sub> - V <sub>eREF-</sub> ) min ≤ (V <sub>eREF+</sub> - V <sub>REF-</sub> - V <sub>eREF-</sub> ), Internal impedance of source R <sub>S</sub> < 100 Ω, C <sub>VREF+</sub> = 10 μF (tantalum) and 100 nF (ceramic)	V <sub>CC</sub> = 2.2 V/3 V		±2	±4	LSB
E <sub>G</sub>	Gain error (V <sub>eREF+</sub> - V <sub>REF-</sub> - V <sub>eREF-</sub> ) min ≤ (V <sub>eREF+</sub> - V <sub>REF-</sub> - V <sub>eREF-</sub> ), C <sub>VREF+</sub> = 10 μF (tantalum) and 100 nF (ceramic)	V <sub>CC</sub> = 2.2 V/3 V		±1.1	±2	LSB
E <sub>T</sub>	Total unadjusted error (V <sub>eREF+</sub> - V <sub>REF-</sub> - V <sub>eREF-</sub> ) min ≤ (V <sub>eREF+</sub> - V <sub>REF-</sub> - V <sub>eREF-</sub> ), C <sub>VREF+</sub> = 10 μF (tantalum) and 100 nF (ceramic)	V <sub>CC</sub> = 2.2 V/3 V		±2	±5	LSB

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, temperature sensor and built-in  $V_{MID}$

PARAMETER	TEST CONDITIONS	$V_{CC}$	MIN	NOM	MAX	UNIT
$I_{SENSOR}$	Operating supply current into $AV_{CC}$ terminal (see Note 1)	REFON = 0, INCH = 0Ah, ADC12ON=NA, $T_A = 25^\circ C$	2.2 V	40	120	$\mu A$
			3 V	60	160	
$V_{SENSOR}$	(see Note 2)	ADC12ON = 1, INCH = 0Ah, $T_A = 0^\circ C$	2.2 V/ 3 V	986		mV
$TC_{SENSOR}$		ADC12ON = 1, INCH = 0Ah	2.2 V/ 3 V	3.55±3%		mV/°C
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected (see Note 3)	ADC12ON = 1, INCH = 0Ah, Error of conversion result $\leq 1$ LSB	2.2 V	30		$\mu s$
			3 V	30		
$I_{VMID}$	Current into divider at channel 11 (see Note 4)	ADC12ON = 1, INCH = 0Bh,	2.2 V		NA	$\mu A$
			3 V		NA	
$V_{MID}$	$AV_{CC}$ divider at channel 11	ADC12ON = 1, INCH = 0Bh, $V_{MID}$ is $-0.5 \times V_{AVCC}$	2.2 V	1.1	1.1±0.04	V
			3 V	1.5	1.50±0.04	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (see Note 5)	ADC12ON = 1, INCH = 0Bh, Error of conversion result $\leq 1$ LSB	2.2 V	1400		ns
			3 V	1220		

- NOTES: 1. The sensor current  $I_{SENSOR}$  is consumed if (ADC12ON = 1 and REFON=1), or (ADC12ON=1 AND INCH=0Ah and sample signal is high). When REFON = 1,  $I_{SENSOR}$  is already included in  $I_{REF+}$ .
2. The temperature sensor offset can be as much as  $\pm 20^\circ C$ . A single-point calibration is recommended in order to minimize the offset error of the built-in temperature sensor.
3. The typical equivalent impedance of the sensor is 51 k $\Omega$ . The sample time required includes the sensor-on time  $t_{SENSOR(on)}$ .
4. No additional current is needed. The  $V_{MID}$  is used during sampling.
5. The on-time  $t_{VMID(on)}$  is included in the sampling time  $t_{VMID(sample)}$ ; no additional on time is needed.

12-bit DAC, supply specifications

PARAMETER	TEST CONDITIONS	$V_{CC}$	MIN	TYP	MAX	UNIT
$AV_{CC}$	Analog supply voltage	$AV_{CC} = DV_{CC}$ , $AV_{SS} = DV_{SS} = 0 V$	2.20		3.60	V
$I_{DD}$	Supply Current: Single DAC Channel (see Notes 1 and 2)	DAC12AMPx=2, DAC12IR=0, DAC12_xDAT=0800h	2.2V/3V	50	110	$\mu A$
		DAC12AMPx=2, DAC12IR=1, DAC12_xDAT=0800h, $V_{eREF+}=V_{REF+}= AV_{CC}$	2.2V/3V	50	110	
		DAC12AMPx=5, DAC12IR=1, DAC12_xDAT=0800h, $V_{eREF+}=V_{REF+}= AV_{CC}$	2.2V/3V	200	440	
		DAC12AMPx=7, DAC12IR=1, DAC12_xDAT=0800h, $V_{eREF+}=V_{REF+}= AV_{CC}$	2.2V/3V	700	1500	
PSRR	Power supply rejection ratio (see Notes 3 and 4)	DAC12_xDAT = 800h, $V_{REF} = 1.5 V$ $\Delta AV_{CC} = 100mV$	2.2V	70		dB
		DAC12_xDAT = 800h, $V_{REF} = 1.5 V$ or 2.5 V $\Delta AV_{CC} = 100mV$	3V			

- NOTES: 1. No load at the output pin, DAC12\_0 or DAC12\_1, assuming that the control bits for the shared pins are set properly.
2. Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications.
3.  $PSRR = 20 \cdot \log\{\Delta AV_{CC} / \Delta V_{DAC12\_xOUT}\}$ .
4.  $V_{REF}$  is applied externally. The internal reference is not used.

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## 12-bit DAC, linearity specifications (see Figure 26)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
Resolution		(12-bit Monotonic)		12			bits
INL	Integral nonlinearity (see Note 1)	V <sub>ref</sub> = 1.5 V DAC12AMPx = 7, DAC12IR = 1	2.2V		±2.0	±8.0	LSB
		V <sub>ref</sub> = 2.5 V DAC12AMPx = 7, DAC12IR = 1	3V				
DNL	Differential nonlinearity (see Note 1)	V <sub>ref</sub> = 1.5 V DAC12AMPx = 7, DAC12IR = 1	2.2V		±0.4	±1.0	LSB
		V <sub>ref</sub> = 2.5 V DAC12AMPx = 7, DAC12IR = 1	3V				
EO	Offset voltage w/o calibration (see Notes 1, 2)	V <sub>ref</sub> = 1.5 V DAC12AMPx = 7, DAC12IR = 1	2.2V			±21	mV
		V <sub>ref</sub> = 2.5 V DAC12AMPx = 7, DAC12IR = 1	3V				
	Offset voltage with calibration (see Notes 1, 2)	V <sub>ref</sub> = 1.5 V DAC12AMPx = 7, DAC12IR = 1	2.2V				
		V <sub>ref</sub> = 2.5 V DAC12AMPx = 7, DAC12IR = 1	3V				
dE(O)/dT	Offset error temperature coefficient (see Note 1)		2.2V/3V		±30	μV/C	
EG	Gain error (see Note 1)	V <sub>REF</sub> = 1.5 V	2.2V		±3.50	% FSR	
		V <sub>REF</sub> = 2.5 V	3V				
dE(G)/dT	Gain temperature coefficient (see Note 1)		2.2V/3V		10	ppm of FSR/°C	
t <sub>Offset_Cal</sub>	Time for offset calibration (see Note 3)	DAC12AMPx=2	2.2V/3V			100	ms
		DAC12AMPx=3,5	2.2V/3V			32	
		DAC12AMPx=4,6,7	2.2V/3V			6	

- NOTES: 1. Parameters calculated from the best-fit curve from 0x0A to 0xFFF. The best-fit curve method is used to deliver coefficients "a" and "b" of the first order equation:  $y = a + b \cdot x$ .  $V_{DAC12\_xOUT} = E_O + (1 + E_G) \cdot (V_{eREF+}/4095) \cdot DAC12\_xDAT$ , DAC12IR = 1.
2. The offset calibration works on the output operational amplifier. Offset Calibration is triggered setting bit DAC12CALON
3. The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx = {0, 1}. It is recommended that the DAC12 module be configured prior to initiating calibration. Port activity during calibration may effect accuracy and is not recommended.

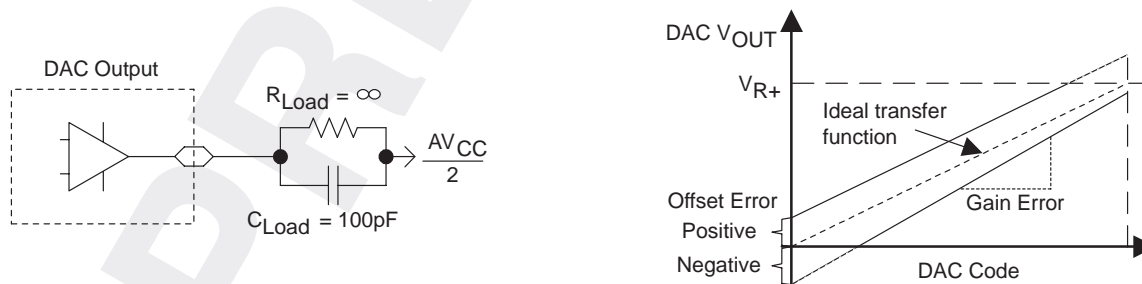
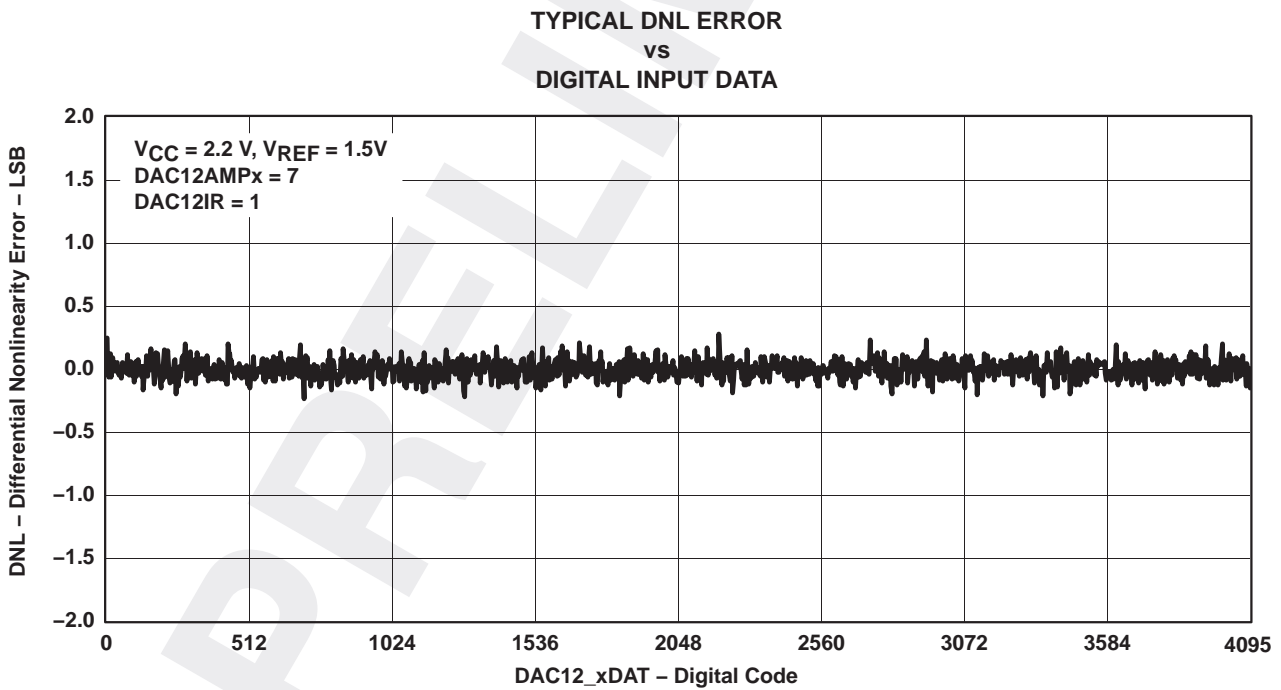
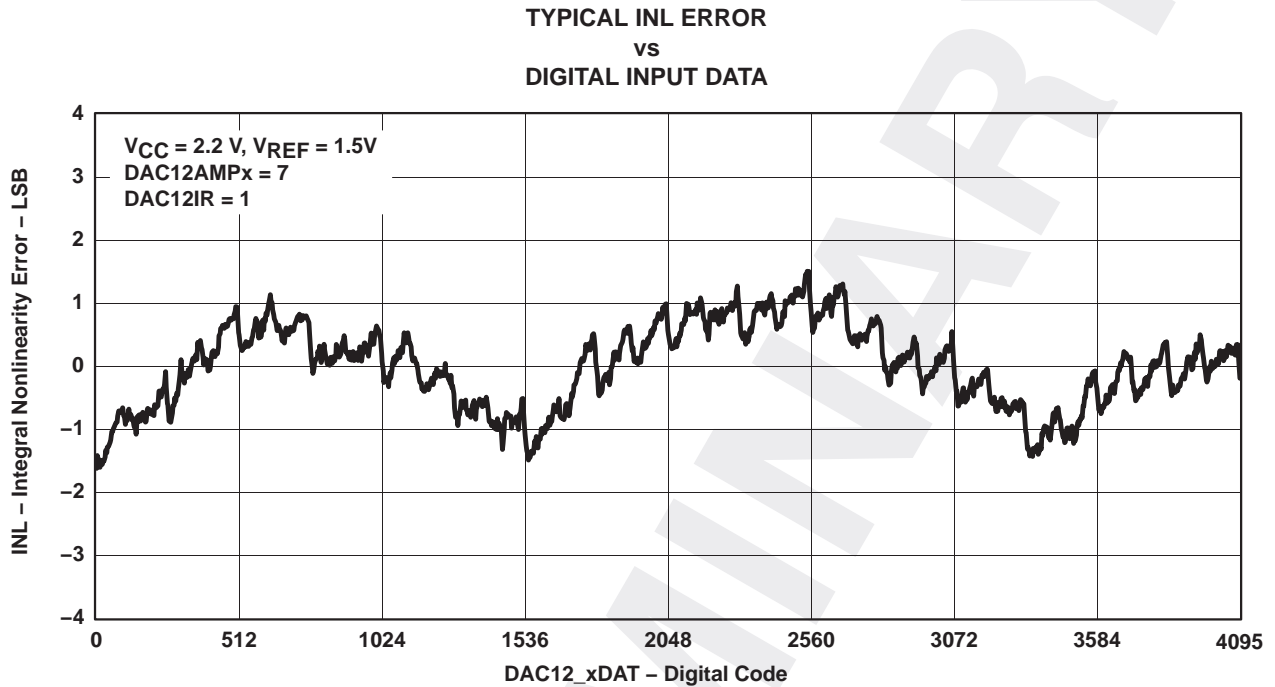


Figure 26. Linearity Test Load Conditions and Gain/Offset Definition



electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, linearity specifications (continued)



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## 12-bit DAC, output specifications

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>O</sub>  Output voltage range (see Note 1, Figure 29)	No Load, V <sub>REF+</sub> = AV <sub>CC</sub> , DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2V/3V	0		0.005	V
	No Load, V <sub>REF+</sub> = AV <sub>CC</sub> , DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7	2.2V/3V	AV <sub>CC</sub> -0.05		AV <sub>CC</sub>	
	R <sub>Load</sub> = 3 kΩ, V <sub>REF+</sub> = AV <sub>CC</sub> , DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2V/3V	0		0.1	
	R <sub>Load</sub> = 3 kΩ, V <sub>REF+</sub> = AV <sub>CC</sub> , DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7	2.2V/3V	AV <sub>CC</sub> -0.13		AV <sub>CC</sub>	
C <sub>L</sub> (DAC12) Max DAC12 load capacitance		2.2V/3V			100	pF
I <sub>L</sub> (DAC12) Max DAC12 load current		2.2V	-0.5		+0.5	mA
		3V	-1.0		+1.0	
R <sub>O/P</sub> (DAC12) Output Resistance (see Figure 29)	R <sub>Load</sub> = 3 kΩ, V <sub>O/P</sub> (DAC12) < 0.3 V, DAC12AMPx = 2, DAC12_xDAT = 0h	2.2V/3V		150	250	Ω
	R <sub>Load</sub> = 3 kΩ, V <sub>O/P</sub> (DAC12) > AV <sub>CC</sub> -0.3 V DAC12_xDAT = 0FFFh	2.2V/3V		150	250	
	R <sub>Load</sub> = 3 kΩ, 0.3V ≤ V <sub>O/P</sub> (DAC12) ≤ AV <sub>CC</sub> - 0.3V	2.2V/3V		1	4	

NOTES: 1. Data is valid after the offset calibration of the output amplifier.

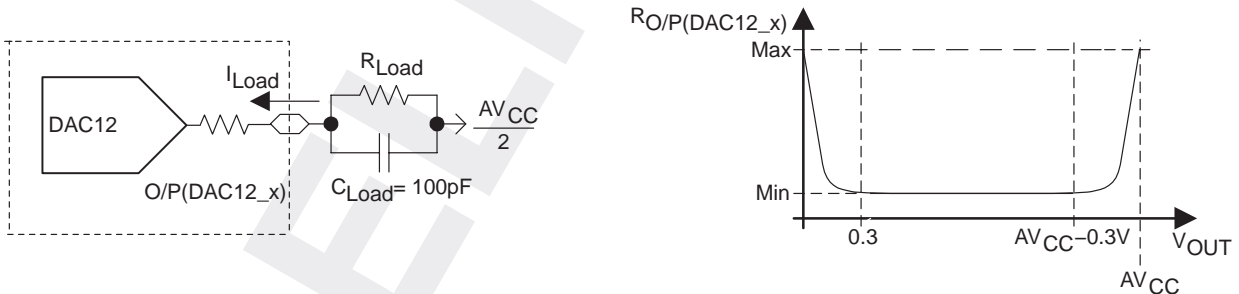


Figure 29. DAC12\_x Output Resistance Tests

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

12-bit DAC, reference input specifications

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT	
V <sub>REF+</sub>	Reference input voltage range	DAC12IR=0, (see Notes 1 and 2)		AV <sub>CC</sub> /3	AV <sub>CC</sub> +0.2	V	
		DAC12IR=1, (see Notes 3 and 4)	2.2V/3V	AV <sub>CC</sub>	AV <sub>CC</sub> +0.2		
R <sub>i</sub> (V <sub>REF+</sub> ), R <sub>i</sub> (V <sub>REF+</sub> )	Reference input resistance	DAC12_0 IR=DAC12_1 IR =0	2.2V/3V	20		MΩ	
		DAC12_0 IR=1, DAC12_1 IR = 0	2.2V/3V	40	48	56	kΩ
		DAC12_0 IR=0, DAC12_1 IR = 1	2.2V/3V				
		DAC12_0 IR=DAC12_1 IR =1 DAC12_0 SREFx = DAC12_1 SREFx (see Note 5)	2.2V/3V	20	24	28	kΩ

- NOTES: 1. For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AV<sub>CC</sub>).  
 2. The maximum voltage applied at reference input voltage terminal V<sub>REF+</sub> = [AV<sub>CC</sub> - V<sub>E(O)</sub>] / [3\*(1 + E<sub>G</sub>)].  
 3. For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AV<sub>CC</sub>).  
 4. The maximum voltage applied at reference input voltage terminal V<sub>REF+</sub> = [AV<sub>CC</sub> - V<sub>E(O)</sub>] / (1 + E<sub>G</sub>).  
 5. When DAC12IR = 1 and DAC12SREFx = 0 or 1 for both channels, the reference input resistive dividers for each DAC are in parallel reducing the reference input resistance.

12-bit DAC, dynamic specifications; V<sub>ref</sub> = V<sub>CC</sub>, DAC12IR = 1 (see Figure 30 and Figure 31)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
t <sub>ON</sub>	DAC12_xDAT = 800h, Error <sub>V(O)</sub> < ±0.5 LSB (see Note 1, Figure 30)	DAC12AMPx=0 → {2, 3, 4}	2.2V/3V	60	120	μs
		DAC12AMPx=0 → {5, 6}	2.2V/3V	15	30	
		DAC12AMPx=0 → 7	2.2V/3V	6	12	
t <sub>S(FS)</sub>	DAC12_xDAT = 80h → F7Fh → 80h	DAC12AMPx=2	2.2V/3V	100	200	μs
		DAC12AMPx=3,5	2.2V/3V	40	80	
		DAC12AMPx=4,6,7	2.2V/3V	15	30	
t <sub>S(C-C)</sub>	DAC12_xDAT = 3F8h → 408h → 3F8h BF8h → C08h → BF8h	DAC12AMPx=2	2.2V/3V	5		μs
		DAC12AMPx=3,5	2.2V/3V	2		
		DAC12AMPx=4,6,7	2.2V/3V	1		
SR	DAC12_xDAT = 80h → F7Fh → 80h (see Note 2)	DAC12AMPx=2	2.2V/3V	0.05	0.12	V/μs
		DAC12AMPx=3,5	2.2V/3V	0.35	0.7	
		DAC12AMPx=4,6,7	2.2V/3V	1.5	2.7	
Glitch energy: full-scale	DAC12_xDAT = 80h → F7Fh → 80h	DAC12AMPx=2	2.2V/3V	600		nV-s
		DAC12AMPx=3,5	2.2V/3V	150		
		DAC12AMPx=4,6,7	2.2V/3V	30		

- NOTES: 1. R<sub>Load</sub> and C<sub>Load</sub> connected to AV<sub>SS</sub> (not AV<sub>CC</sub>/2) in Figure 30.  
 2. Slew rate applies to output voltage steps >= 200mV.

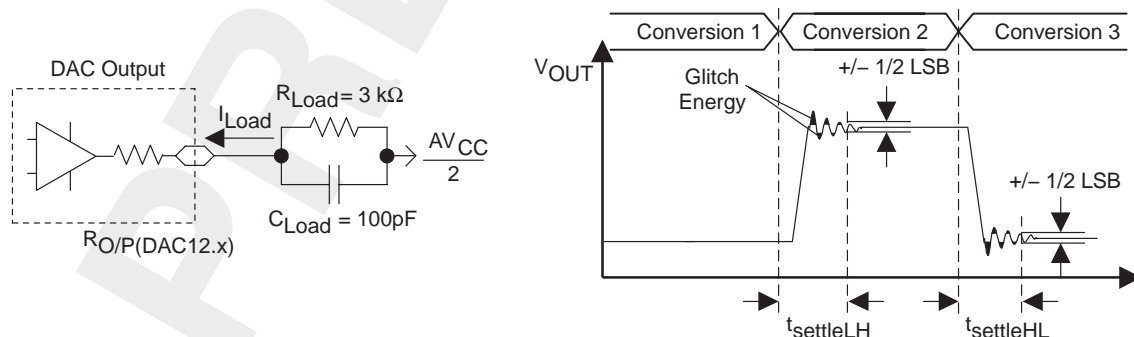


Figure 30. Settling Time and Glitch Energy Testing

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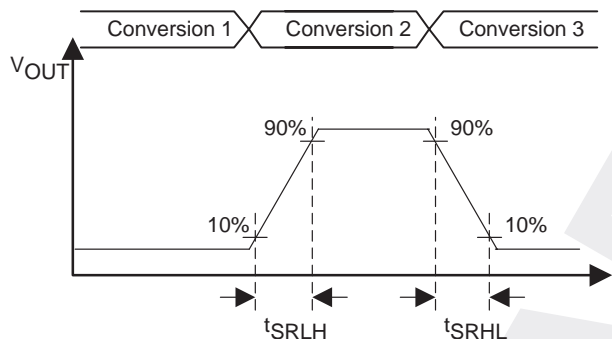


Figure 31. Slew Rate Testing

12-bit DAC, dynamic specifications continued ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
3-dB bandwidth, BW <sub>-3dB</sub> V <sub>DC</sub> =1.5V, V <sub>AC</sub> =0.1V <sub>PP</sub> (see Figure 32)	DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2V/3V	40			kHz
	DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2V/3V	180			
	DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2V/3V	550			
Channel-to-channel crosstalk (see Note 1 and Figure 33)	DAC12_0DAT = 800h, No Load, DAC12_1DAT = 80h<->F7Fh, R <sub>Load</sub> = 3kΩ f <sub>DAC12_1OUT</sub> = 10kHz @ 50/50 duty cycle	2.2V/3V		-80		dB
	DAC12_0DAT = 80h<->F7Fh, R <sub>Load</sub> = 3kΩ, DAC12_1DAT = 800h, No Load f <sub>DAC12_0OUT</sub> = 10kHz @ 50/50 duty cycle	2.2V/3V		-80		

NOTES: 1. R<sub>LOAD</sub> = 3 kΩ, C<sub>LOAD</sub> = 100 pF

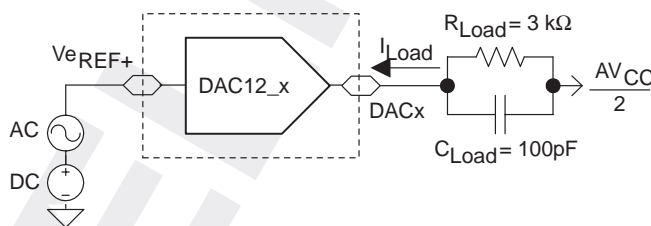


Figure 32. Test Conditions for 3-dB Bandwidth Specification

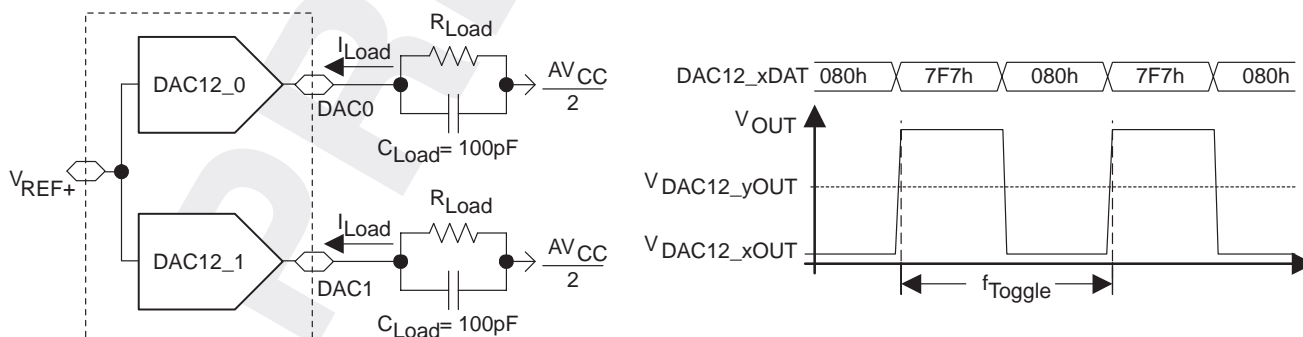


Figure 33. Crosstalk Test Conditions

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

operational amplifier OA, supply specifications

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>CC</sub>	Supply voltage		—	2.2		3.6	V
I <sub>CC</sub>	Supply current (see Note 1)	Fast Mode, OARRIP OFF	2.2 V/3 V		180	290	μA
		Medium Mode, OARRIP OFF	2.2 V/3 V		110	190	
		Slow Mode, OARRIP OFF	2.2 V/3 V		50	80	
		Fast Mode, OARRIP ON	2.2 V/3 V		300	490	
		Medium Mode, OARRIP ON	2.2 V/3 V		190	350	
		Slow Mode, OARRIP ON	2.2 V/3 V		90	190	
PSRR	Power supply rejection ratio	Non-inverting	2.2 V/3 V		70		dB

NOTES: 1. P6SEL.x = 1 for each corresponding pin when used in OA input or OA output mode.

operational amplifier OA, input/output specifications

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT	
V <sub>I/P</sub>	Voltage supply, I/P	OARRIP OFF	—	−0.1		V <sub>CC</sub> −1.2	V	
		OARRIP ON	—	−0.1		V <sub>CC</sub> +0.1	V	
I <sub>lkg</sub>	Input leakage current, I/P (see Notes 1 and 2)	T <sub>A</sub> = −40 to +55°C	—	−5	±0.5	5	nA	
		T <sub>A</sub> = +55 to +85°C	—	−20	±5	20	nA	
V <sub>n</sub>	Voltage noise density, I/P	Fast Mode	f <sub>V(I/P)</sub> = 1 kHz			50	nV/√Hz	
				Medium Mode		80		
				Slow Mode		140		
		Fast Mode		f <sub>V(I/P)</sub> = 10 kHz				30
					Medium Mode			50
					Slow Mode			65
V <sub>IO</sub>	Offset voltage, I/P		2.2 V/3 V				±10	mV
	Offset temperature drift, I/P	see Note 3	2.2 V/3 V			±10		μV/°C
	Offset voltage drift with supply, I/P	0.3V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> −0.3V ΔV <sub>CC</sub> ≤ ±10%, T <sub>A</sub> = 25°C	2.2 V/3 V				±1.5	mV/V
V <sub>OH</sub>	High-level output voltage, O/P	Fast Mode, I <sub>SOURCE</sub> ≤ −500μA	2.2 V	V <sub>CC</sub> −0.2		V <sub>CC</sub>	V	
		Slow Mode, I <sub>SOURCE</sub> ≤ −150μA	3 V	V <sub>CC</sub> −0.1		V <sub>CC</sub>	V	
V <sub>OL</sub>	Low-level output voltage, O/P	Fast Mode, I <sub>SOURCE</sub> ≤ +500μA	2.2 V	V <sub>SS</sub>		0.2	V	
		Slow Mode, I <sub>SOURCE</sub> ≤ +150μA	3 V	V <sub>SS</sub>		0.1	V	
R <sub>O/P</sub> (OAx)	Output Resistance (see Figure 34 and Note 4)	R <sub>Load</sub> = 3 kΩ, C <sub>Load</sub> = 50pF, OARRIP ON, V <sub>O/P</sub> (OAx) < 0.2 V	2.2 V/3 V		150	250	Ω	
		R <sub>Load</sub> = 3 kΩ, C <sub>Load</sub> = 50pF, OARRIP ON, V <sub>O/P</sub> (OAx) > AV <sub>CC</sub> − 0.2 V	2.2 V/3 V		150	250		
		R <sub>Load</sub> = 3 kΩ, C <sub>Load</sub> = 50pF, OARRIP ON, 0.2 V ≤ V <sub>O/P</sub> (OAx) ≤ AV <sub>CC</sub> − 0.2 V	2.2 V/3 V		0.1	4		
CMRR	Common-mode rejection ratio	Non-inverting	2.2 V/3 V		70		dB	

NOTES: 1. ESD damage can degrade input current leakage.  
2. The input bias current is overridden by the input leakage current.  
3. Calculated using the box method.  
4. Specification valid for voltage-follower OAx configuration.

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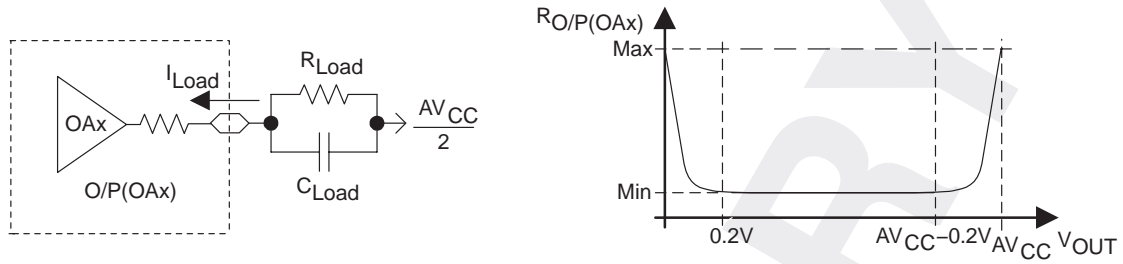


Figure 34. OAx Output Resistance Tests

## operational amplifier OA, dynamic specifications

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
SR	Slew rate	Fast Mode	—		1.2		V/μs
		Medium Mode	—		0.8		
		Slow Mode	—		0.3		
	Open-loop voltage gain		—		100		dB
φ <sub>m</sub>	Phase margin	C <sub>L</sub> = 50 pF	—		60		deg
	Gain margin	C <sub>L</sub> = 50 pF	—		20		dB
GBW	Gain-Bandwidth Product (see Figure 35 and Figure 36)	Non-inverting, Fast Mode, R <sub>L</sub> = 47kΩ, C <sub>L</sub> = 50pF	2.2 V/3 V		2.2		MHz
		Non-inverting, Medium Mode, R <sub>L</sub> = 300kΩ, C <sub>L</sub> = 50pF	2.2 V/3 V		1.4		
		Non-inverting, Slow Mode, R <sub>L</sub> = 300kΩ, C <sub>L</sub> = 50pF	2.2 V/3 V		0.5		
t <sub>en(on)</sub>	Enable time on	t <sub>on</sub> , non-inverting, Gain = 1	2.2 V/3 V		10	20	μs
t <sub>en(off)</sub>	Enable time off		2.2 V/3 V			1	μs

TYPICAL OPEN-LOOP GAIN vs FREQUENCY

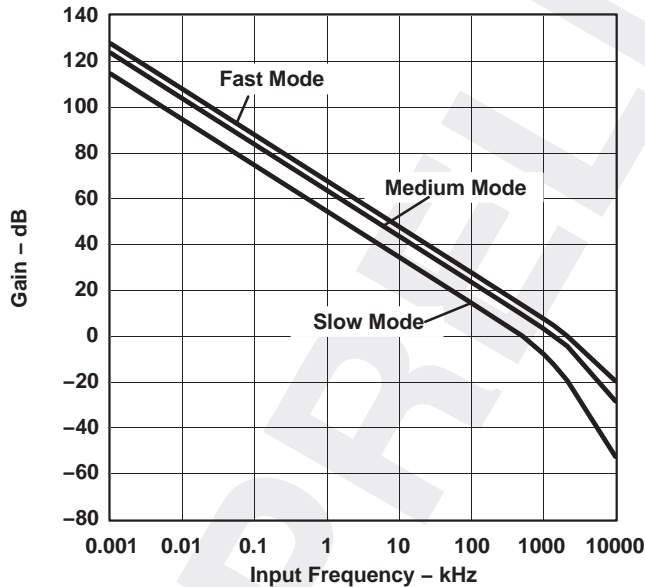


Figure 35

TYPICAL PHASE vs FREQUENCY

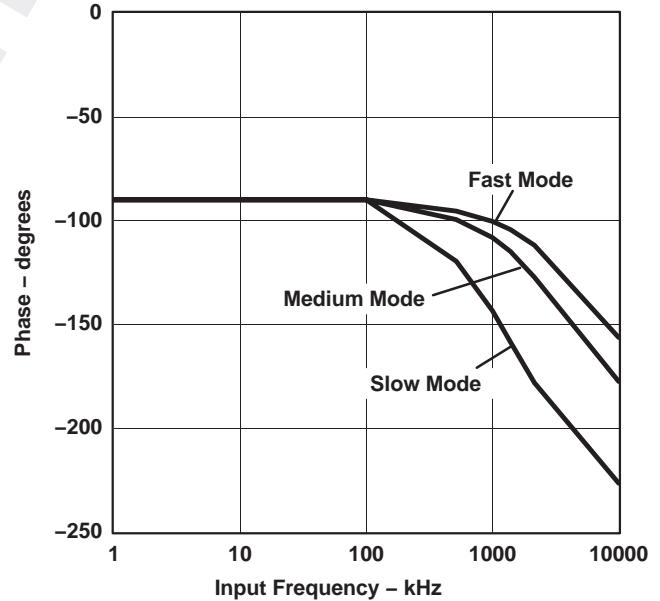


Figure 36

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

Flash Memory

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>CC(PGM/ERASE)</sub>	Program and Erase supply voltage			2.7		3.6	V
f <sub>FTG</sub>	Flash Timing Generator frequency			257		476	kHz
I <sub>PGM</sub>	Supply current from DV <sub>CC</sub> during program		2.7 V/ 3.6 V		3	5	mA
I <sub>ERASE</sub>	Supply current from DV <sub>CC</sub> during erase	see Note 3	2.7 V/ 3.6 V		3	7	mA
I <sub>GMERASE</sub>	Supply current from DV <sub>CC</sub> during global mass erase	see Note 4	2.7 V/ 3.6 V		6	14	mA
t <sub>CPT</sub>	Cumulative program time	see Note 1	2.7 V/ 3.6 V			10	ms
t <sub>CMErase</sub>	Cumulative mass erase time		2.7 V/ 3.6 V	20			ms
	Program/Erase endurance			10 <sup>4</sup>	10 <sup>5</sup>		cycles
t <sub>Retention</sub>	Data retention duration	T <sub>J</sub> = 25°C		100			years
t <sub>Word</sub>	Word or byte program time	see Note 2			30		t <sub>FTG</sub>
t <sub>Block, 0</sub>	Block program time for 1 <sup>st</sup> byte or word				25		
t <sub>Block, 1-63</sub>	Block program time for each additional byte or word				18		
t <sub>Block, End</sub>	Block program end-sequence wait time				6		
t <sub>Mass Erase</sub>	Mass erase time				10593		
t <sub>Global Mass Erase</sub>	Global mass erase time				10593		
t <sub>Seg Erase</sub>	Segment erase time				4819		

- NOTES: 1. The cumulative program time must not be exceeded during a block-write operation. This parameter is only relevant if the block write feature is used.  
 2. These values are hardwired into the Flash Controller's state machine (t<sub>FTG</sub> = 1/f<sub>FTG</sub>).  
 3. Lower 64-KB or upper 64-KB Flash memory erased.  
 4. All Flash memory erased.

JTAG Interface

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
f <sub>TCK</sub>	TCK input frequency	see Note 1	2.2 V	0		5	MHz
			3 V	0		10	MHz
R <sub>Internal</sub>	Internal pull-up resistance on TMS, TCK, TDI/TCLK	see Note 2	2.2 V/ 3 V	25	60	90	kΩ

- NOTES: 1. f<sub>TCK</sub> may be restricted to meet the timing requirements of the module selected.  
 2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

JTAG Fuse (see Note 1)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>CC(FB)</sub>	Supply voltage during fuse-blow condition	T <sub>A</sub> = 25°C		2.5			V
V <sub>FB</sub>	Voltage level on TDI/TCLK for fuse-blow: F versions			6		7	V
I <sub>FB</sub>	Supply current into TDI/TCLK during fuse blow					100	mA
t <sub>FB</sub>	Time to blow fuse					1	ms

- NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

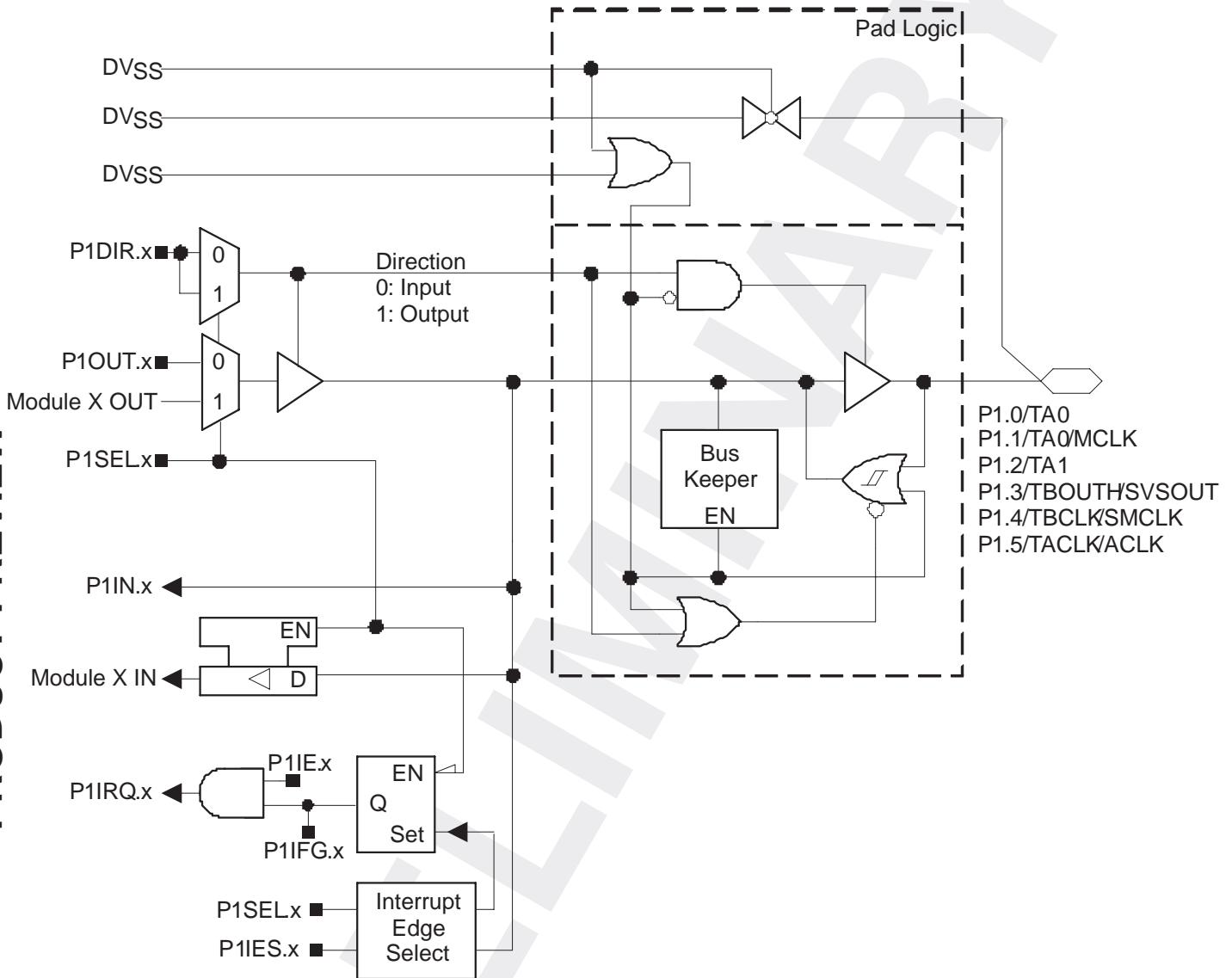
# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## input/output schematic

### Port P1, P1.0 to P1.5, input/output with Schmitt-trigger

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Note: x = 0,1,2,3,4,5

### Port P1 (P1.0 to P1.5) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TA0	0	P1.0 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.1/TA0/MCLK	1	P1.1 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0B	0	1
		MCLK	1	1



Port P1 (P1.0 to P1.5) pin functions (continued)

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P1DIR.x	P1SEL.x
P1.2/TA1	2	P1.2 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI1A	0	1
		Timer_A3.TA1	1	1
P1.3/TBOUTH/SVSOUT	3	P1.3 (I/O)	I: 0; O: 1	0
		Timer_B7.TBOUTH	0	1
		SVSOUT	1	1
P1.4/TBCLK/SMCLK	4	P1.4 (I/O)	I: 0; O: 1	0
		Timer_B7.TBCLK	0	1
		SMCLK	1	1
P1.5/TACLK/ACLK	5	P1.5 (I/O)	I: 0; O: 1	0
		Timer_A3.TACLK	0	1
		ACLK	1	1

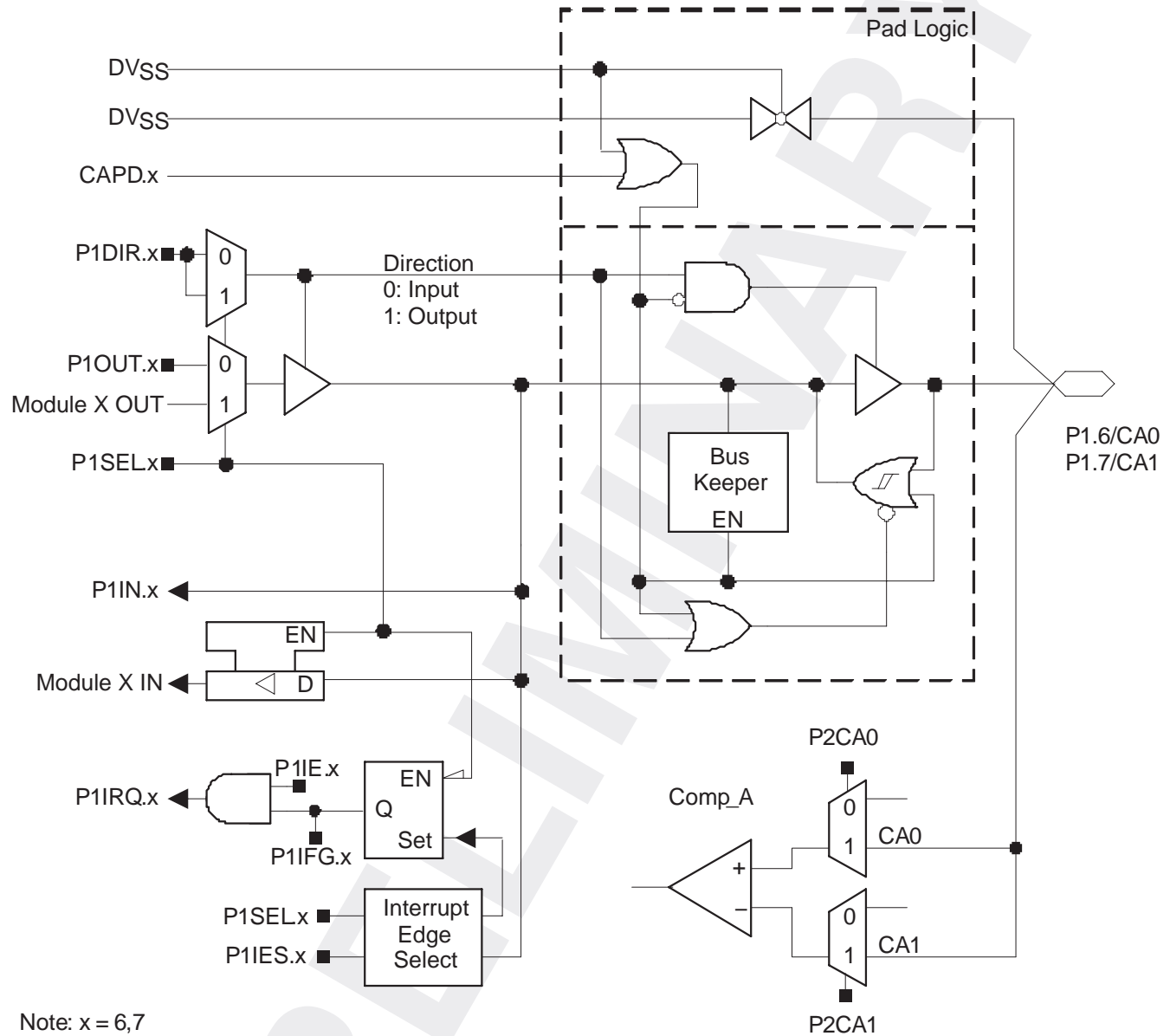
PRODUCT PREVIEW

# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## input/output schematic (continued)

### Port P1, P1.6, P1.7, input/output with Schmitt-trigger



Note: x = 6,7

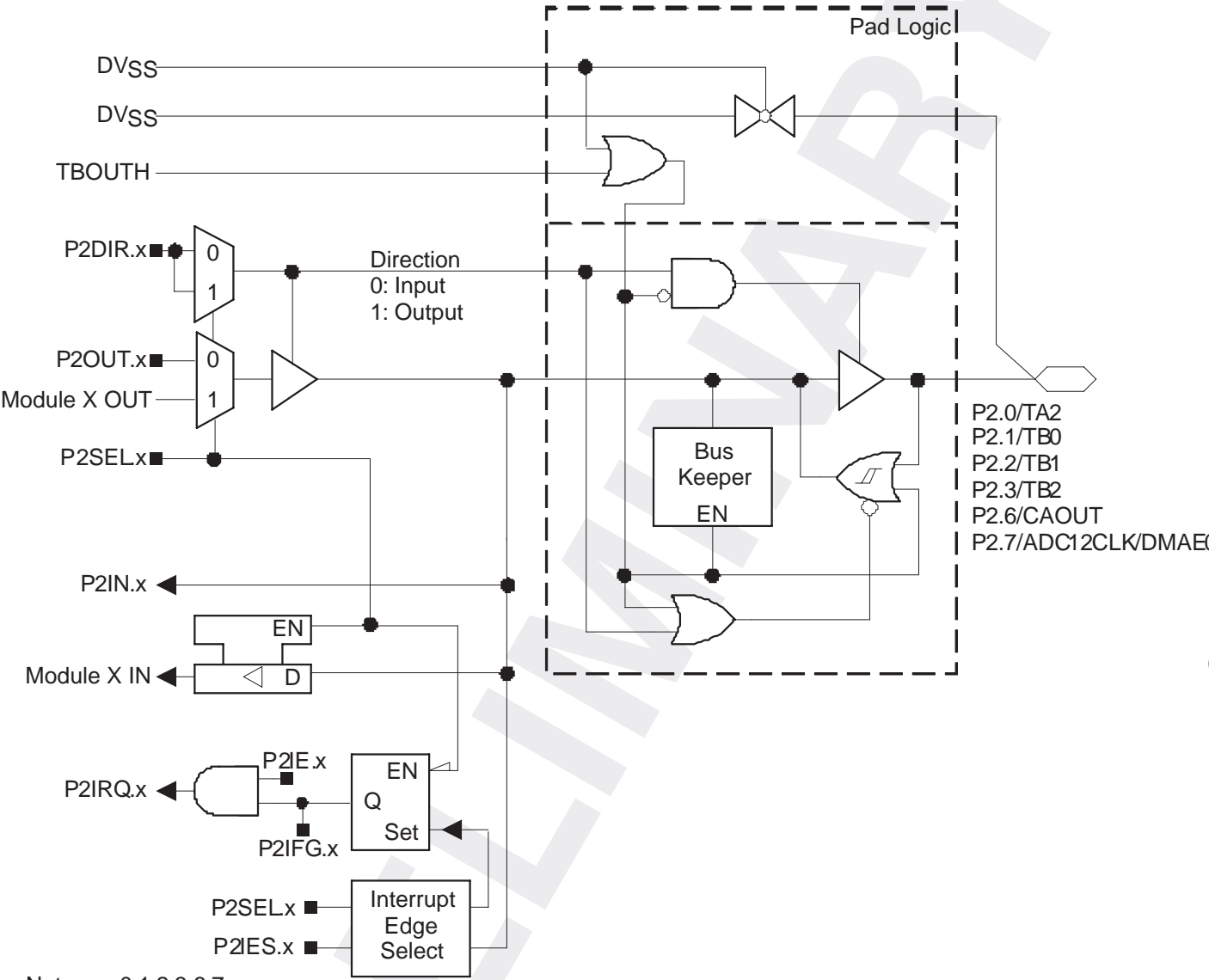
### Port P1 (P1.6 and P1.7) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			CAPD.x	P1DIR.x	P1SEL.x
P1.6/CA0	6	P1.6 (I/O)	0	I: 0; O: 1	0
		CA0	1	X	X
P1.7/CA1	7	P1.6 (I/O)	0	I: 0; O: 1	0
		CA0	1	X	X

NOTES: 1. X: Don't care.

input/output schematic (continued)

port P2, P2.0 to P2.3, P2.6 to P2.7, input/output with Schmitt-trigger



Note: x = 0,1,2,3,6,7

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# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## Port P2 (P2.0, P2.1, P2.2, P2.3, P2.6 and P2.7) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.0/TA2	0	P2.0 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI2A	0	1
		Timer_A3.TA2	1	1
P2.1/TB0	1	P2.1 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI0A and Timer_B7.CCI0B	0	1
		Timer_B7.TB0 (see Note 1)	1	1
P2.2/TB1	2	P2.2 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI1A and Timer_B7.CCI1B	0	1
		Timer_B7.TB1 (see Note 1)	1	1
P2.3/TB3	3	P2.3 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI2A and Timer_B7.CCI2B	0	1
		Timer_B7.TB3 (see Note 1)	1	1
P2.6/CAOUT	6	P2.6 (I/O)	I: 0; O: 1	0
		CAOUT	1	1
P2.7/ADC12CLK/DMAE0	7	P2.7 (I/O)	I: 0; O: 1	0
		ADC12CLK	1	1
		DMAE0	0	1

NOTES: 1. Setting TBOUTH causes all Timer\_B outputs to be set to high impedance.

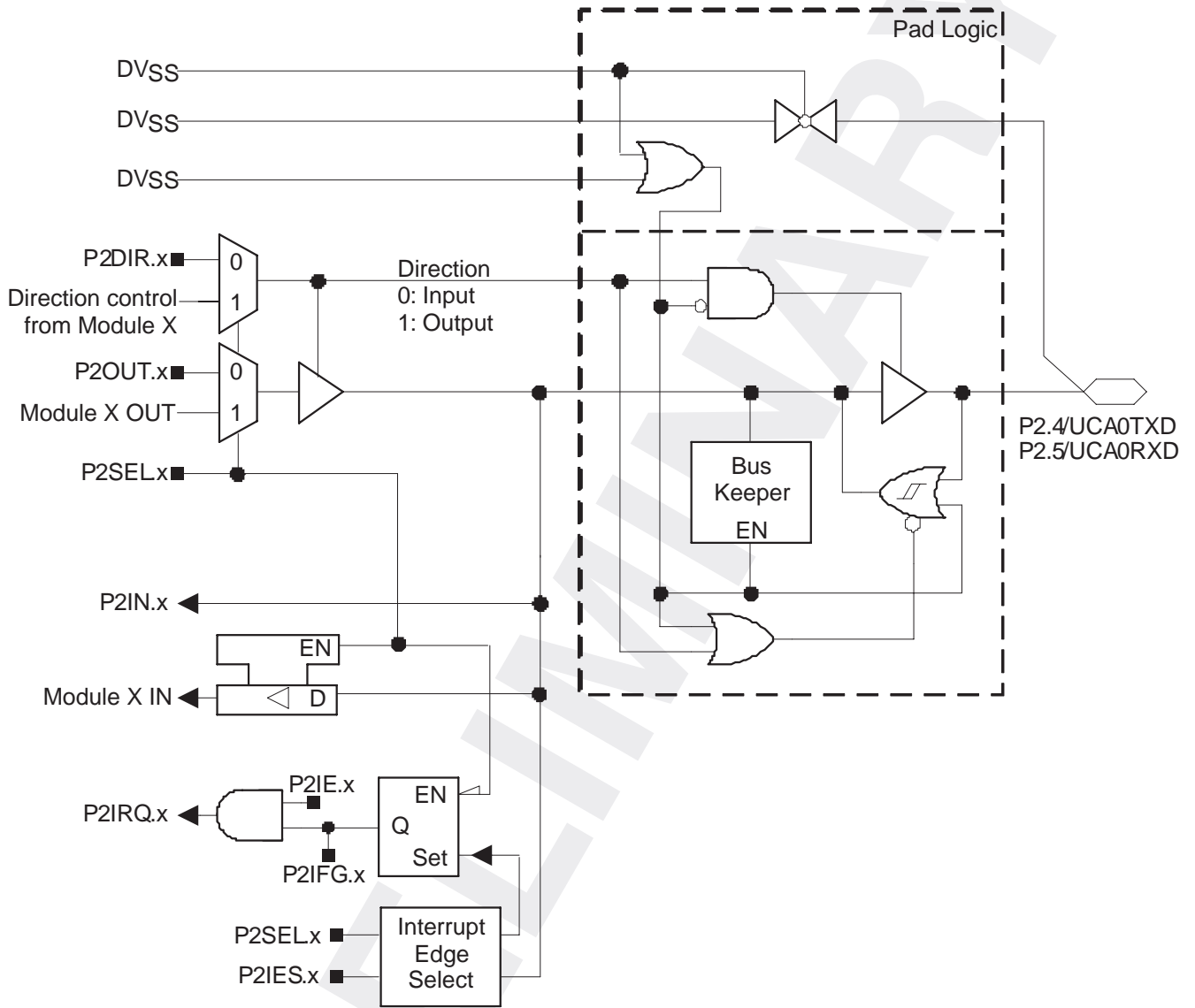
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PRELIMINARY



input/output schematic (continued)

port P2, P2.4 to P2.5, input/output with Schmitt-trigger



Note x = 4,5

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# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## Port P2 (P2.4 and P2.5) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.4/UCA0TXD	4	P2.4 (I/O)	I: 0; O: 1	0
		USCI_A0.UCA0TXD (see Note 1, 2)	X	1
P2.5/UCA0RXD	5	P2.5 (I/O)	I: 0; O: 1	0
		USCI_A0.UCA0RXD (see Note 1, 2)	X	1

NOTES: 1. X: Don't care.  
2. When in USCI mode, P2.4 is set to output, P2.5 is set to input.

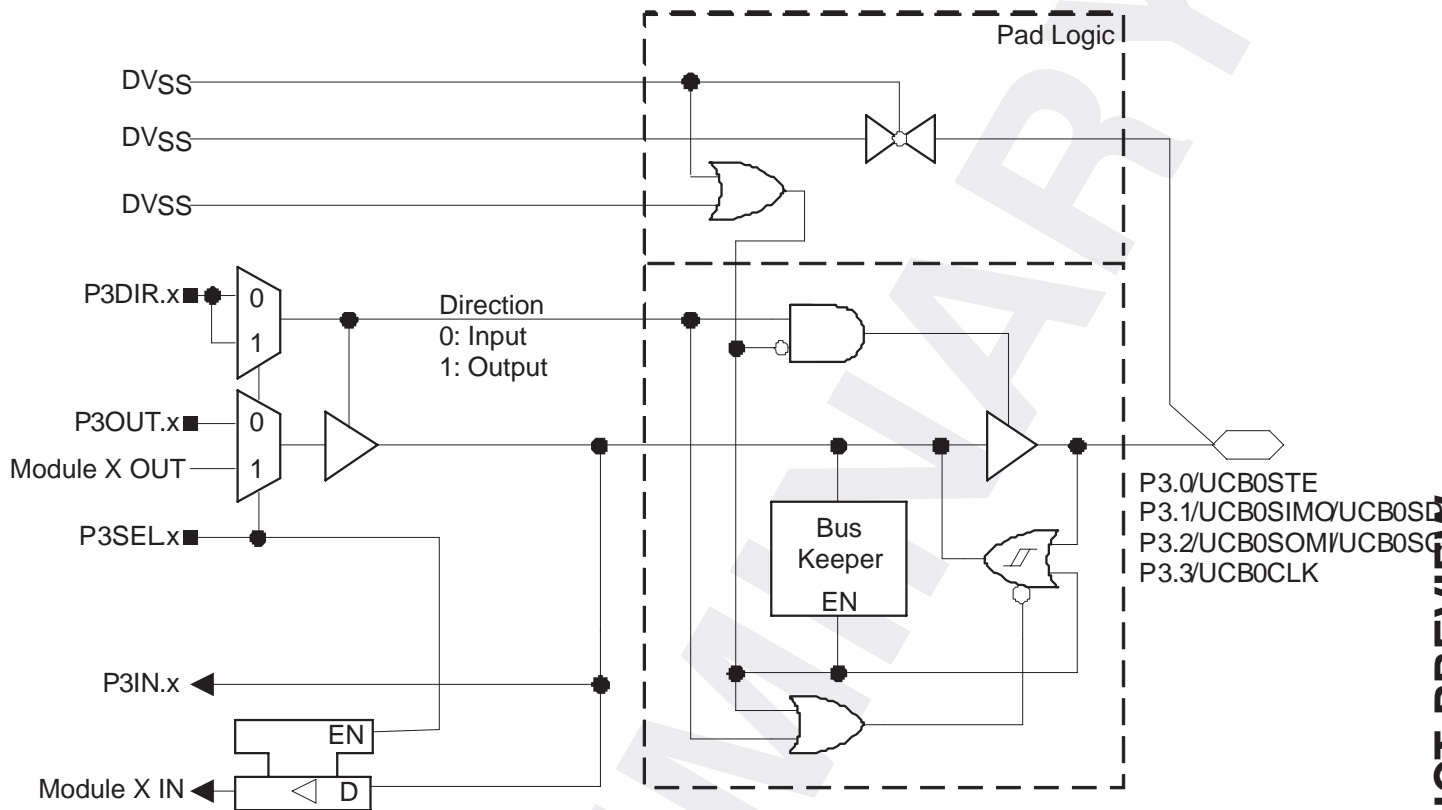
PRODUCT PREVIEW

PRELIMINARY



input/output schematic (continued)

port P3, P3.0 to P3.3, input/output with Schmitt-trigger



Note: x = 0,1,2,3

Port P3 (P3.0 to P3.3) pin functions

PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P3DIR.x	P3SEL.x
P3.0/UCB0STE	0	P3.0 (I/O)	I: 0; O: 1	0
		UCB0STE (see Notes 1, 2)	X	1
P3.1/UCB0SIMO/ UCB0SDA	1	P3.1 (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA (see Notes 1, 2, 3)	X	1
P3.2/UCB0SOMI/ UCB0SCL	2	P3.2 (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL (see Notes 1, 2, 3)	X	1
P3.3/UCB0CLK	3	P3.3 (I/O)	I: 0; O: 1	0
		UCB0CLK (see Notes 1, 2)	X	1

- NOTES: 1. X: Don't care.  
2. The pin direction is controlled by the USCI module.  
3. In case the I2C functionality is selected the output drives only the logical 0 to  $V_{SS}$  level.

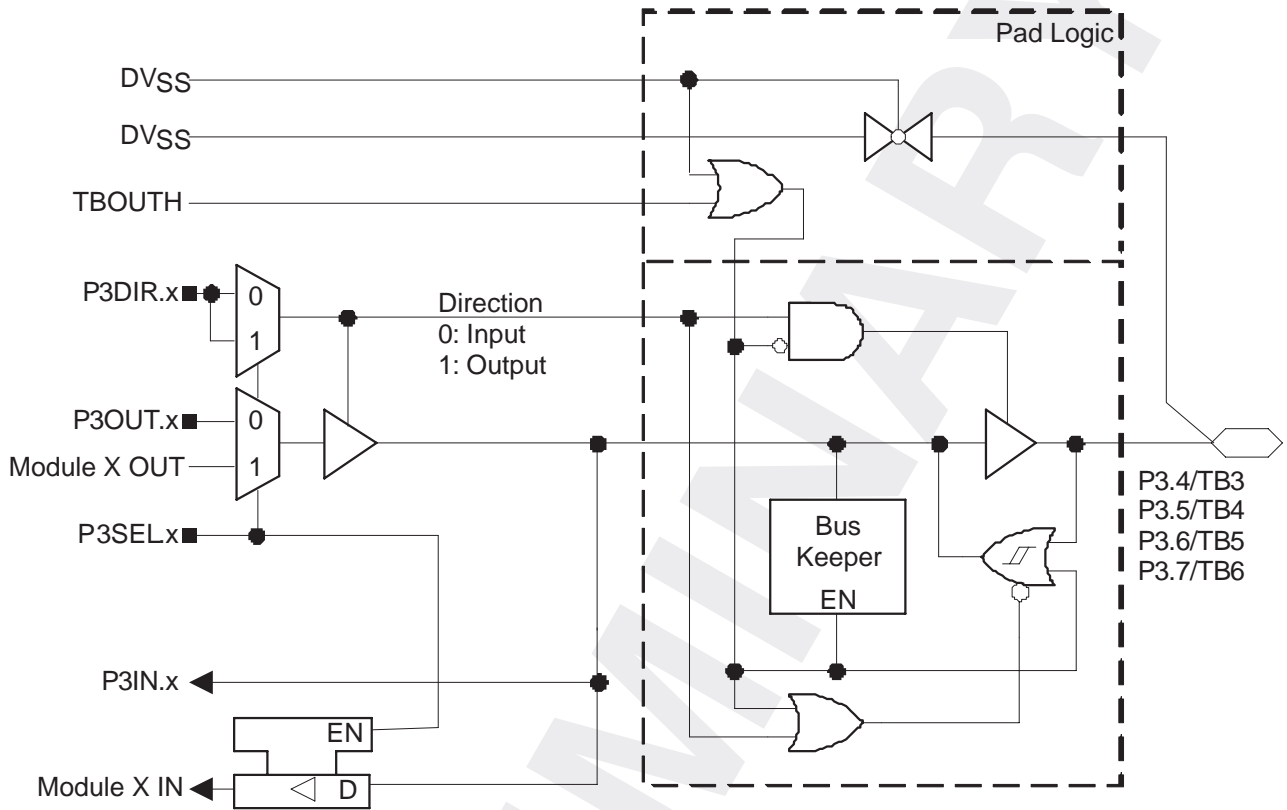
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# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## input/output schematic (continued)

### port P3, P3.4 to P3.7, input/output with Schmitt-trigger



Note: x = 4,5,6,7

### Port P3 (P3.4 to P3.7) pin functions

PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P3DIR.x	P3SEL.x
P3.4/TB3	4	P3.4 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI3A and Timer_B7.CCI3B	0	1
		Timer_B7.TB3 (see Note 1)	1	1
P3.5/TB4	5	P3.5 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI4A and Timer_B7.CCI4B	0	1
		Timer_B7.TB4 (see Note 1)	1	1
P3.6/TB5	6	P3.6 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI5A and Timer_B7.CCI5B	0	1
		Timer_B7.TB5 (see Note 1)	1	1
P3.7/TB6	7	P3.7 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI6A and Timer_B7.CCI6B	0	1
		Timer_B7.TB6 (see Note 1)	1	1

NOTES: 1. Setting TBOUTH causes all Timer\_B outputs to be set to high impedance.

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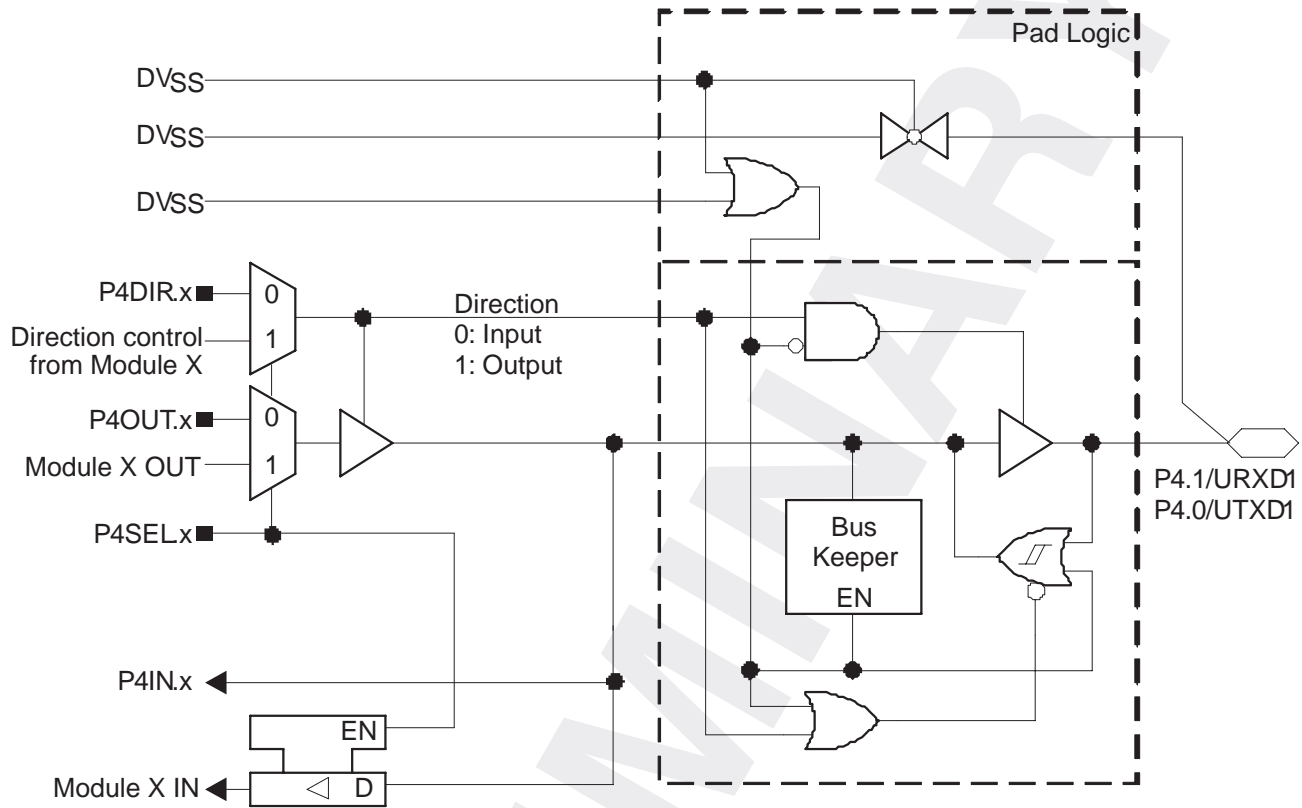


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input/output schematic (continued)

port P4, P4.0 to P4.1, input/output with Schmitt-trigger



Note: x = 0,1

Port P4 (P4.0 to P4.1) pin functions

PIN NAME (P4.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P4DIR.x	P4SEL.x
P4.0/UTXD1	0	P4.0 (I/O)	I: 0; O: 1	0
		USART1.UTXD1 (see Notes 1, 2)	X	1
P4.1/URXD1	1	P4.1 (I/O)	I: 0; O: 1	0
		USART1.URXD1 (see Notes 1, 2)	X	1

NOTES: 1. X: Don't care.  
2. When in USART1 mode, P4.0 is set to output, P4.1 is set to input.

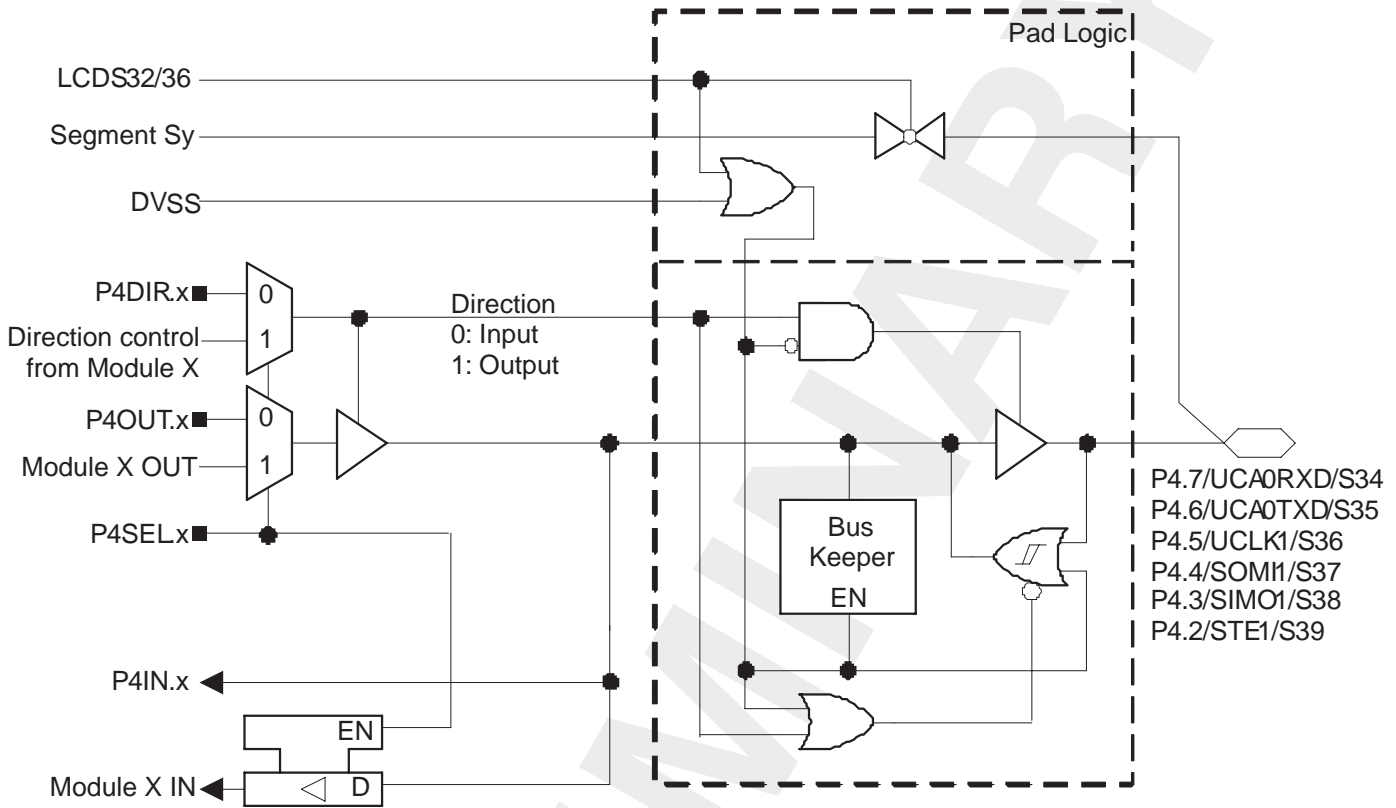
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## input/output schematic (continued)

### port P4, P4.2 to P4.7, input/output with Schmitt-trigger



Note : x = 2,3,4,5,6,7  
y = 34,35,36,37,38,39

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### Port P4 (P4.2 to P4.5) pin functions

PIN NAME (P4.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P4DIR.x	P4SEL.x	LCDS36
P4.2/STE1/S39	2	P4.2 (I/O)	I: 0; O: 1	0	0
		USART1.STE1	0	1	0
		S39 (see Note 1)	X	X	1
P4.3/SIMO/S38	3	P4.3 (I/O)	I: 0; O: 1	0	0
		USART1.SIMO1 (see Notes 1, 2)	0	1	0
		S38 (see Note 1)	X	X	1
P4.4/SOMI/S37	4	P4.4 (I/O)	I: 0; O: 1	0	0
		USART1.SOMI1 (see Notes 1, 2)	0	1	0
		S37 (see Note 1)	X	X	1
P4.5/SOMI/S36	5	P4.5 (I/O)	I: 0; O: 1	0	0
		USART1.UCLK1 (see Notes 1, 2)	0	1	0
		S36 (see Note 1)	X	X	1

NOTES: 1. X: Don't care.  
2. The pin direction is controlled by the USART1 module.



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**Port P4 (P4.6 to P4.7) pin functions (continued)**

PIN NAME (P4.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P4DIR.x	P4SEL.x	LCDS32
P4.6/UCA0TXD/S35	6	P4.6 (I/O)	I: 0; O: 1	0	0
		USCI_A0.UCA0TXD (see Notes 1, 2)	X	1	0
		S35 (see Note 1)	X	X	1
P4.7/UCA0RXD/S34	7	P4.7 (I/O)	I: 0; O: 1	0	0
		USCI_A0.UCA0RXD (see Notes 1, 2)	0	1	0
		S34 (see Note 1)	X	X	1

NOTES: 1. X: Don't care.  
2. When in USCI mode, P4.6 is set to output, P4.7 is set to input.

PRELIMINARY

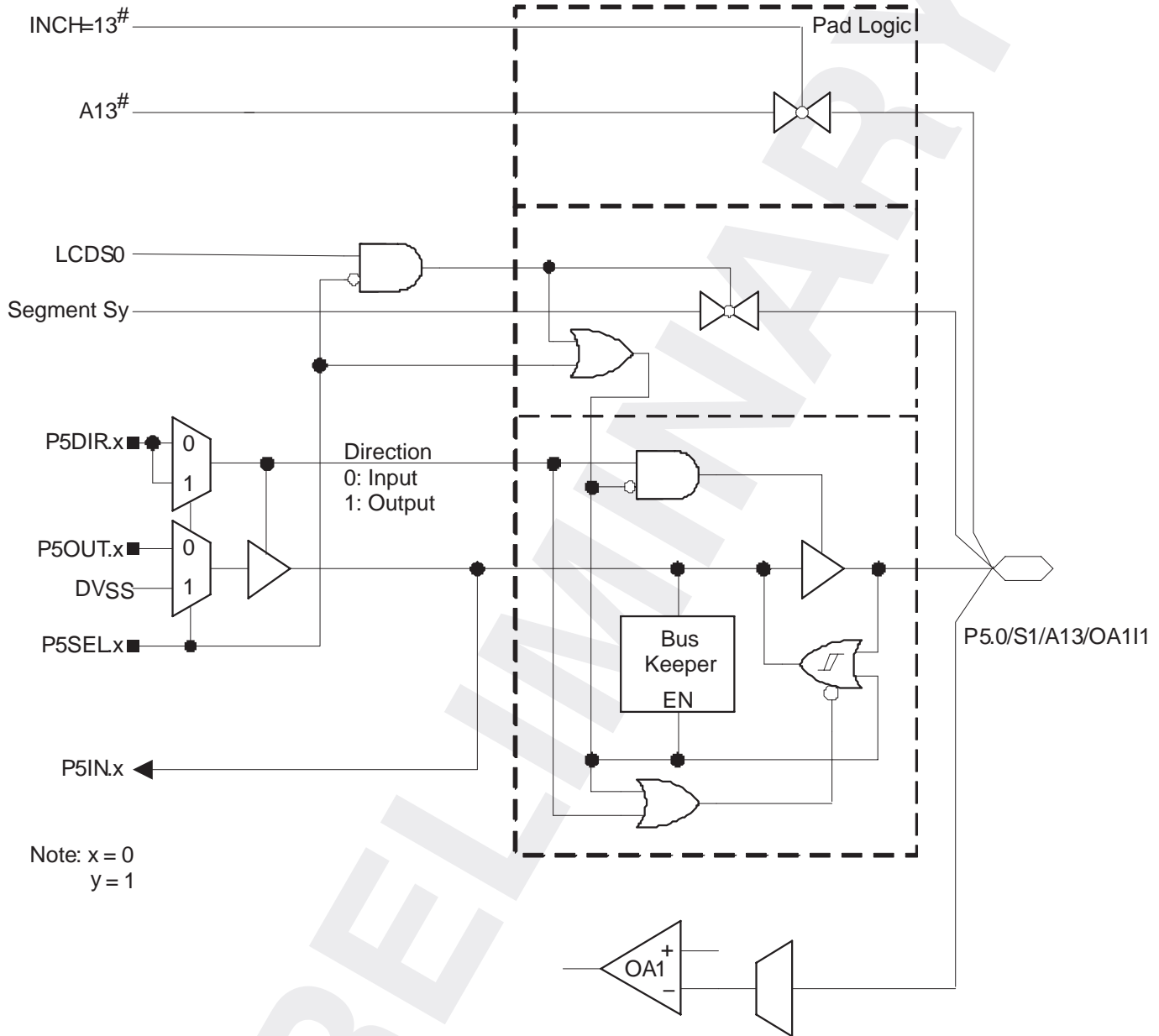
PRODUCT PREVIEW

# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## input/output schematic (continued)

### port P5, P5.0, input/output with Schmitt-trigger



PRODUCT PREVIEW

PRELIMINARY

**Port P5 (P5.0) pin functions**

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS				
			P5DIR.x	P5SEL.x	INCHx	OANx(OA1)	LCDS0
P5.0/S1/A13/OA111	0	P5.0 (I/O) (see Note 1)	I: 0; O: 1	0	X	X	0
		OA111 (see Note 1)	X	X	X	1	0
		A13 (see Notes 1, 3)	X	1	13	X	X
		S1 enabled (see Note 1)	X	0	X	X	1
		S1 disabled (see Note 1)	X	1	X	X	1

- NOTES: 1. X: Don't care.  
 2. N/A: Not available or not applicable.  
 3. Setting the P5SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

PRELIMINARY

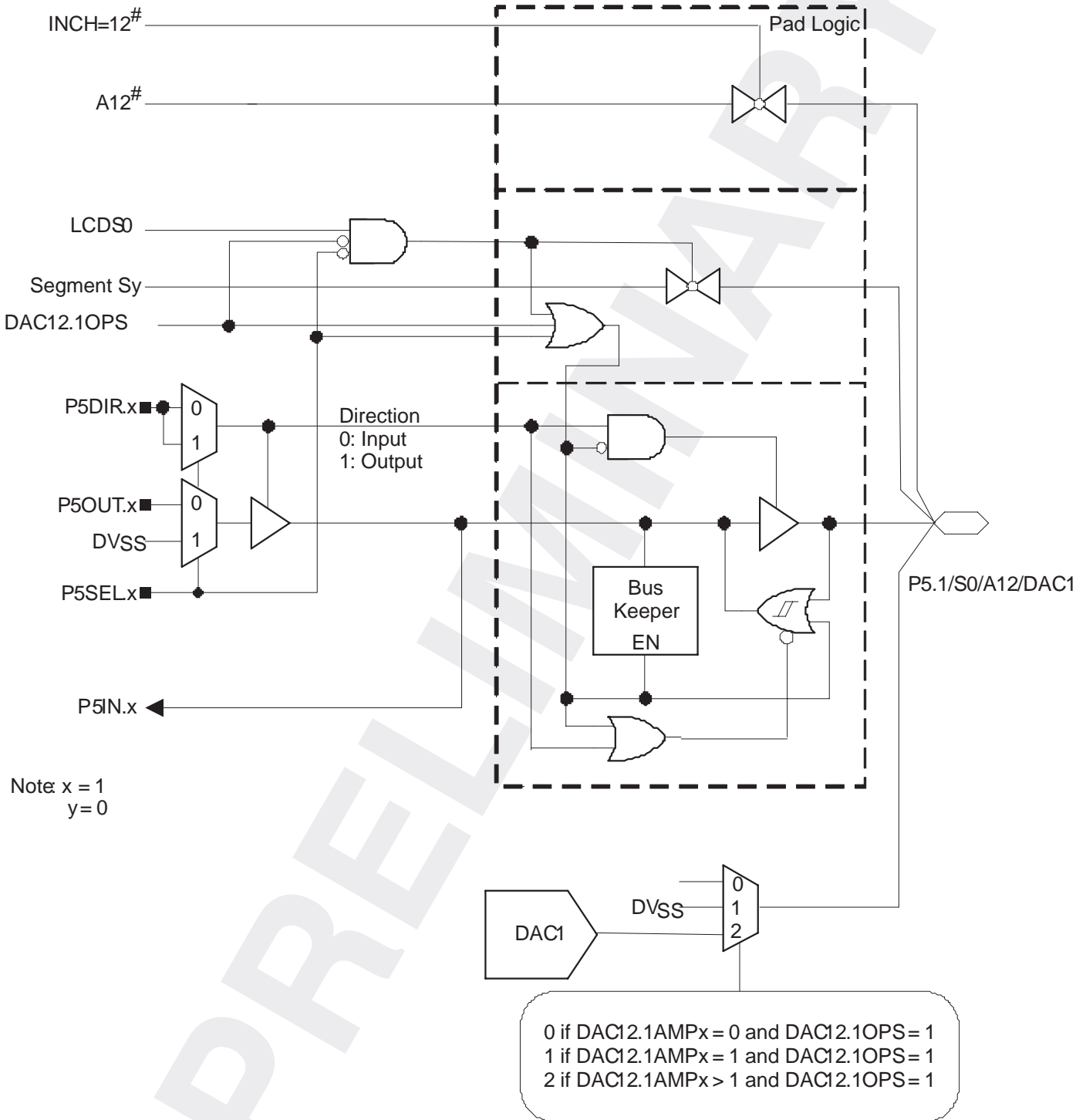
PRODUCT PREVIEW

# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## input/output schematic (continued)

### port P5, P5.1, input/output with Schmitt-trigger



Port P5 (P5.1) pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS					
			P5DIR.x	P5SEL.x	INCHx	DAC12.1OPS	DAC12.1AMPx	LCDS0
P5.0/S0/A12/DAC1	1	P5.0 (I/O) (see Note 1)	I: 0; O: 1	0	X	0	X	0
		DAC1 high impedance (see Note 1)	X	X	X	1	0	X
		DVSS (see Note 1)	X	X	X	1	1	X
		DAC1 output (see Note 1)	X	X	X	1	> 1	X
		A12 (see Notes 1, 2)	X	1	12	0	X	0
		S0 enabled (see Note 1)	X	0	X	0	X	1
		S0 disabled (see Note 1)	X	1	X	0	X	1

- NOTES: 1. X: Don't care.  
2. Setting theP5SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

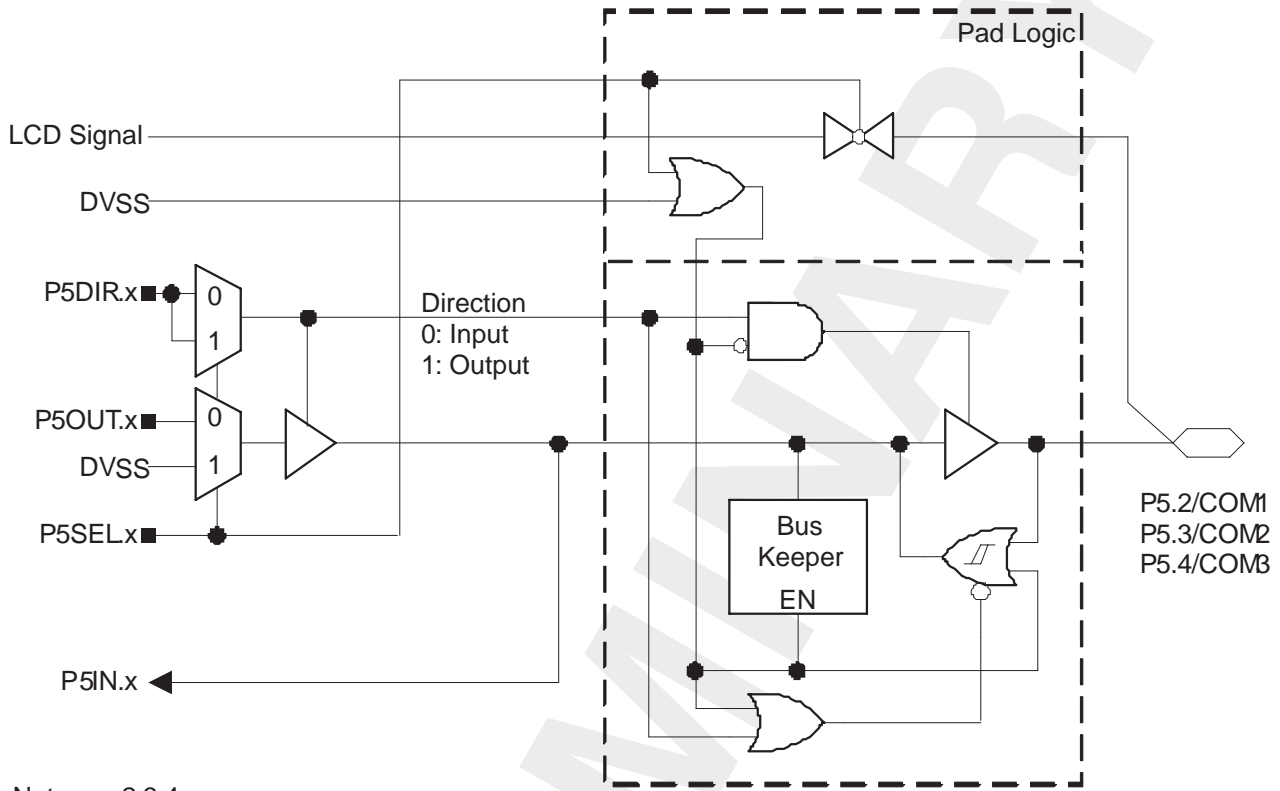
PRODUCT PREVIEW

# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## input/output schematic (continued)

### port P5, P5.2 to P5.4, input/output with Schmitt-trigger



Note: x = 2,3,4

### Port P5 (P5.2 to P5.4) pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P5DIR.x	P5SEL.x
P5.2/COM1	2	P5.2 (I/O)	I: 0; O: 1	0
		COM1 (see Note 1)	X	1
P5.3/COM2	3	P5.3 (I/O)	I: 0; O: 1	0
		COM2 (see Note 1)	X	1
P5.4/COM3	4	P5.4 (I/O)	I: 0; O: 1	0
		COM3 (see Note 1)	X	1

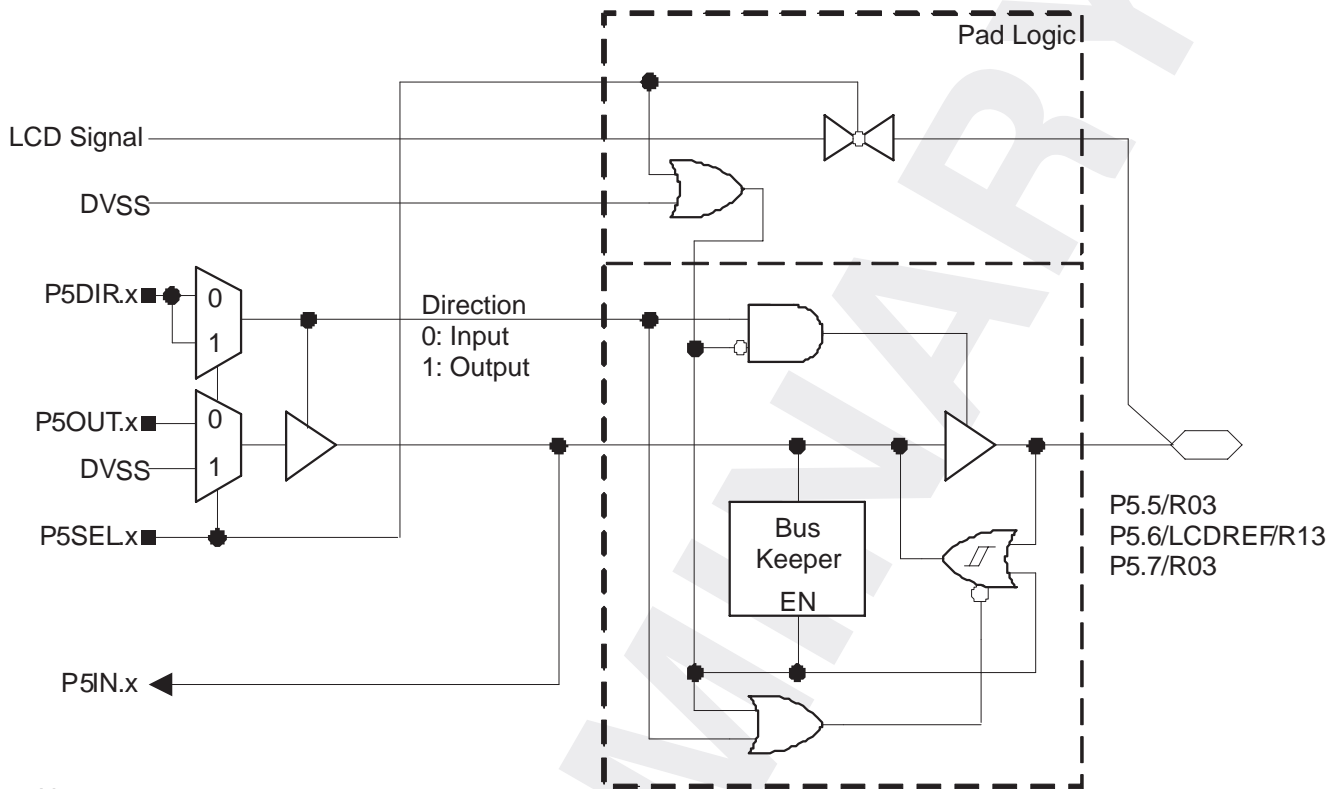
NOTES: 1. X: Don't care.

PRODUCT PREVIEW



input/output schematic (continued)

port P5, P5.5 to P5.7, input/output with Schmitt-trigger



Note: x = 5,6,7

Port P5 (P5.5 to P5.7) pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P5DIR.x	P5SEL.x
P5.5/R03	5	P5.5 (I/O)	I: 0; O: 1	0
		R03 (see Note 1)	X	1
P5.6/LCDREF/R13	6	P5.6 (I/O)	I: 0; O: 1	0
		R13 or LCDREF (see Notes 1, 2)	X	1
P5.7/R03	7	P5.7 (I/O)	I: 0; O: 1	0
		R03 (see Note 1)	X	1

NOTES: 1. X: Don't care.  
2. External reference for the LCD\_A charge pump is applied when VLCDREFx = 01. Otherwise R13 is selected.

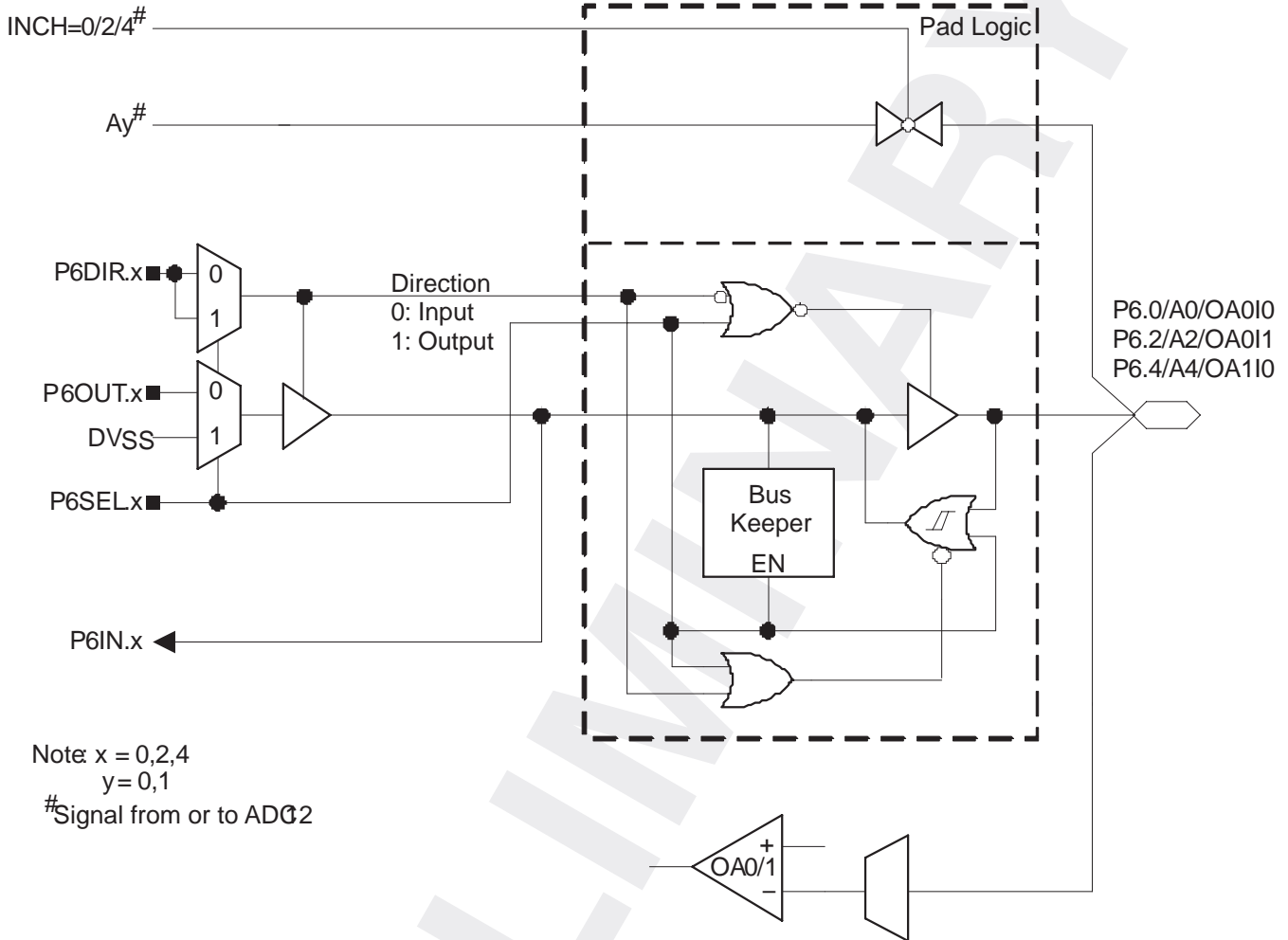
PRODUCT PREVIEW

# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## input/output schematic (continued)

port P6, P6.0, P6.2, and P6.4, input/output with Schmitt-trigger



PRODUCT PREVIEW

PRELIMINARY

**Port P6 (P6.0, P6.2, and P6.4) pin functions**

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS				
			P6DIR.x	P6SEL.x	OAPx (OA0) OANx (OA0)	OAPx (OA1) OANx(OA1)	INCHx
P6.0/A0/OA0I0	0	P6.0 (I/O) (see Note 1)	I: 0; O: 1	0	X	X	X
		OA0I0 (see Note 1)	X	X	0	X	X
		A0 (see Notes 1, 3)	X	1	X	X	0
P6.2/A2/OA0I1	2	P6.2 (I/O) (see Note 1)	I: 0; O: 1	0	X	X	X
		OA0I1 (see Note 1)	X	X	1	X	X
		A2 (see Notes 1, 3)	X	1	X	X	2
P6.4/A4/OA1I0	4	P6.4 (I/O) (see Note 1)	I: 0; O: 1	0	X	X	X
		OA1I0 (see Note 1)	X	X	X	0	X
		A4 (see Notes 1, 3)	X	1	X	X	4

- NOTES: 1. X: Don't care.  
 2. N/A: Not available or not applicable.  
 3. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

PRELIMINARY

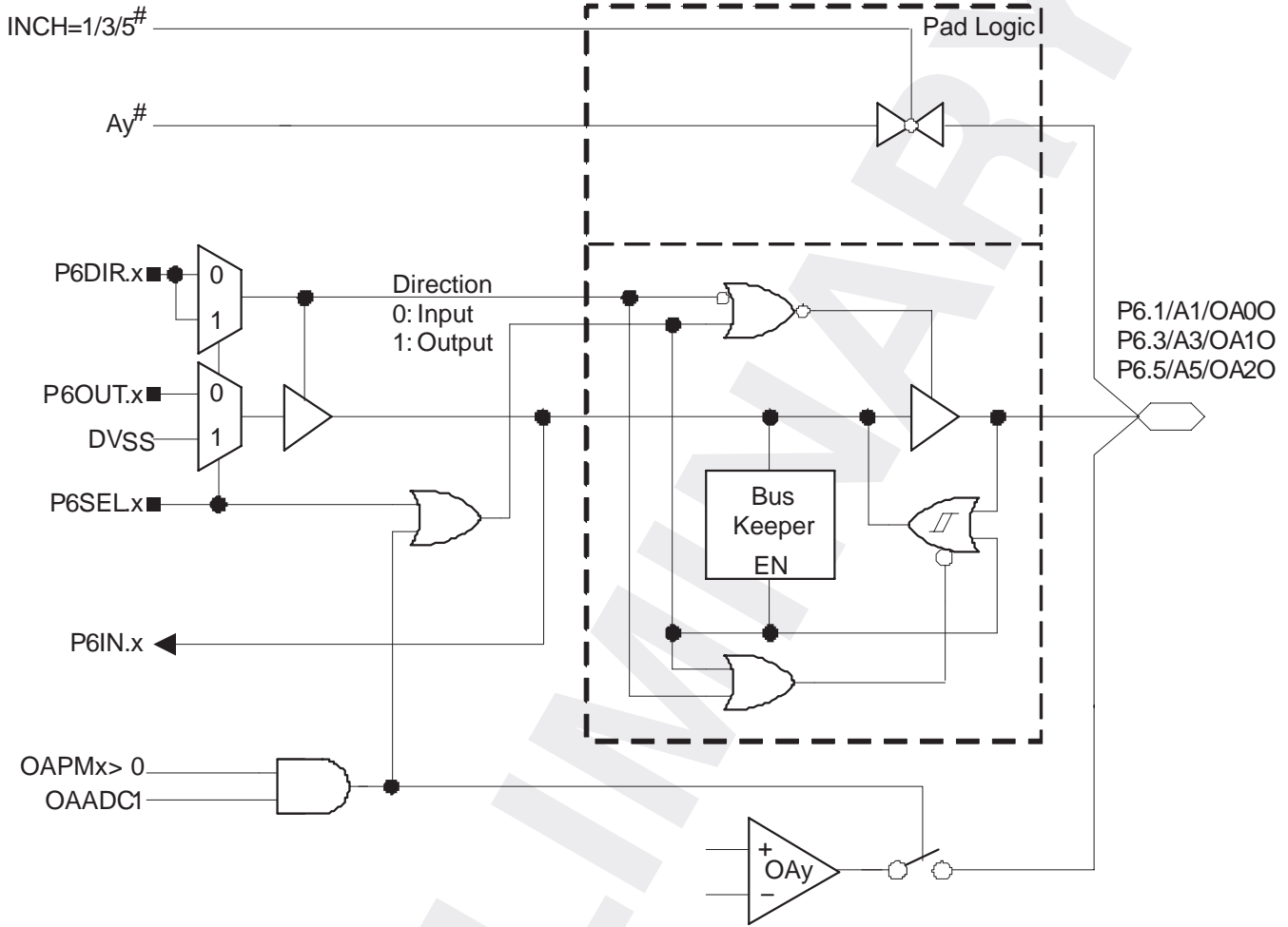
**PRODUCT PREVIEW**

# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## input/output schematic (continued)

### port P6, P6.1, P6.3, and P6.5 input/output with Schmitt-trigger



Note: x = 1,3,5  
y = 0,1,2  
#Signal from or to ADG2

PRODUCT PREVIEW

PRELIMINARY

**Port P6 (P6.1, P6.3, and P6.5) pin functions**

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS				
			P6DIR.x	P6SEL.x	OAADC1	OAPMx	INCHx
P6.1/A1/OA00	1	P6.1 (I/O) (see Note 1)	I: 0; O: 1	0	X	X	X
		OA00 (see Notes 1, 4)	X	X	1	> 0	X
		A1 (see Notes 1, 3)	X	1	X	X	1
P6.3/A3/OA10	3	P6.3 (I/O) (see Note 1)	I: 0; O: 1	0	X	X	X
		OA10 (see Notes 1, 4)	X	X	1	> 0	X
		A3 (see Notes 1, 3)	X	1	X	X	3
P6.5/A5/OA20	5	P6.5 (I/O) (see Note 1)	I: 0; O: 1	0	X	X	X
		OA20 (see Notes 1, 4)	X	X	1	> 0	X
		A5 (see Notes 1, 3)	X	1	X	X	5

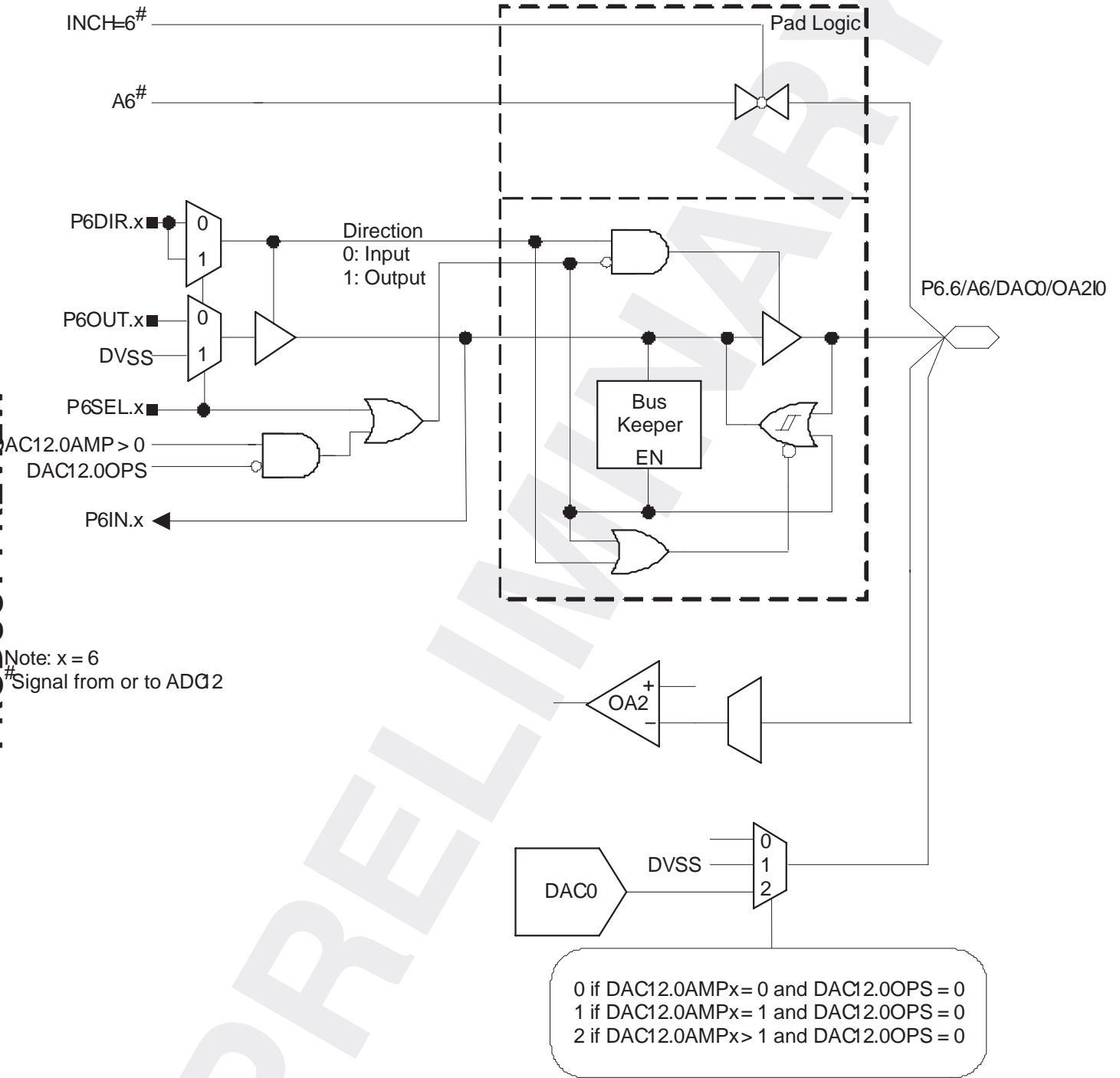
- NOTES:
1. X: Don't care.
  2. N/A: Not available or not applicable.
  3. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
  4. Setting the OAADC1 bit or setting OAFc<sub>x</sub> = 00 will cause the operational amplifier to be present at the pin as well as internally connected to the corresponding ADC12 input.

# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## input/output schematic (continued)

### port P6, P6.6, input/output with Schmitt-trigger



PRODUCT PREVIEW

PRELIMINARY

**Port P6 (P6.6) pin functions**

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS					
			P6DIR.x	P6SEL.x	INCHx	DAC12.0OPS	DAC12.0AMPx	OAPx (OA2) OANx (OA2)
P6.6/A6/DAC0/OA2I0	6	P6.6 (I/O) (see Note 1)	I: 0; O: 1	0	X	1	X	X
		DAC0 high impedance (see Note 1)	X	X	X	0	0	X
		DVSS (see Note 1)	X	X	X	0	1	X
		DAC0 output (see Note 1)	X	X	X	0	>1	X
		A6 (see Notes 1, 2)	X	1	6	X	X	X
		OA2I0 (see Note 1)	X	X	0	X	X	0

- NOTES: 1. X: Don't care.  
 2. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

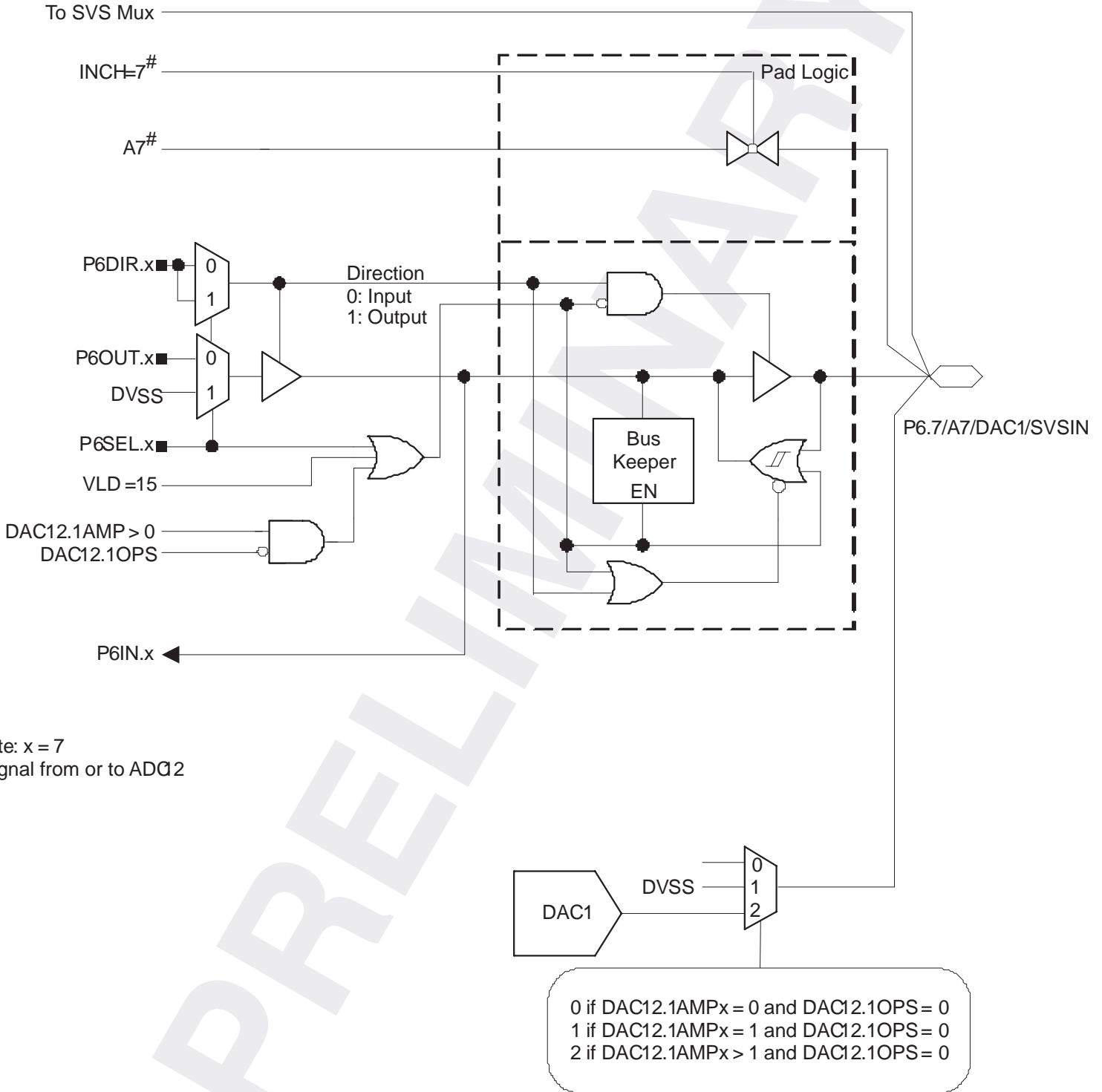
**PRODUCT PREVIEW**

# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## input/output schematic (continued)

### port P6, P6.7, input/output with Schmitt-trigger



Note: x = 7  
#Signal from or to ADQ2

PRODUCT PREVIEW

PRELIMINARY



**Port P6 (P6.7) pin functions**

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS				
			P6DIR.x	P6SEL.x	INCHx	DAC12.1OPS	DAC12.1AMPx
P6.7/A7/DAC1/SVSIN	7	P6.7 (I/O) (see Note 1)	I: 0; O: 1	0	X	1	X
		DAC1 high impedance (see Note 1)	X	X	X	0	0
		DVSS (see Note 1)	X	X	X	0	1
		DAC1 output (see Note 1)	X	X	X	0	> 1
		A7 (see Notes 1, 2)	X	1	7	X	X
		SVSIN (see Notes 1,3)	0	1	0	1	X

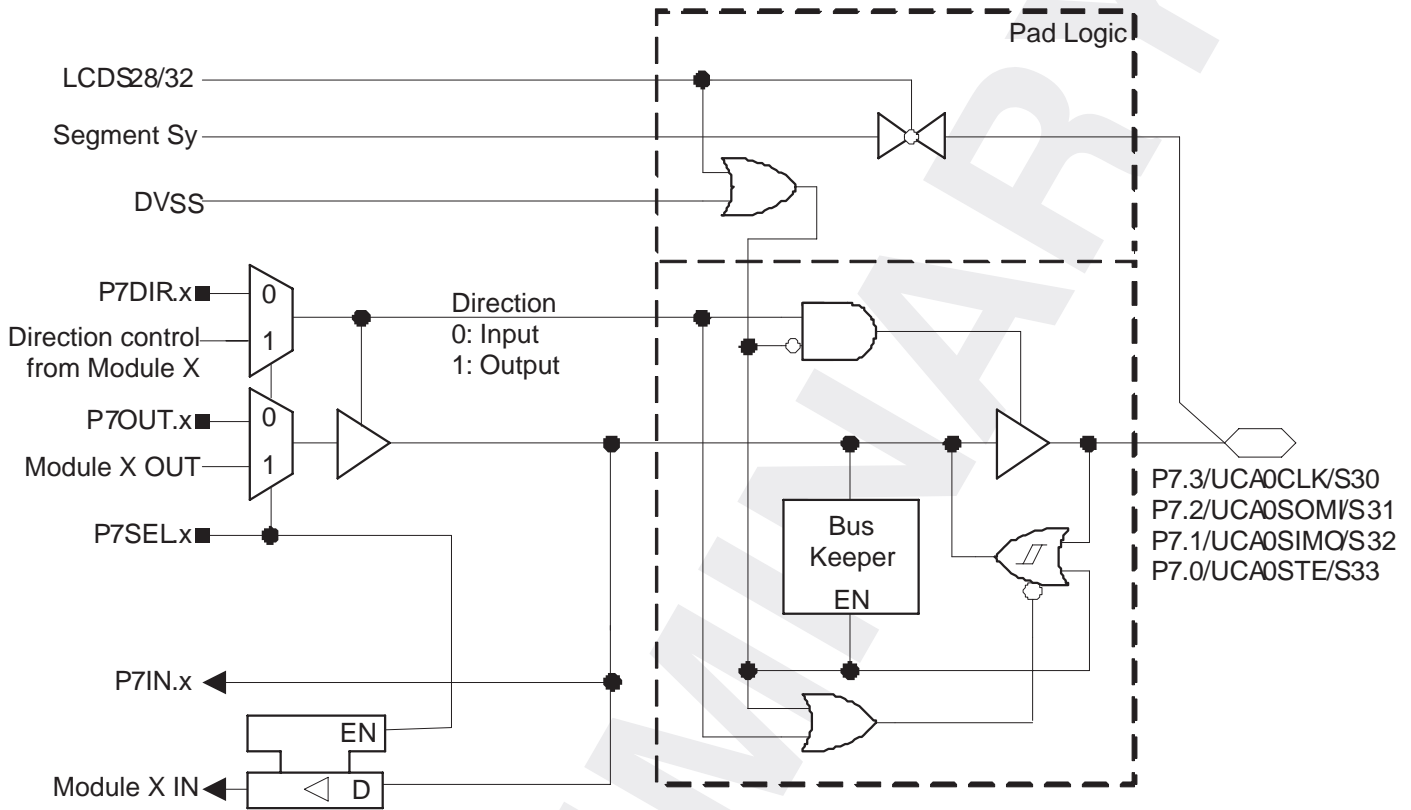
- NOTES: 1. X: Don't care.  
 2. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.  
 3. Setting VLDx = 15 will also cause the external SVSIN to be used. In this case, the P6SEL.x bit is a do not care.

# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## input/output schematic (continued)

### port P7, P7.0 – P7.3, input/output with Schmitt-trigger



Note: x = 0,1,2,3  
y = 30,31,32,33

### Port P7 (P7.0 to P7.1) pin functions

PIN NAME (P7.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P7DIR.x	P7SEL.x	LCDS32
P7.0/UCA0STE/S33	0	P7.0 (I/O)	I: 0; O: 1	0	0
		USCI_A0.UCA0STE (see Notes 1, 2)	X	1	0
		S33 (see Note 1)	X	X	1
P7.1/UCA0SIMO/S32	1	P7.1 (I/O)	I: 0; O: 1	0	0
		USCI_A0.UCA0SIMO (see Notes 1, 2)	X	1	0
		S32 (see Note 1)	X	X	1

NOTES: 1. X: Don't care.  
2. The pin direction is controlled by the USCI module.

PRODUCT PREVIEW

Port P7 (P7.2 to P7.3) pin functions (continued)

PIN NAME (P7.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P7DIR.x	P7SEL.x	LCDS28
P7.2/UCA0SOMI/S31	2	P7.2 (I/O)	I: 0; O: 1	0	0
		USCI_A0.UCA0SOMI (see Notes 1, 2)	X	1	0
		S31 (see Note 1)	X	X	1
P7.3/UCA0CLK/S30	3	P7.3 (I/O)	I: 0; O: 1	0	0
		USCI_A0.UCA0CLK (see Notes 1, 2)	X	1	0
		S30 (see Note 1)	X	X	1

NOTES: 1. X: Don't care.  
2. The pin direction is controlled by the USCI module.

PRELIMINARY

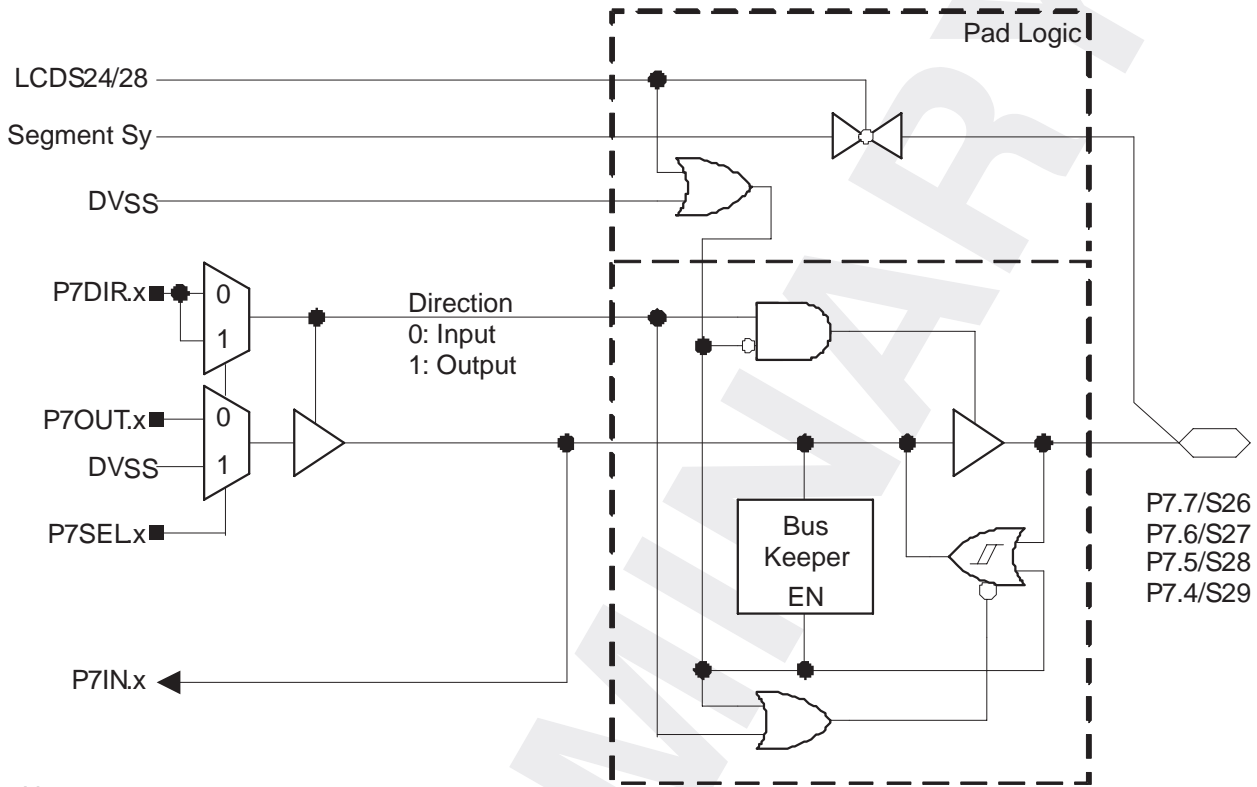
PRODUCT PREVIEW

# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## input/output schematic (continued)

### port P7, P7.4 – P7.7, input/output with Schmitt-trigger



Note: x = 4,5,6,7  
y = 26,27,28,29

### Port P7 (P7.4 to P7.5) pin functions

PIN NAME (P7.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P7DIR.x	P7SEL.x	LCDS28
P7.4/S29	4	P7.4 (I/O)	I: 0; O: 1	0	0
		S29 (see Note 1)	X	X	1
P7.5/S28	5	P7.5 (I/O)	I: 0; O: 1	0	0
		S28 (see Note 1)	X	X	1

NOTES: 1. X: Don't care.

PRODUCT PREVIEW

**Port P7 (P7.6 to P7.7) pin functions (continued)**

PIN NAME (P7.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P7DIR.x	P7SEL.x	LCDS24
P7.6/S27	6	P7.6 (I/O)	I: 0; O: 1	0	0
		S27 (see Note 1)	X	X	1
P7.7/S26	7	P7.7 (I/O)	I: 0; O: 1	0	0
		S26 (see Note 1)	X	X	1

NOTES: 1. X: Don't care.

PRELIMINARY

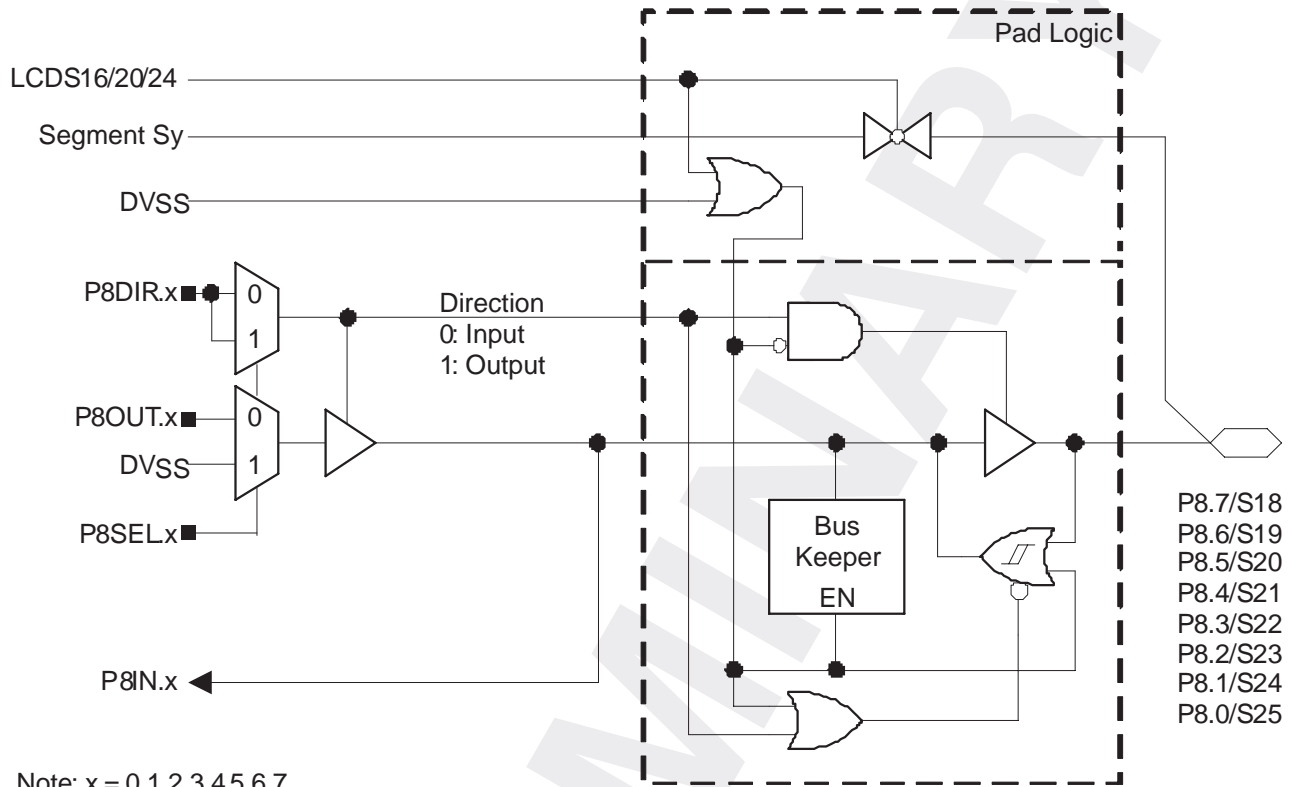
**PRODUCT PREVIEW**

# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## input/output schematic (continued)

### port P8, P8.0 – P8.7, input/output with Schmitt-trigger



Note: x = 0,1,2,3,4,5,6,7  
y = 25,24,23,22,21,20,19,18

### Port P8 (P8.0 to P8.1) pin functions

PIN NAME (P8.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P8DIR.x	P8SEL.x	LCDS16
P8.0/S18	0	P8.0 (I/O)	I: 0; O: 1	0	0
		S18 (see Note 1)	X	X	1
P8.1/S19	0	P8.0 (I/O)	I: 0; O: 1	0	0
		S19 (see Note 1)	X	X	1

NOTES: 1. X: Don't care.

PRODUCT PREVIEW

**Port P8 (P8.2 to P8.5) pin functions (continued)**

PIN NAME (P8.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P8DIR.x	P8SEL.x	LCDS20
P8.2/S20	2	P8.2 (I/O)	I: 0; O: 1	0	0
		S20 (see Note 1)	X	X	1
P8.3/S21	3	P8.3 (I/O)	I: 0; O: 1	0	0
		S21 (see Note 1)	X	X	1
P8.4/S22	4	P8.4 (I/O)	I: 0; O: 1	0	0
		S22 (see Note 1)	X	X	1
P8.5/S23	5	P8.5 (I/O)	I: 0; O: 1	0	0
		S23 (see Note 1)	X	X	1

NOTES: 1. X: Don't care.

**Port P8 (P8.6 to P8.7) pin functions**

PIN NAME (P8.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P8DIR.x	P8SEL.x	LCDS24
P8.6/S24	6	P8.6 (I/O)	I: 0; O: 1	0	0
		S24 (see Note 1)	X	X	1
P8.7/S25	7	P8.7 (I/O)	I: 0; O: 1	0	0
		S25 (see Note 1)	X	X	1

NOTES: 1. X: Don't care.

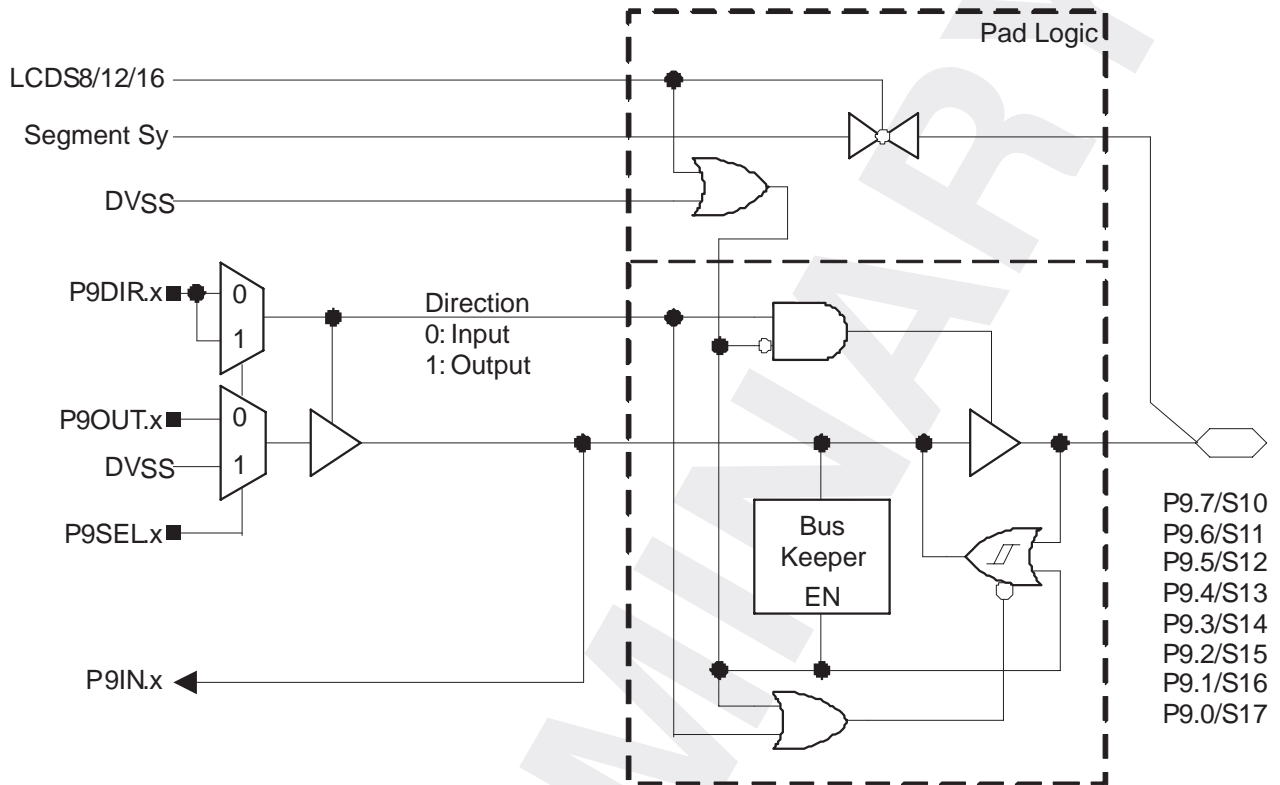
PRODUCT PREVIEW

# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## input/output schematic (continued)

port P9, P9.0 – P9.7, input/output with Schmitt-trigger



Note: x = 0,1,2,3,4,5,6,7  
y = 17,16,15,14,13,12,11,10

### Port P9 (P9.0 to P9.1) pin functions

PIN NAME (P9.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P9DIR.x	P9SEL.x	LCDS16
P9.0/S17	0	P9.0 (I/O)	I: 0; O: 1	0	0
		S17 (see Note 1)	X	X	1
P9.1/S16	1	P9.1 (I/O)	I: 0; O: 1	0	0
		S16 (see Note 1)	X	X	1

NOTES: 1. X: Don't care.

PRODUCT PREVIEW



**Port P9 (P9.2 to P9.5) pin functions (continued)**

PIN NAME (P9.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P9DIR.x	P9SEL.x	LCDS12
P9.2/S20	2	P9.2 (I/O)	I: 0; O: 1	0	0
		S15 (see Note 1)	X	X	1
P9.3/S21	3	P9.3 (I/O)	I: 0; O: 1	0	0
		S14 (see Note 1)	X	X	1
P9.4/S22	4	P9.4 (I/O)	I: 0; O: 1	0	0
		S13 (see Note 1)	X	X	1
P9.5/S23	5	P9.5 (I/O)	I: 0; O: 1	0	0
		S12 (see Note 1)	X	X	1

NOTES: 1. X: Don't care.

**Port P9 (P9.6 to P9.7) pin functions (continued)**

PIN NAME (P9.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P9DIR.x	P9SEL.x	LCDS8
P9.6/S24	6	P9.6 (I/O)	I: 0; O: 1	0	0
		S11 (see Note 1)	X	X	1
P9.7/S25	7	P9.7 (I/O)	I: 0; O: 1	0	0
		S10 (see Note 1)	X	X	1

NOTES: 1. X: Don't care.

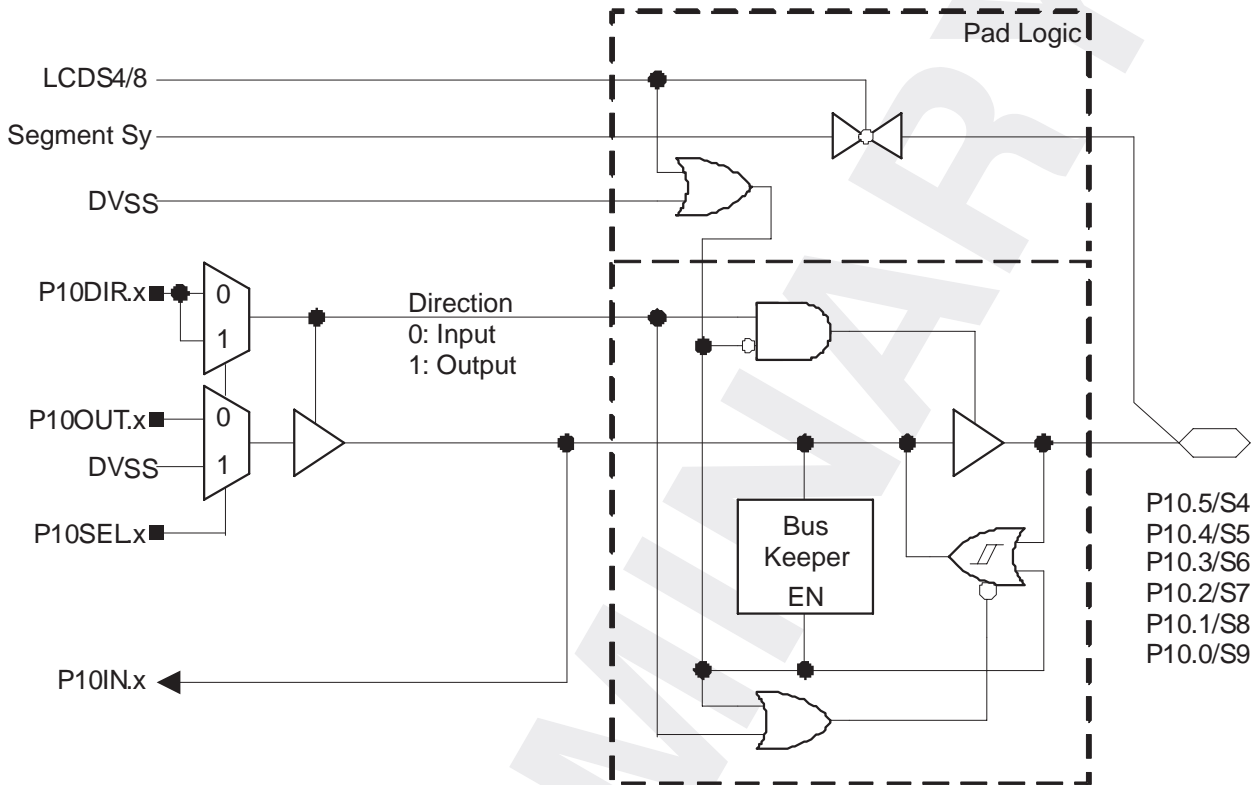
PRODUCT PREVIEW

# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## input/output schematic (continued)

### port P10, P10.0 – P10.5, input/output with Schmitt-trigger



Note: x = 0,1,2,3,4,5  
y = 9,8,7,6,5,4

### Port P10 (P10.0 to P10.1) pin functions

PIN NAME (P10.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P10DIR.x	P10SEL.x	LCDS8
P10.0/S8	0	P10.0 (I/O)	I: 0; O: 1	0	0
		S8 (see Note 1)	X	X	1
P10.1/S7	1	P10.1 (I/O)	I: 0; O: 1	0	0
		S7 (see Note 1)	X	X	1

NOTES: 1. X: Don't care.

PRODUCT PREVIEW

Port P10 (P10.2 to P10.5) pin functions (continued)

PIN NAME (P10.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P10DIR.x	P10SEL.x	LCDS4
P10.2/S7	2	P10.2 (I/O)	I: 0; O: 1	0	0
		S7 (see Note 1)	X	X	1
P10.3/S6	3	P10.3 (I/O)	I: 0; O: 1	0	0
		S6 (see Note 1)	X	X	1
P10.4/S5	4	P10.4 (I/O)	I: 0; O: 1	0	0
		S5 (see Note 1)	X	X	1
P10.5/S4	5	P10.5 (I/O)	I: 0; O: 1	0	0
		S4 (see Note 1)	X	X	1

NOTES: 1. X: Don't care.

PRELIMINARY

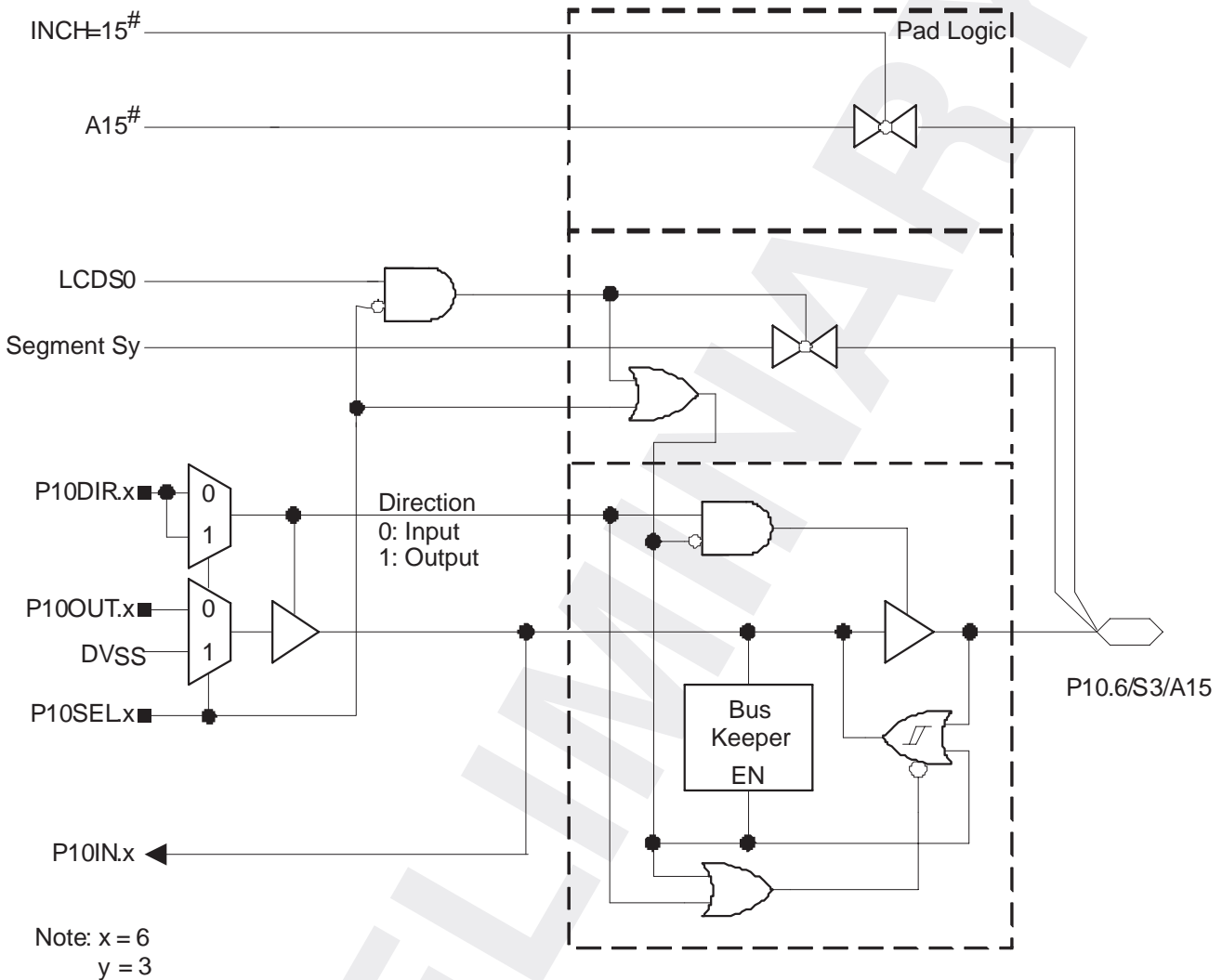
PRODUCT PREVIEW

# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## input/output schematic (continued)

### port P10, P10.6, input/output with Schmitt-trigger



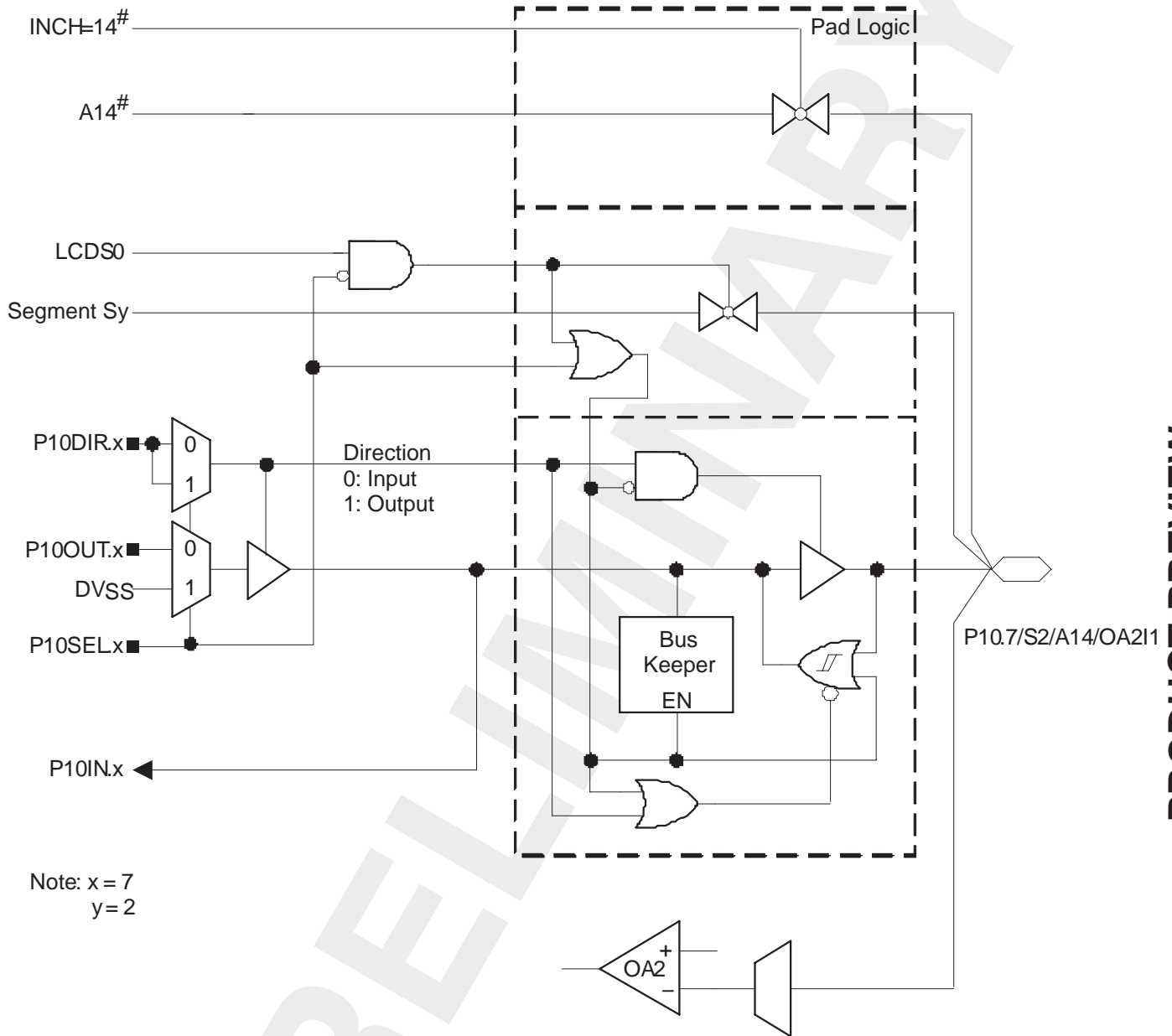
### Port P10 (P10.6) pin functions

PIN NAME (P10.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			P10DIR.x	P10SEL.x	INCHx	LCDS0
P10.6/S3/A15	6	P5.0 (I/O) (see Note 1)	I: 0; O: 1	0	X	0
		A15 (see Notes 1, 3)	X	1	15	0
		S3 enabled (see Note 1)	X	0	X	1
		S3 disabled (see Note 1)	X	1	X	1

- NOTES: 1. X: Don't care.  
2. N/A: Not available or not applicable.  
3. Setting the P10SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

input/output schematic (continued)

port P10, P10.7, input/output with Schmitt-trigger



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# MSP430FG461x

## MIXED SIGNAL MICROCONTROLLER

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### Port P10 (P10.7) pin functions

PIN NAME (P10.X)	X	FUNCTION	CONTROL BITS / SIGNALS				
			P10DIR.x	P10SEL.x	INCHx	OAPx (OA1) OANx (OA1)	LCDS0
P10.7/S2/A14/OA2I1	7	P10.7 (I/O) (see Note 1)	I: 0; O: 1	0	X	X	0
		A14 (see Notes 1, 3)	X	1	14	X	0
		OA2I1 (see Notes 1, 3)	X	X	X	1	0
		S2 enabled (see Note 1)	X	0	X	X	1
		S2 disabled (see Note 1)	X	1	X	X	1

- NOTES: 1. X: Don't care.  
 2. N/A: Not available or not applicable.  
 3. Setting the P10SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

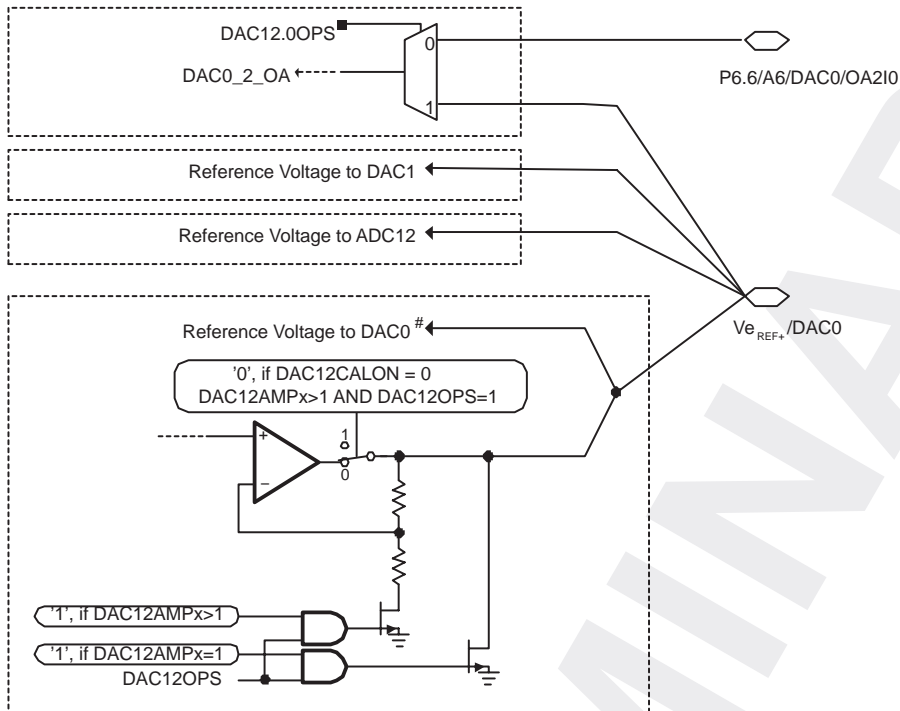
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PRELIMINARY



input/output schematic (continued)

$V_{eREF+}/DAC0$



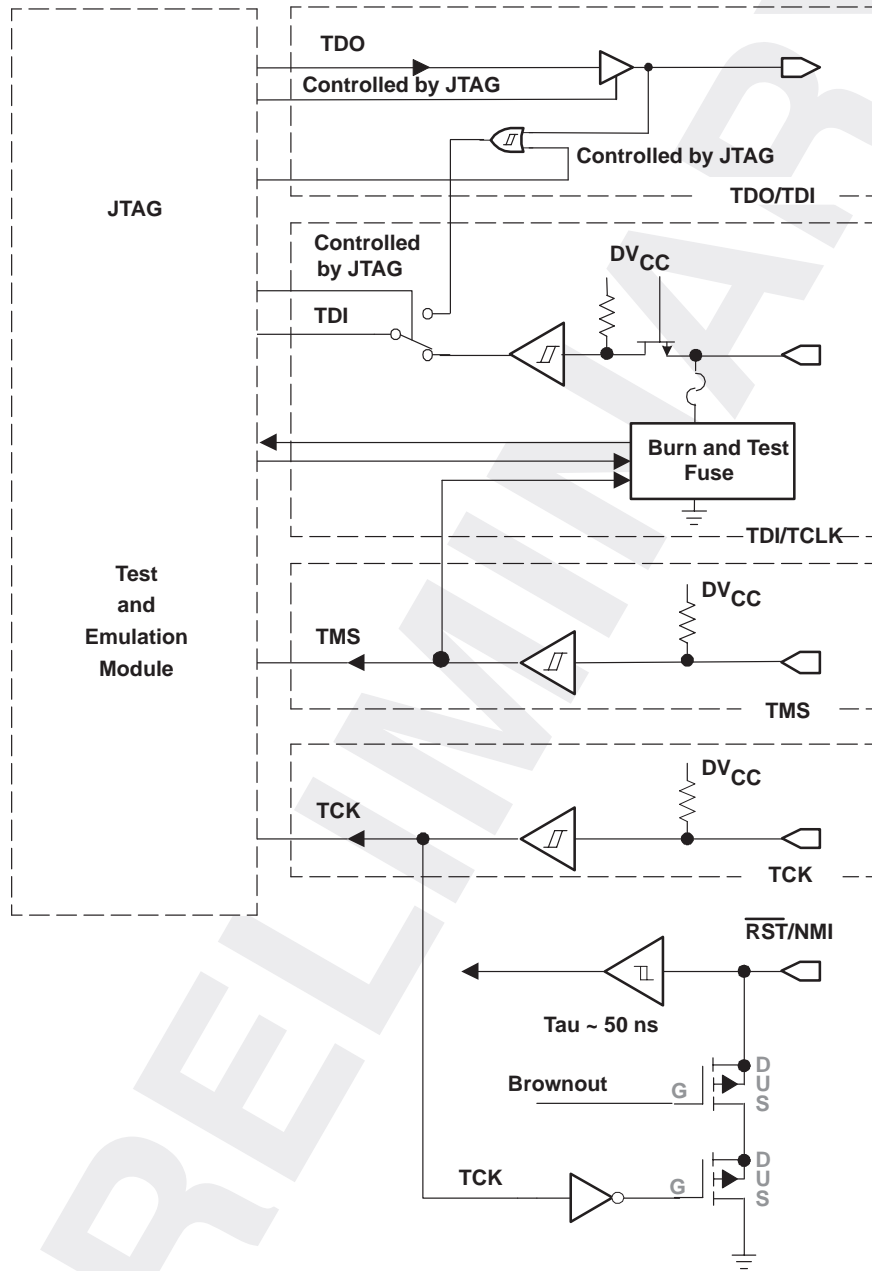
# If the reference of DAC0 is taken from pin  $V_{eREF+}/DAC0$ , unpredictable voltage levels will be on pin. In this situation, the DAC0 output is fed back to its own reference input.

# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## input/output schematic (continued)

JTAG pins TMS, TCK, TDI/TCLK, TDO/TDI, input/output with Schmitt-trigger or output



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### JTAG fuse check mode

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current ( $I_{(TF)}$ ) of 1 mA at 3 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current only flows when the fuse check mode is active and the TMS pin is in a low state (see Figure 37). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition). The JTAG pins are terminated internally and therefore do not require external termination.

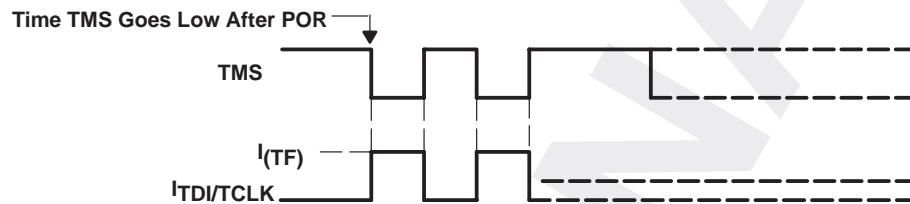


Figure 37. Fuse Check Mode Current

# MSP430FG461x MIXED SIGNAL MICROCONTROLLER

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## Data Sheet Revision History

Literature Number	Summary
SLAS508	Preliminary PRODUCT PREVIEW datasheet release.

NOTE: The referring page and figure numbers are referred to the respective document revision.

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**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
MSP430FG4616IPZ	PREVIEW	LQFP	PZ	100	90	TBD	Call TI	Call TI
MSP430FG4616IPZR	PREVIEW	LQFP	PZ	100	1000	TBD	Call TI	Call TI
MSP430FG4617IPZ	PREVIEW	LQFP	PZ	100	90	TBD	Call TI	Call TI
MSP430FG4617IPZR	PREVIEW	LQFP	PZ	100	1000	TBD	Call TI	Call TI
MSP430FG4618IPZ	PREVIEW	LQFP	PZ	100	90	TBD	Call TI	Call TI
MSP430FG4618IPZR	PREVIEW	LQFP	PZ	100	1000	TBD	Call TI	Call TI
MSP430FG4619IPZ	PREVIEW	LQFP	PZ	100	90	TBD	Call TI	Call TI
MSP430FG4619IPZR	PREVIEW	LQFP	PZ	100	1000	TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

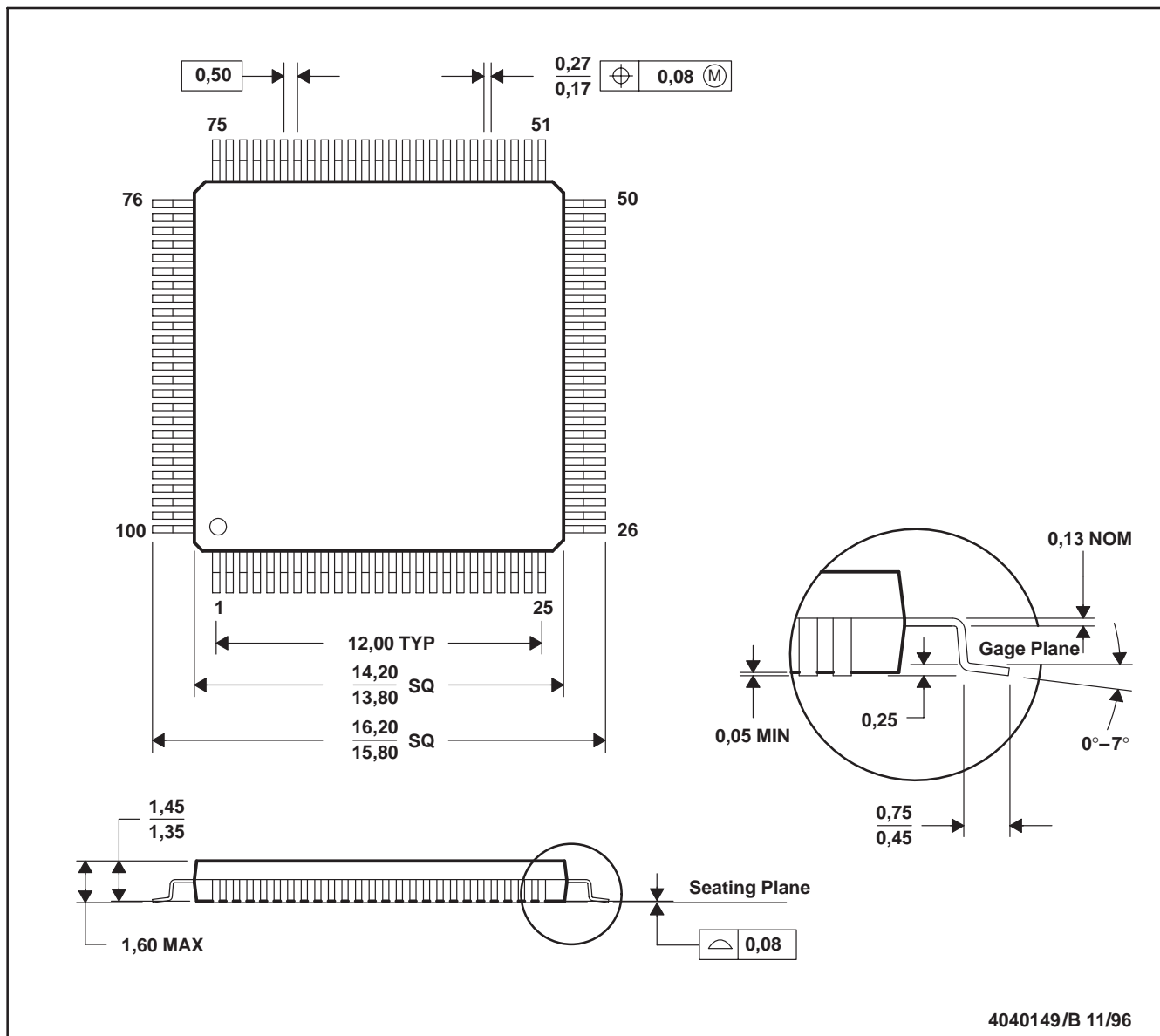
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PZ (S-PQFP-G100)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-026

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Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
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