SL1461SA

Wideband PLL FM Demodulator

Advance Information

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The SL1461SA is a wideband PLL FM demodulator, intended primarily for application in satellite tuners.

The device contains all elements necessary, with the exception of external oscillator sustaining network and loop feedback components, to form a complete PLL system operating at frequencies up to 800MHz.

An AFC with window adjust is provided, whose output signal can be used to correct for any frequency drift at the head end local oscillator.

FEATURES

- Single chip PLL system for wideband FM demodulation
- Simple low component count application
- Allows for application of threshold extension
- Fully balanced low radiation design
- High operating input sensivity
- Improved VCO stability with variations in supply or temperature
- AGC detect and bias adjust
- 75Ω video output drive with low distortion levels
- Dynamic self biasing analog AFC
- Full ESD Protection*

* Normal ESD handling procedures should be observed

Ordering Information
SL1461SA/KG/MPAS

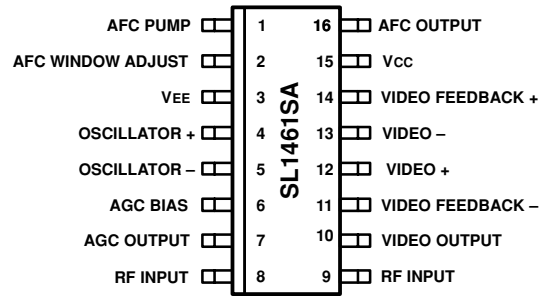


Fig.1 Pin connections - top view

APPLICATIONS

- Satellite receiver systems
- Data communications Systems

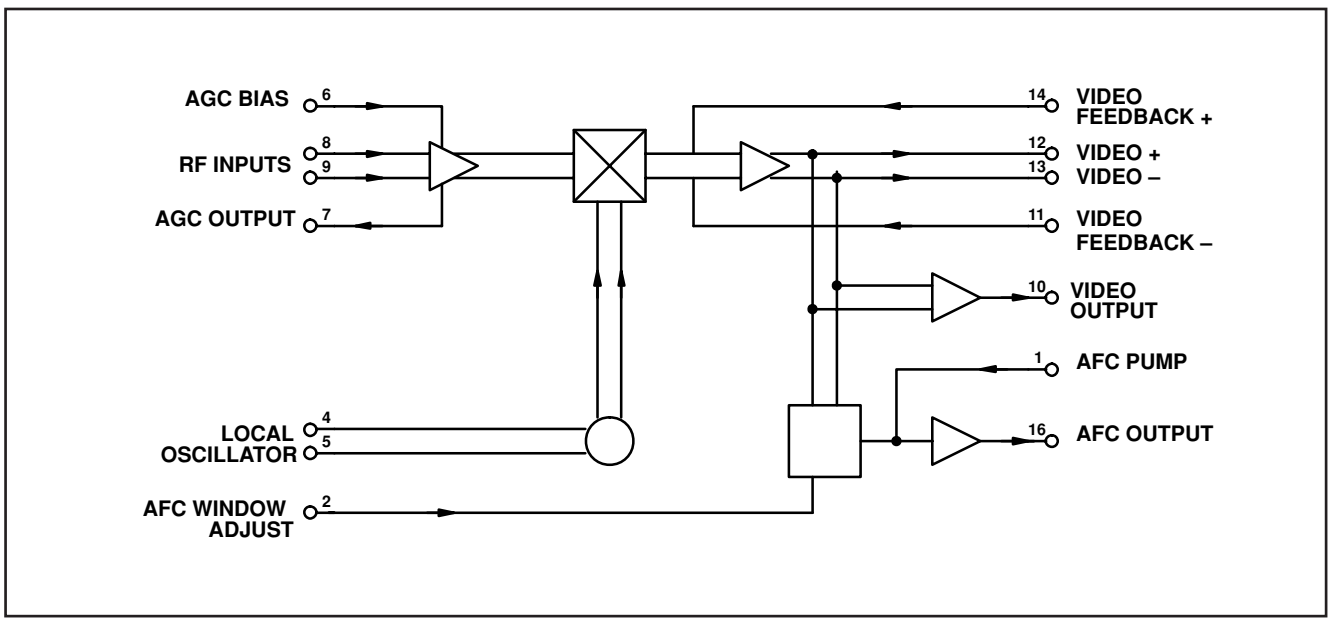


Fig.2 SL1461SA block diagram

ELECTRICAL CHARACTERISTICS

T_{amb} = -20°C to +80°C, V_{CC} = +4.5V to +5.5V. The electrical characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		36	40	mA	
Operating frequency	300		800	MHz	
Input sensitivity		-40		dBm	Preamp limiting
Input overload	0			dBm	
VCO sensitivity (dF/dV)	25	32	39	MHz/V	Refer to application in Fig. 3
VCO linearity		25		%	Refer to application in Fig. 3; with 13.5MHz p-p deviation
VCO supply stability		2.0		MHz/V	See note 5
VCO temperature stability		20		KHz/°C	See note 5
Phase detector gain		0.5		V/rad	Differential loop filter
		0.25		V/rad	Single ended loop filter
Loop amplifier input impedance	450	570	700	Ω	Single ended
Loop amplifier output impedance		25		Ω	Single ended
Loop amplifier open loop gain		38		dB	Single ended
Loop amplifier gain bandwidth product		240		MHz	Single ended
Loop amplifier output swing			1.2	Vp-p	Single ended
Video drive output impedance	55	75	95	Ω	
Video drive:					
Luminance nonlinearity		1.9	5	%	1KΩ load, See note 3 and 4
- differential gain		0.5	2.5	%	75KΩ load, See note 3 and 4
- differential phase		1.0	3	Degree	75KΩ load, See note 3 and 4
- intermodulation			-40	dB	See notes 1, 3 and 4
- signal/noise	66	72		dB	1KΩ load, See note 2 and 4
- Tilt		0.3	3	%	1KΩ load, See note 3 and 4
- baseline distortion		0.4	2	%	1KΩ load, See note 3 and 4
AGC output current	10		400	µA	Maximum load voltage drop 2V
AGC bias current	0		250	µA	
AFC window current	0		400	µA	400µA gives 1.5V deadband window
AFC charge pump current		50		µA	
AFC leakage current			10	µA	With charge pump disabled
AFC output saturation voltage			0.4	V	AFC output enabled

Note 1. Product of input modulation f_1 at 4.43MHz, 13.5MHz p–p deviation and f_2 at 6MHz p–p deviation, (PAL chroma and sound subcarriers).

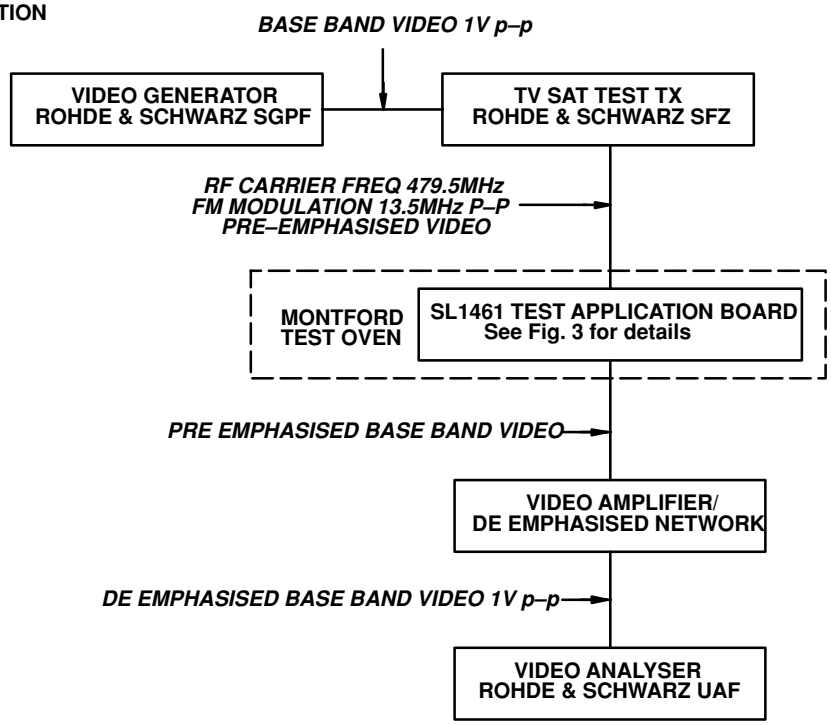
Note 2. Ratio of output video signal with input modulation at 1MHz, 13.5MHz p–p deviation, to output rms noise in 6MHz bandwidth with no input modulation.

Note 3. Input test signal pre–emphasised video 13.5MHz p–p deviation. Output voltage 600mV pk–pk.

Note 4. See page 3

Note 5. Assuming operating frequency of 479.5MHz set with V_{CC} @ 5.0V and ambient temperature of +20°C. Only applies to Application shown in Fig. 3. also refer to Fig. 8.

TEST CONFIGURATION



The video drive characteristics measurements were made using the above test configuration. The maximum figures recorded in the Electrical Characteristics Table coincide with high temperatures and extremes of supply voltage. No adjustment to the recorded figures has been made to compensate for the effects of temperature on the external components of the application test board, in particular the varactor diodes. If operation of the device at high ambient temperatures is envisaged then attention to temperature compensation of the external circuitry will result in performance figures closer to the stated typical figures.

Fig.2 SL1461SA block diagram

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} at 0V

Characteristics	Min.	Typ.	Max.	Conditions
Supply voltage	-0.3	7	V	
RF input voltage		2.5	Vp-p	
RF input DC offset	-0.3	V_{CC}+0.3	V	
Oscillator ± DC offset	-0.3	V_{CC}+0.3	V	
Video ± DC offset	-0.3	V_{CC}+0.3	V	
Video feedback ± DC offset	-0.3	V_{CC}+0.3	V	
Video output DC offset	-0.3	V_{CC}+0.3	V	
AFC pump DC offset	-0.3	V_{CC}+0.3	V	
AFC disable DC offset	-0.3	V_{CC}+0.3	V	
AFC deadband DC offset	-0.3	V_{CC}+0.3	V	
AGC bias DC offset	-0.3	V_{CC}+0.3	V	
AGC output DC offset	-0.3	V_{CC}+0.3	V	
Storage temperature	-55	125	°C	
Junction temperature		150	°C	
MP16 package thermal resistance, chip to ambient		111	°C/W	

ABSOLUTE MAXIMUM RATINGS cont.

All voltages are referred to V_{EE} at 0V

Characteristics	Min.	Typ.	Max.	Conditions
MP16 package thermal resistance, chip to case		41	°C/W	
Power consumption at 5.5V		250	mW	
ESD protection - pins 1 to 15	2		kV	Mil-std-883 method 3015 class 1
ESD protection - Pin 16	1.7		kV	Mil-std-883 method 3015 class 1

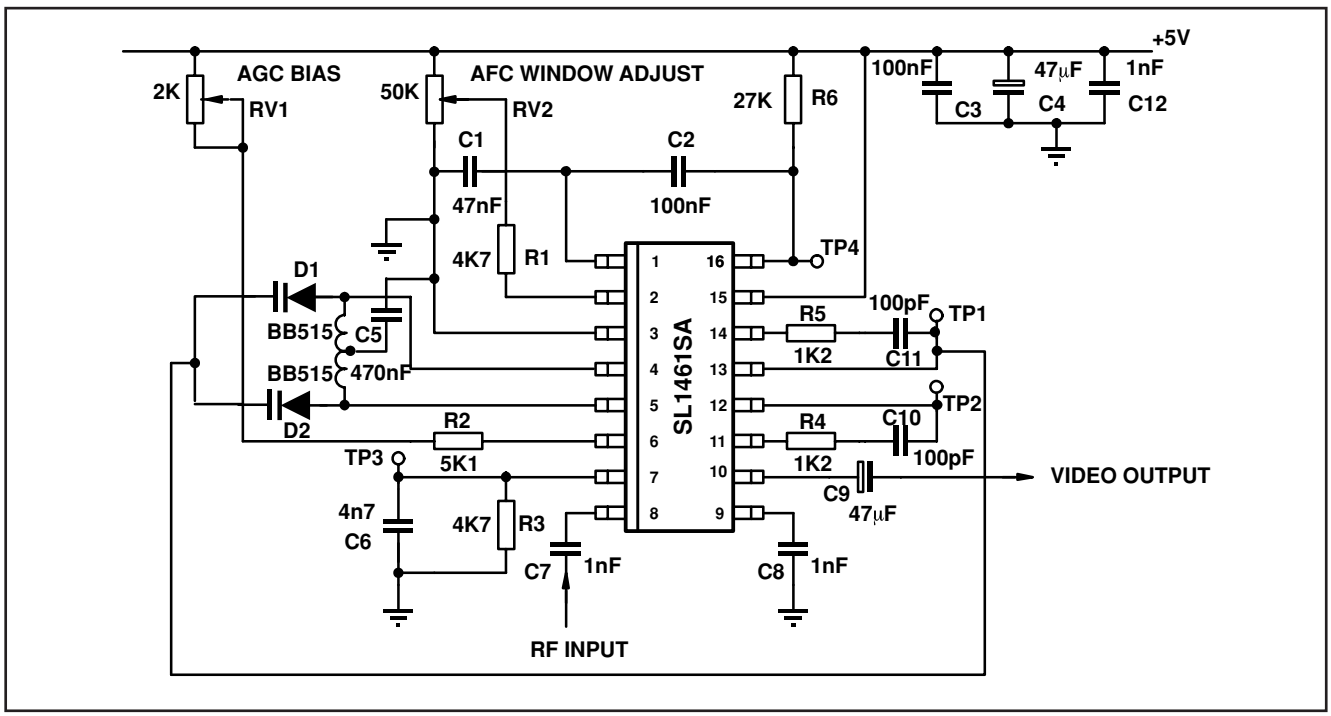


Fig.3 Standard application circuit

FUNCTIONAL DESCRIPTION

The SL1461SA is a wideband PLL FM demodulator, optimised for application in satellite receiver systems and requiring a minimum external component count. It contains all the elements required for construction of a phase locked loop circuit, with the exception of tuning components for the local oscillator, and an AFC detector circuit for generation of error signal to correct for any frequency drift in the outdoor unit local oscillator. A block diagram is contained in Fig. 2 and the typical application in Fig. 3.

The internal pin connections are contained in Fig.6/6a

In normal applications the second satellite IF frequency of typically 402 or 479.5MHz is fed to the RF preamplifier, which has a working sensitivity of typically -40 dBm, depending on application and layout. The preamplifier contains an RF level detect circuit, which generates an AGC signal that can be used for controlling the gain of the IF amplifier stages, so maintaining a fixed level to the RF input of the SL1461SA, for optimum threshold performance. The bias point of the AGC circuit can be adjusted to cater for variation in AGC line voltage requirement and device input power. The typical AGC curves are shown in Fig. 9. It is recommended that the device is operated with an input signal between -30 and -35dBm. This ensures optimum linearity and threshold performance, and gives a good safety margin over the typical sensitivity of
-40dBm.

The output of the preamplifier is fed to the mixer section which is of balanced design for low radiation. In this stage the RF signal is mixed with the local oscillator frequency, which is generatedby an on–board oscillator. The oscillator block uses an external varactor tuned sustaining network and is optimised for high linearity over the normal deviation range. A typical frequency versus voltage characteristic for the oscillator is contained in Fig. 7. The loop output is designed to compensate for first order temperature variation effects; the typical stability is shown in Fig. 8

The output of the mixer is then fed to the loop amplifier around which feedback is applied to determine loop transfer characteristic . Feedback can be applied either in differential or single ended mode; if the appropriate phase detector gains are assumed in calculating loop filters, both modes should give the same loop response.

The loop amplifier drives a 75Ω output impedance buffer amplifier, which can either be connected to a 75Ω load or used to drive a high input impedance stage giving greater linearity and approximately 6dB higher demodulated signal output level.

DESIGN OF PLL LOOP PARAMETERS

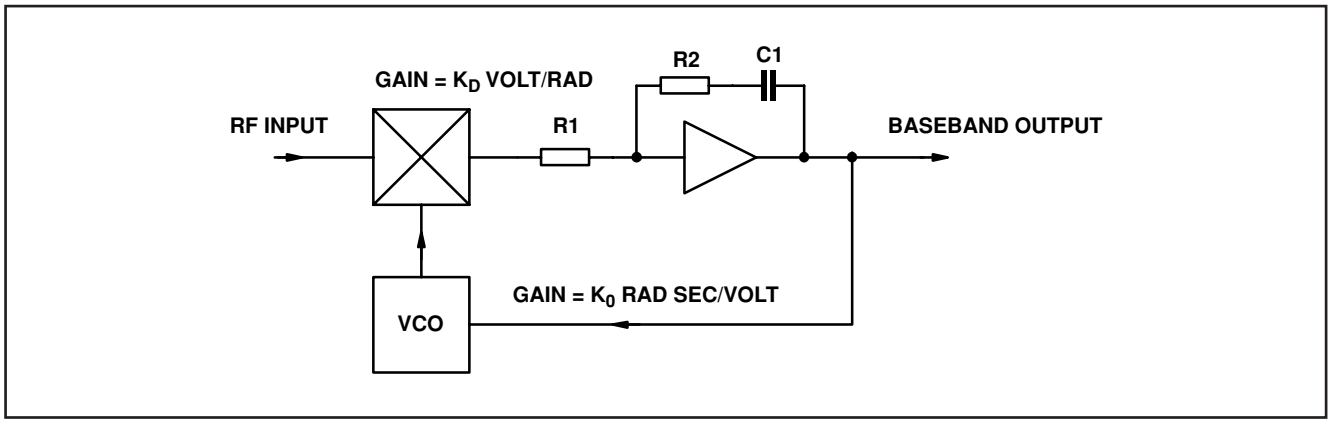


Fig.4

The SL1461SA is normally used as a type 1 second order loop and can be represented by the above diagram. For such a system the following parameters apply;

$$\tau_1 = C1 \cdot R1$$

$$\tau_2 = C1 \cdot R2$$

and

$$\tau_1 = \frac{K_0 K_D}{\omega_n^2}$$

$$\tau_2 = \frac{2\zeta}{\omega_n}$$

where:
K_0 is the VCO gain in radian seconds per volt
K_D is the phase detector gain in volts per radian
ω_n is the natural loop bandwidth
ζ is the loop damping factor
R1 is loop amplifier input impedance

Note: K_0 is dependant on sensitivity of VCO used.
K_D = 0.25V/rad single ended, 0.5V/rad differential

From these factors the loop 3dB bandwidth can be determined from the following expression;

$$\omega_{3dB}^2 = \omega_n^2(2\zeta^2 + 1) \pm \omega_n^2\sqrt{(2\zeta^2 + 1)^2 + 1}$$

Which approximates to $\omega_{3dB} = 2\omega_n$ when $\zeta = \frac{1}{\sqrt{2}}$

AFC FACILITY

The SL1461SA contains an analog frequency error detect circuit, which generates DC voltage proportional to the integral of frequency error. If the incident RF is high then the AFC voltage increases, if low then the voltage decreases. The AFC voltage can then be converted by an ADC to be read by the micro controller for frequency fine tuning; if used in an I^2C system it is recommended the device is used with either the SP5055 or SP5056 frequency synthesiser which contains an internal ADC readable via the I^2C bus.

The voltage corresponding to frequency alignment is arbitrary and user defined; if used with the SP5055 it is suggested the aligned voltage is 0.375 V_{CC} , corresponding to the centre code of the ADC on port 6.

The AFC detect circuit contains a deadband centre around the aligned frequency. The deadband can be adjusted from zero window to approximately 25MHz width assuming an oscillator dF/dV of 15MHz/V. If the incident RF is within this window the AFC voltage does not integrate, except by component leakage.

With reference to Fig.5; in normal operation the demodulated video is fed to a dual comparator where it is compared with two reference voltages, corresponding to the extremes of the deadband, or window. These voltages are variable and set by the window adjust input.

The comparators produce two digital outputs corresponding to voltages above or below the voltage window, or frequency above or below deadband. These digital control signals are used to control a complimentary current source pump. The current signals are then fed to the input of an amplifier which is arranged as an integrator, so integrating the
pulses into a DC voltage.

If the frequency is correctly aligned both the current source and sink are disabled, therefore the DC output voltage remains constant. There will be a small drift due to component leakage; the maximum drift can be calculated from;

$$\frac{dV}{dt} = \frac{I}{2500 \cdot C} \quad \text{where} \quad I = \frac{V_{CC}}{R_{EXT}}, \quad C = C_{EXT}$$

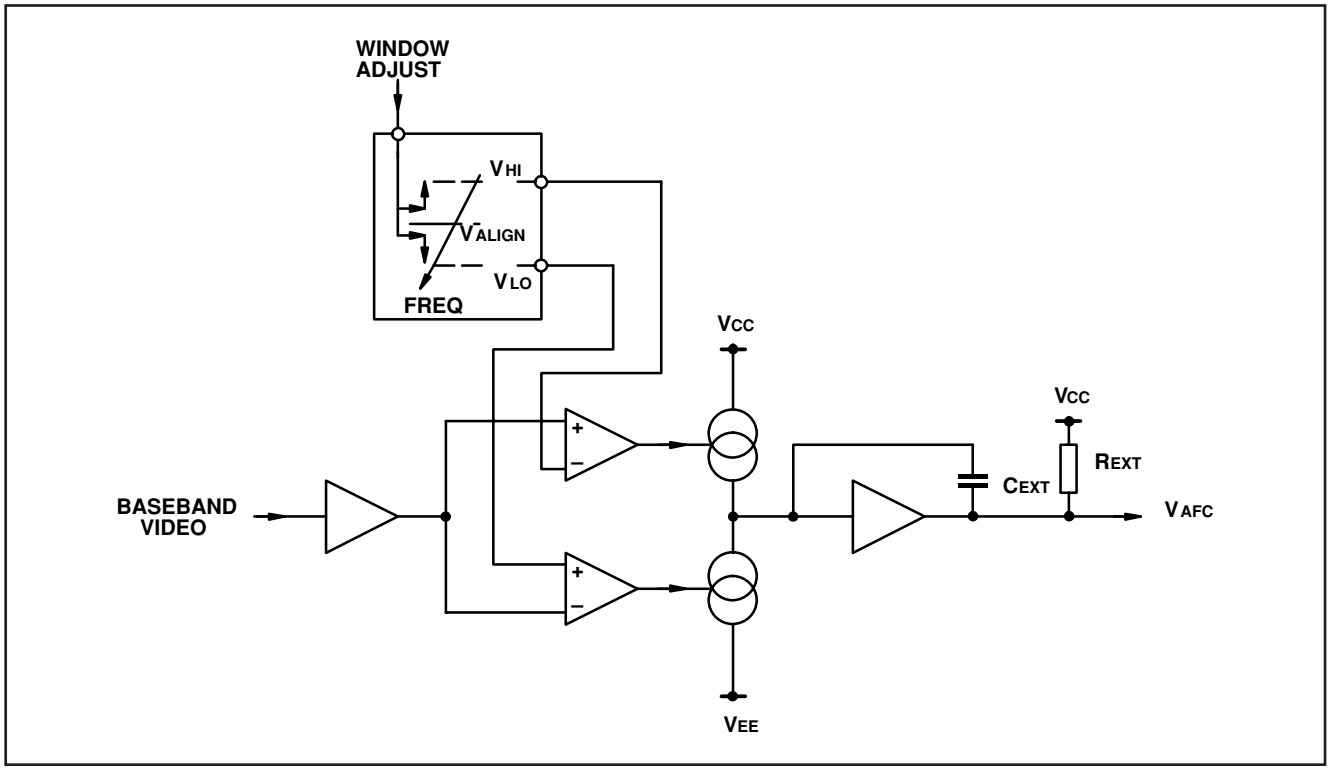
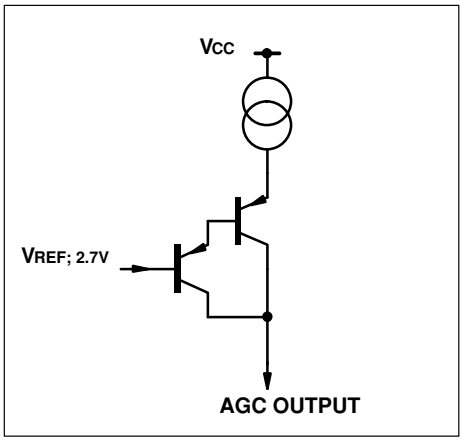
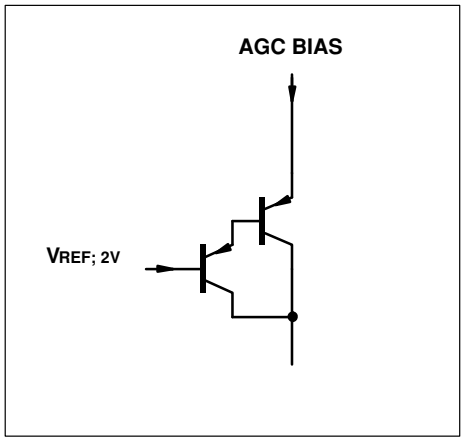


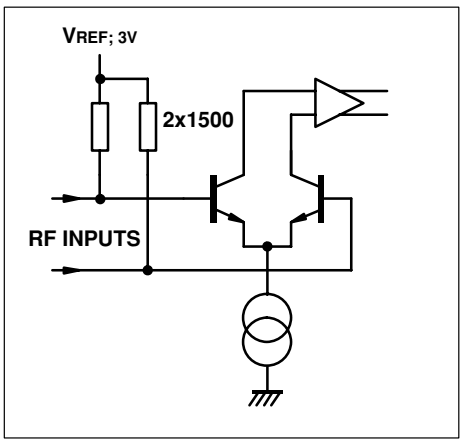
Fig.5 AFC system block diagram



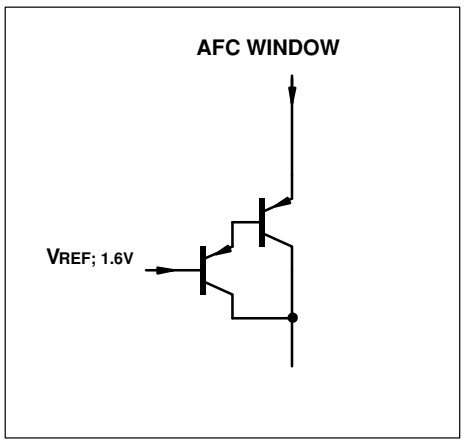
AGC output



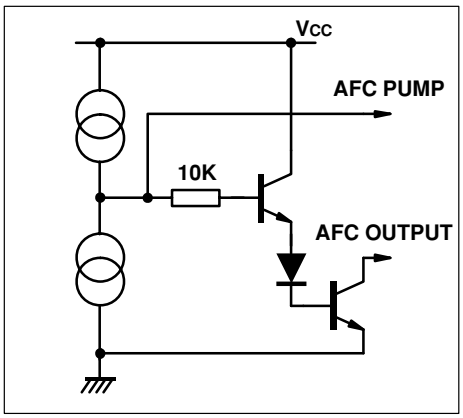
AGC bias adjust



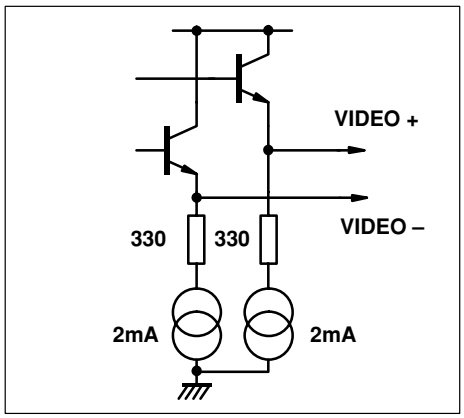
RF inputs



AFC window adjust

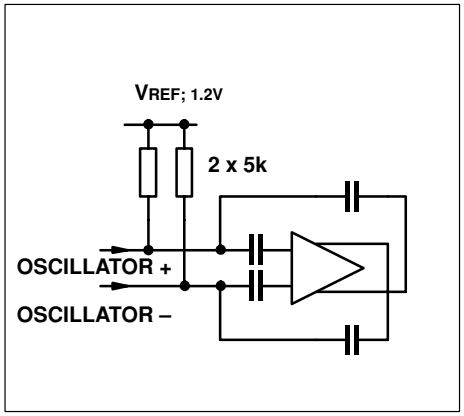


AFC output stage

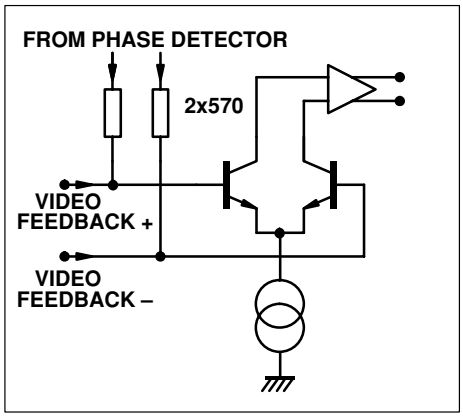


Video amp outputs

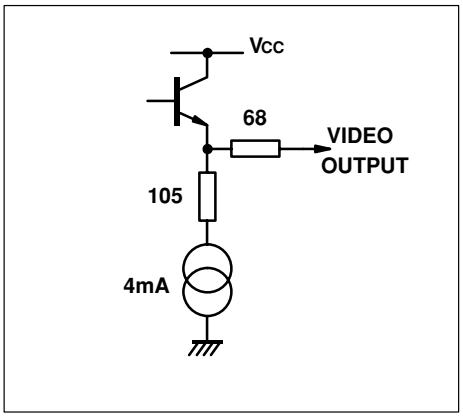
Fig.6 SL1461SA I/O port internal circuitry



Local oscillator



Video amp feedback inputs



Video output drive

Fig.6a SL1461SA I/O port internal circuitry

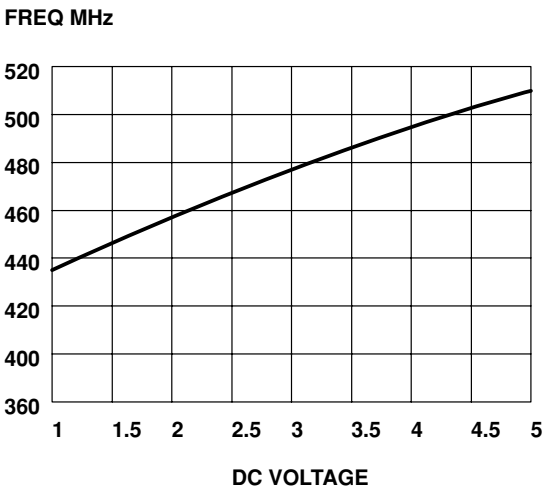


Fig.7 Typical VCO frequency vs DC control voltage

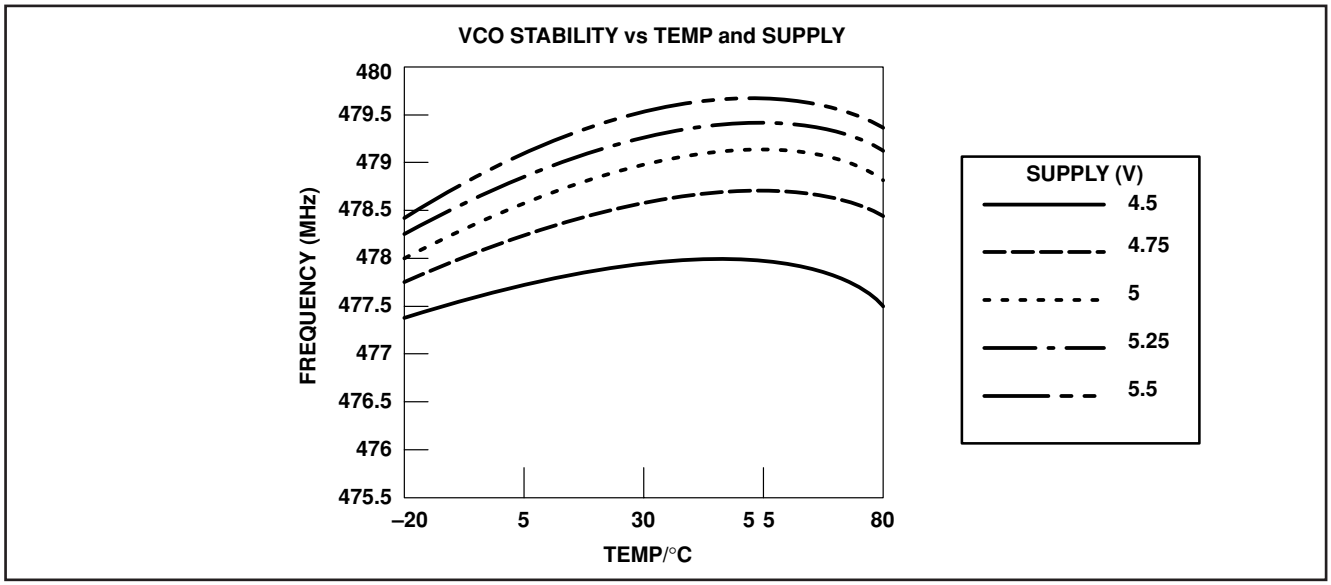


Fig.8 SL1461SA VCO centre frequency uncompensated temperature stability

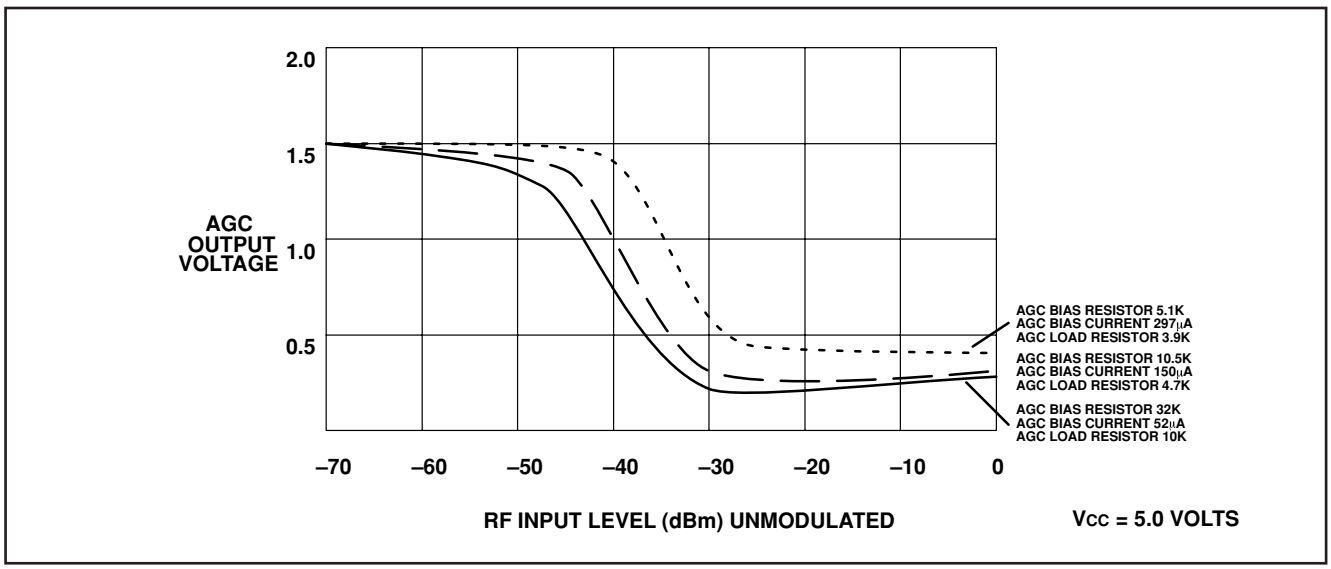


Fig.9 SL1461SA AGC output voltage for differing values of AGC bias resistor

APPLICATION NOTES

Capture range

Under conditions when there is no RF input signal present, the SL1461SA may react to spurious radiation from the free running oscillator coupling into the RF inputs. Because of the constant phase error between the VCO input to the phase detector and the spuriously coupled signal via the RF input, the phase comparator will drive the control voltage to either the bottom or the top of the range.

In such a case, the capture range will be asymmetrical about the VCO free running frequency, since any control voltage will only be able to tune the VCO in one direction if the tuning voltage is already at the max or min.

This effect can be avoided by driving the RF input differentially or achieving good common mode rejection to the VCO signal.

The lock range is independant of the above effects and will be symmetric about the centre of the phase detector S-curve provided the VCO is correctly aligned.

EXAMPLE

Loop out of lock

Tuning voltage =4.3V (maximum)

frequency =520MHz (maximum

It is only possible to capture signals below this frequency since the VCO is already at its maximum frequency.

Testing of capture range should be done with the device operating under normal conditions. An input signal of between -35dBm to -10dBm is suitable for such a measurement.

Lock range

Lock range should be symmetric about the centre of the S-curve. When the oscillator is sitting in the centre of the S-curve, the two video outputs will be at the same DC voltage.

RF oscillator design

The standard application circuit for the SL1461SA is shown in Fig.3 The layout of the VCO tank should follow normal good RF techniques - ie as compact as possible. This will minimise parasitics, thus giving improved VCO linearity and stability. The PCB layout used for testing purpose is shown in Fig. 10.

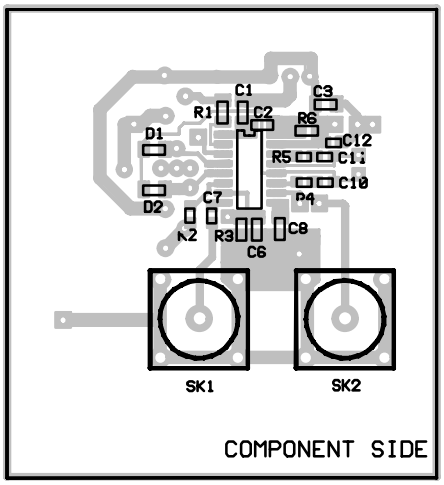
Setting up of oscillator

The VCO should be set up so that the desired input RF frequency is at the centre of the lock range. This will coincide with the centre of the S-curve and the point at which the AFC toggles when set to zero deadband.

The easiest way to centralise the VCO is to input an RF carrier which is being modulated by a low frequency squarewave. The tuning coil(s) should be adjusted until the AFC voltage toggles between 0.2V and $V_{CC-0.7V}$. The smaller the FM deviation of the squarewave used, the more accurate the setting will be.

A pre-emphasised video input containing black to white transitions can also be used for this setting, since the DC content in a pre-emphased video is much less than that in non pre–emphasised video. This is important as any dc content in the input waveform will introduce an offset in the AFC transition point.

The setting can be confirmed by measuring the DC voltage on the two video outputs, the voltages should be the same when the oscillator is centred around the incoming frequency. This DC measurement must be carried out with an unmodulated carrier of the required frequency. Modulation must not be present, since by definition, the dc voltages would be changing, thus making accurate measurement difficult.



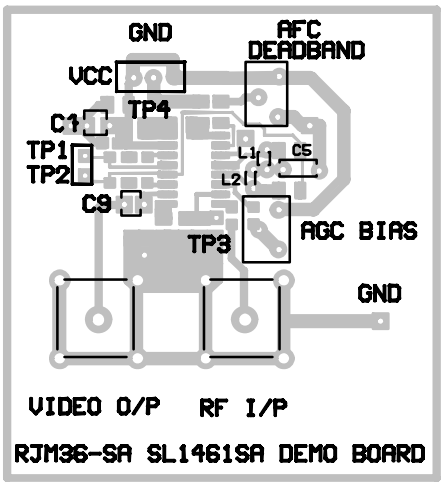
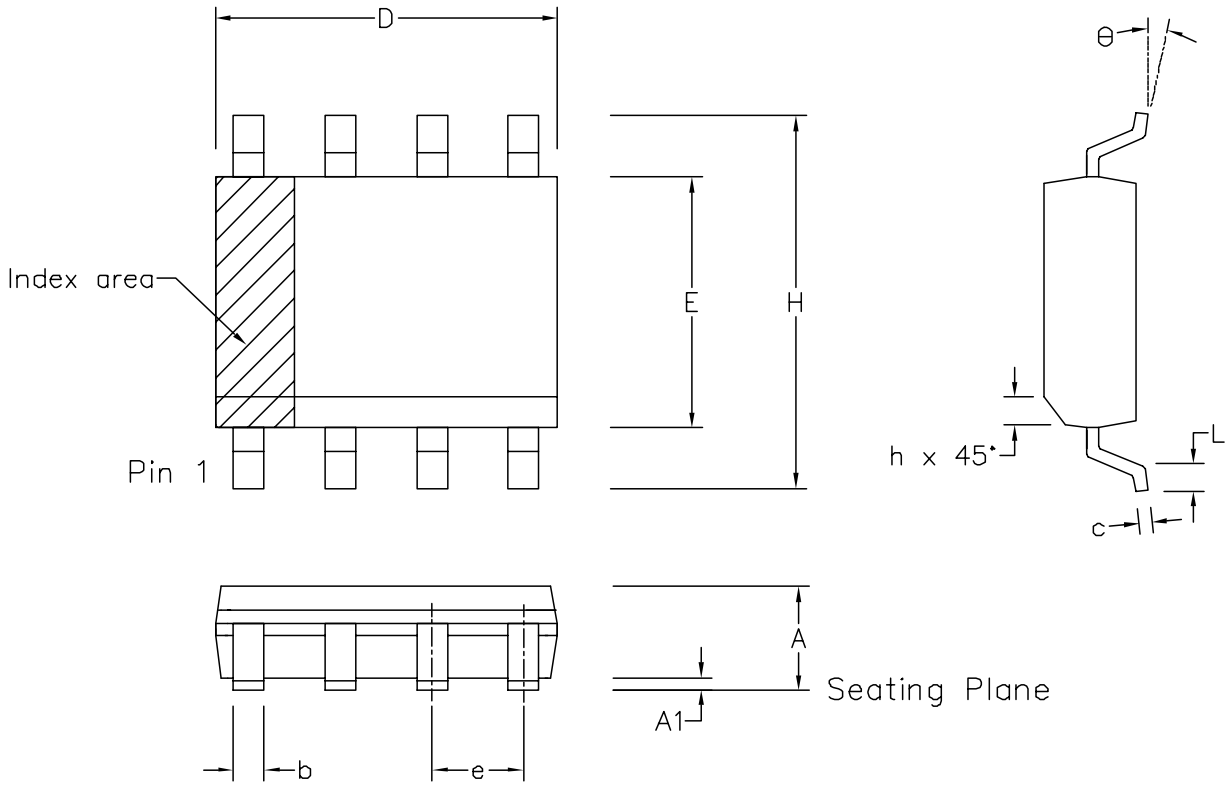


Fig.10 Layout of demo board with component locations



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	9.80	10.00	0.386	0.394
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
Θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	16		16	
Conforms to JEDEC MS-012AC Iss. C				

Notes:
1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	4	
ACN	006745	201938	202597	203706	
DATE	7APR95	27FEB97	12JUN97	9DEC97	
APPROVED					

ORIGINATING SITE: SWINDON

Title: Package Outline Drawing for 16 lds SOIC(N)-0.150" Body Width (MP)

Drawing Number
GPD00012

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