

FEATURES

- Member of the Texas Instruments Widebus™ Family
- Max t_{pd} of 5.8 ns at 3.3 V
- ± 24 -mA Output Drive at 3.3 V
- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- Latch-Up Performance Exceeds 250 mA Per JESD 17

NOTE: New and improved versions of the SN74ALVC164245 are available. The new part numbers are SN74LVC16T245 and SN74LVCH16T245 and should be considered for new designs.

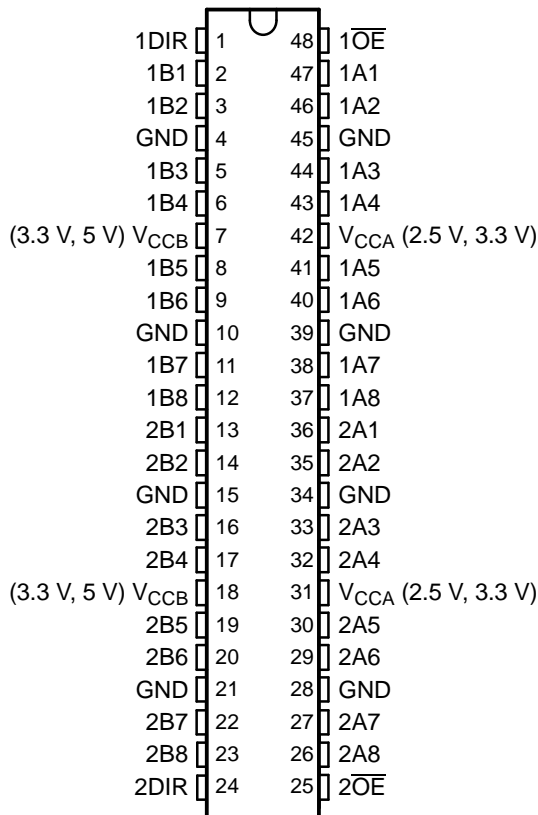
DESCRIPTION/ORDERING INFORMATION

This 16-bit (dual-octal) noninverting bus transceiver contains two separate supply rails. B port has V_{CCB} , which is set to operate at 3.3 V and 5 V. A port has V_{CCA} , which is set to operate at 2.5 V and 3.3 V. This allows for translation from a 2.5-V to a 3.3-V environment, and vice versa, or from a 3.3-V to a 5-V environment, and vice versa.

The SN74ALVC164245 is designed for asynchronous communication between data buses. The control circuitry (1DIR, 2DIR, $1\overline{OE}$, and $2\overline{OE}$) is powered by V_{CCA} .

To ensure the high-impedance state during power up or power down, the output-enable (\overline{OE}) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DGG OR DL PACKAGE
(TOP VIEW)



ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|---------------|--|------------------|
| -40°C to 85°C | FBGA – GRD | Tape and reel | 74ALVC164245GRDR | VC4245 |
| | FBGA – ZRD (Pb-free) | | 74ALVC164245ZRDR | |
| | SSOP – DL | Tube of 25 | SN74ALVC164245DL | ALVC164245 |
| | | Reel of 1000 | SN74ALVC164245DLR 74ALVC164245DLRG4 | |
| | TSSOP – DGG | Reel of 2000 | SN74ALVC164245DGGR | ALVC164245 |
| | | | 74ALVC164245DGGRG4 | |
| | | Reel of 250 | SN74ALVC164245DGGT | |
| | | | 74ALVC164245DGGTE4 | |
| | VFBGA – GQL | Reel of 1000 | SN74ALVC164245KR | VC4245 |
| | VFBGA – ZQL (Pb-free) | | 74ALVC164245ZQLR | |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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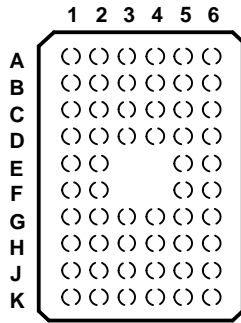
SN74ALVC164245
16-BIT 2.5-V TO 3.3-V/3.3-V TO 5-V LEVEL-SHIFTING TRANSCEIVER
WITH 3-STATE OUTPUTS

SCAS416P—MARCH 1994—REVISED NOVEMBER 2005

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The logic levels of the direction-control (DIR) input and the output-enable (\overline{OE}) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ} .

GQL OR ZQL PACKAGE
(TOP VIEW)

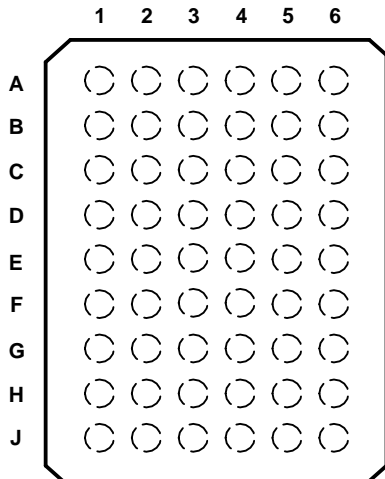


TERMINAL ASSIGNMENTS⁽¹⁾
(56-Ball GQL/ZQL Package)

| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|------|-----|------------------|------------------|-----|-------------------|
| A | 1DIR | NC | NC | NC | NC | 1 \overline{OE} |
| B | 1B2 | 1B1 | GND | GND | 1A1 | 1A2 |
| C | 1B4 | 1B3 | V _{CCB} | V _{CCA} | 1A3 | 1A4 |
| D | 1B6 | 1B5 | GND | GND | 1A5 | 1A6 |
| E | 1B8 | 1B7 | | | 1A7 | 1A8 |
| F | 2B1 | 2B2 | | | 2A2 | 2A1 |
| G | 2B3 | 2B4 | GND | GND | 2A4 | 2A3 |
| H | 2B5 | 2B6 | V _{CCB} | V _{CCA} | 2A6 | 2A5 |
| J | 2B7 | 2B8 | GND | GND | 2A8 | 2A7 |
| K | 2DIR | NC | NC | NC | NC | 2 \overline{OE} |

(1) NC – No internal connection

GRD OR ZRD PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS⁽¹⁾
(54-Ball GRD/ZRD Package)

| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|-----|-----|------------------|-------------------|-----|-----|
| A | 1B1 | NC | 1DIR | 1 \overline{OE} | NC | 1A1 |
| B | 1B3 | 1B2 | NC | NC | 1A2 | 1A3 |
| C | 1B5 | 1B4 | V _{CCB} | V _{CCA} | 1A4 | 1A5 |
| D | 1B7 | 1B6 | GND | GND | 1A6 | 1A7 |
| E | 2B1 | 1B8 | GND | GND | 1A8 | 2A1 |
| F | 2B3 | 2B2 | GND | GND | 2A2 | 2A3 |
| G | 2B5 | 2B4 | V _{CCB} | V _{CCA} | 2A4 | 2A5 |
| H | 2B7 | 2B6 | NC | NC | 2A6 | 2A7 |
| J | 2B8 | NC | 2DIR | 2 \overline{OE} | NC | 2A8 |

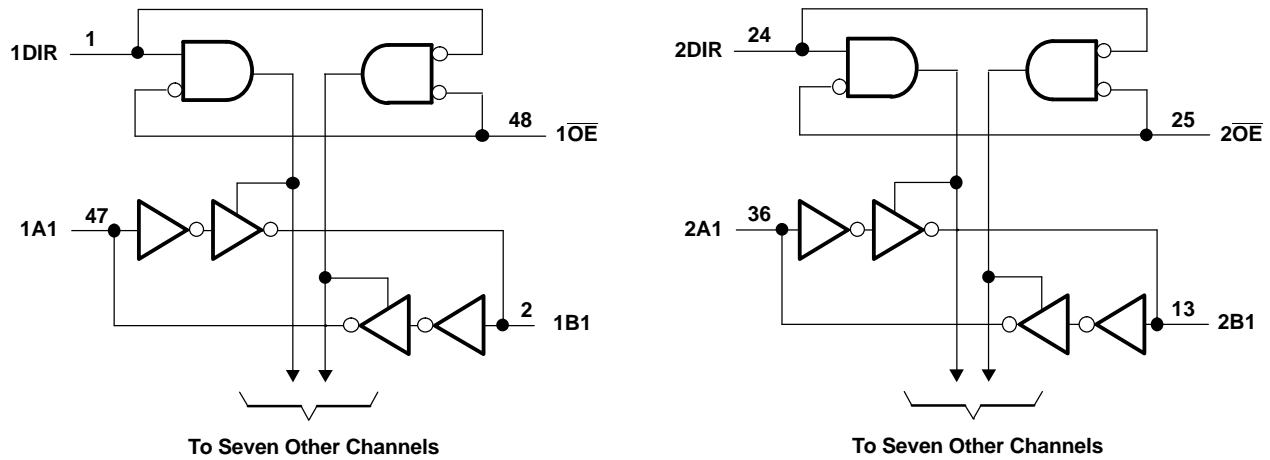
(1) NC – No internal connection

FUNCTION TABLE⁽¹⁾
(EACH 8-BIT SECTION)

| CONTROL INPUTS | | OUTPUT CIRCUITS | | OPERATION |
|-----------------|-----|-----------------|---------|-----------------|
| \overline{OE} | DIR | A PORT | B PORT | |
| L | L | Enabled | Hi-Z | B data to A bus |
| L | H | Hi-Z | Enabled | A data to B bus |
| H | X | Hi-Z | Hi-Z | Isolation |

(1) Input circuits of the data I/Os always are active.

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range for V_{CCB} at 5 V and V_{CCA} at 3.3 V (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---------------|---|---------------------------------|------|-----------------|------|
| V_{CC} | Supply voltage range | V_{CCA} | -0.5 | 4.6 | V |
| | | V_{CCB} | -0.5 | 6 | |
| V_I | Input voltage range | Except I/O ports ⁽²⁾ | -0.5 | 6 | V |
| | | I/O port A ⁽³⁾ | -0.5 | $V_{CCA} + 0.5$ | |
| | | I/O port B ⁽²⁾ | -0.5 | $V_{CCB} + 0.5$ | |
| I_{IK} | Input clamp current | $V_I < 0$ | | -50 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ | | -50 | mA |
| I_O | Continuous output current | | | ± 50 | mA |
| | Continuous current through each V_{CC} or GND | | | ± 100 | mA |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | DGG package | | 70 | °C/W |
| | | DL package | | 63 | |
| | | GQL/ZQL package | | 42 | |
| | | GRD/ZRD package | | 36 | |
| T_{stg} | Storage temperature range | | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) This value is limited to 6 V maximum.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

SN74ALVC164245
16-BIT 2.5-V TO 3.3-V/3.3-V TO 5-V LEVEL-SHIFTING TRANSCEIVER
WITH 3-STATE OUTPUTS

SCAS416P—MARCH 1994—REVISED NOVEMBER 2005

Recommended Operating Conditions⁽¹⁾

for V_{CCB} at 3.3 V and 5 V

| | | MIN | MAX | UNIT |
|---------------------|------------------------------------|---|-----------|------|
| V_{CCB} | Supply voltage | 3 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | V |
| V_{IL} | Low-level input voltage | $V_{CCB} = 3 \text{ V to } 3.6 \text{ V}$ | | V |
| | | $V_{CCB} = 4.5 \text{ V to } 5.5 \text{ V}$ | | |
| V_{IB} | Input voltage | 0 | V_{CCB} | V |
| V_{OB} | Output voltage | 0 | V_{CCB} | V |
| I_{OH} | High-level output current | | -24 | mA |
| I_{OL} | Low-level output current | | 24 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | ns/V |
| T_A | Operating free-air temperature | -40 | 85 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Recommended Operating Conditions⁽¹⁾

for V_{CCA} at 2.5 V and 3.3 V

| | | MIN | MAX | UNIT |
|---------------------|------------------------------------|---|-----------|------|
| V_{CCA} | Supply voltage | 2.3 | 3.6 | V |
| V_{IH} | High-level input voltage | $V_{CCA} = 2.3 \text{ V to } 2.7 \text{ V}$ | | V |
| | | $V_{CCA} = 3 \text{ V to } 3.6 \text{ V}$ | | |
| V_{IL} | Low-level input voltage | $V_{CCA} = 2.3 \text{ V to } 2.7 \text{ V}$ | | V |
| | | $V_{CCA} = 3 \text{ V to } 3.6 \text{ V}$ | | |
| V_{IA} | Input voltage | 0 | V_{CCA} | V |
| V_{OA} | Output voltage | 0 | V_{CCA} | V |
| I_{OH} | High-level output current | $V_{CCA} = 2.3 \text{ V}$ | | mA |
| | | $V_{CCA} = 3 \text{ V}$ | | |
| I_{OL} | Low-level output current | $V_{CCA} = 2.3 \text{ V}$ | | mA |
| | | $V_{CCA} = 3 \text{ V}$ | | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | ns/V |
| T_A | Operating free-air temperature | -40 | 85 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range for $V_{CCA} = 2.7\text{ V to }3.6\text{ V}$ and $V_{CCB} = 4.5\text{ V to }5.5\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CCA} | V_{CCB} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-----------------------|----------------|---|----------------|----------------|----------------|--------------------|----------|---------------|
| V_{OH} | B to A | $I_{OH} = -100\ \mu\text{A}$ | 2.7 V to 3.6 V | | $V_{CC} - 0.2$ | | | V |
| | | $I_{OH} = -12\ \text{mA}$ | 2.7 V | | 2.2 | | | |
| | | $I_{OH} = -24\ \text{mA}$ | 3 V | | 2.4 | | | |
| | A to B | $I_{OH} = -100\ \mu\text{A}$ | | 4.5 V | 4.3 | | | |
| | | | | 5.5 V | 5.3 | | | |
| | | $I_{OH} = -24\ \text{mA}$ | | 4.5 V | 3.7 | | | |
| | | | 5.5 V | 4.7 | | | | |
| V_{OL} | B to A | $I_{OL} = 100\ \mu\text{A}$ | 2.7 V to 3.6 V | | | | 0.2 | V |
| | | $I_{OL} = 12\ \text{mA}$ | 2.7 V | | | | 0.4 | |
| | | $I_{OL} = 24\ \text{mA}$ | 3 V | | | | 0.55 | |
| | A to B | $I_{OL} = 100\ \mu\text{A}$ | | 4.5 V to 5.5 V | | | 0.2 | |
| | | | | 4.5 V to 5.5 V | | | 0.55 | |
| | | $I_{OL} = 24\ \text{mA}$ | | | | | | |
| I_I | Control inputs | $V_I = V_{CCA}/V_{CCB}$ or GND | 3.6 V | 5.5 V | | | ± 5 | μA |
| $I_{OZ}^{(2)}$ | A or B port | $V_O = V_{CCA}/V_{CCB}$ or GND | 3.6 V | 5.5 V | | | ± 10 | μA |
| I_{CC} | | $V_I = V_{CCA}/V_{CCB}$ or GND, $I_O = 0$ | 3.6 V | 5.5 V | | | 40 | μA |
| $\Delta I_{CC}^{(3)}$ | | One input at $V_{CCA}/V_{CCB} - 0.6\text{ V}$, Other inputs at V_{CCA}/V_{CCB} or GND | 3 V to 3.6 V | 4.5 V to 5.5 V | | | 750 | μA |
| C_i | Control inputs | $V_I = V_{CCA}/V_{CCB}$ or GND | 3.3 V | 5 V | | 6.5 | | pF |
| C_{io} | A or B port | $V_O = V_{CCA}/V_{CCB}$ or GND | 3.3 V | 3.3 V | | 8.5 | | pF |

(1) Typical values are measured at $V_{CCA} = 3.3\text{ V}$ and $V_{CCB} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

(2) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(3) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than at 0 or the associated V_{CC} .

Electrical Characteristics

over recommended operating free-air temperature range for $V_{CCA} = 2.3\text{ V to }2.7\text{ V}$ and $V_{CCB} = 3\text{ V to }3.6\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CCA} | V_{CCB} | MIN | MAX | UNIT |
|-----------------------|----------------|---|----------------|--------------|-----------------|----------|---------------|
| V_{OH} | B to A | $I_{OH} = -100\ \mu\text{A}$ | 2.3 V to 2.7 V | 3 V to 3.6 V | $V_{CCA} - 0.2$ | | V |
| | | $I_{OH} = -8\ \text{mA}$ | 2.3 V | 3 V to 3.6 V | 1.7 | | |
| | | $I_{OH} = -12\ \text{mA}$ | 2.7 V | 3 V to 3.6 V | 1.8 | | |
| | A to B | $I_{OH} = -100\ \mu\text{A}$ | 2.3 V to 2.7 V | 3 V to 3.6 V | $V_{CCB} - 0.2$ | | |
| | | $I_{OH} = -18\ \text{mA}$ | 2.3 V to 2.7 V | 3 V | 2.2 | | |
| | | | | | | | |
| V_{OL} | B to A | $I_{OL} = 100\ \mu\text{A}$ | 2.3 V to 2.7 V | 3 V to 3.6 V | | 0.2 | V |
| | | $I_{OL} = 12\ \text{mA}$ | 2.3 V | 3 V to 3.6 V | | 0.6 | |
| | A to B | $I_{OL} = 100\ \mu\text{A}$ | 2.3 V to 2.7 V | 3 V to 3.6 V | | 0.2 | |
| | | $I_{OL} = 18\ \text{mA}$ | 2.3 V | 3 V | | 0.55 | |
| I_I | Control inputs | $V_I = V_{CCA}/V_{CCB}$ or GND | 2.3 V to 2.7 V | 3 V to 3.6 V | | ± 5 | μA |
| $I_{OZ}^{(1)}$ | A or B port | $V_O = V_{CCA}/V_{CCB}$ or GND | 2.3 V to 2.7 V | 3 V to 3.6 V | | ± 10 | μA |
| I_{CC} | | $V_I = V_{CCA}/V_{CCB}$ or GND, $I_O = 0$ | 2.3 V to 2.7 V | 3 V to 3.6 V | | 20 | μA |
| $\Delta I_{CC}^{(2)}$ | | One input at $V_{CCA}/V_{CCB} - 0.6\text{ V}$, Other inputs at V_{CCA}/V_{CCB} or GND | 2.3 V to 2.7 V | 3 V to 3.6 V | | 750 | μA |

(1) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than at 0 or the associated V_{CC} .

SN74ALVC164245
16-BIT 2.5-V TO 3.3-V/3.3-V TO 5-V LEVEL-SHIFTING TRANSCEIVER
WITH 3-STATE OUTPUTS

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Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#) through [Figure 4](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$ | | $V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$ | | | | UNIT |
|-----------|-----------------|----------------|---|-----|---|-----|---|-----|------|
| | | | $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ | | $V_{CCA} = 2.7\text{ V}$ | | $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A | B | 7.6 | | 5.9 | | 1 5.8 | | ns |
| | B | A | 7.6 | | 6.7 | | 1.2 5.8 | | |
| t_{en} | \overline{OE} | B | 11.5 | | 9.3 | | 1 8.9 | | ns |
| t_{dis} | \overline{OE} | B | 10.5 | | 9.2 | | 2.1 9.5 | | ns |
| t_{en} | \overline{OE} | A | 12.3 | | 10.2 | | 2 9.1 | | ns |
| t_{dis} | \overline{OE} | A | 9.3 | | 9 | | 2.9 8.6 | | ns |

Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | $V_{CCB} = 3.3\text{ V}$ | $V_{CCB} = 5\text{ V}$ | UNIT |
|--|----------------------|---|--------------------------|--------------------------|------|
| | | | $V_{CCA} = 2.5\text{ V}$ | $V_{CCA} = 3.3\text{ V}$ | |
| | | | TYP | TYP | |
| C_{pd} Power dissipation capacitance | Outputs enabled (B) | $C_L = 50\text{ pF}, f = 10\text{ MHz}$ | 55 | 56 | pF |
| | Outputs disabled (B) | | 27 | 6 | |
| | Outputs enabled (A) | $C_L = 50\text{ pF}, f = 10\text{ MHz}$ | 118 | 56 | |
| | Outputs disabled (A) | | 58 | 6 | |

POWER-UP CONSIDERATIONS⁽¹⁾

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. Take these precautions to guard against such power-up problems:

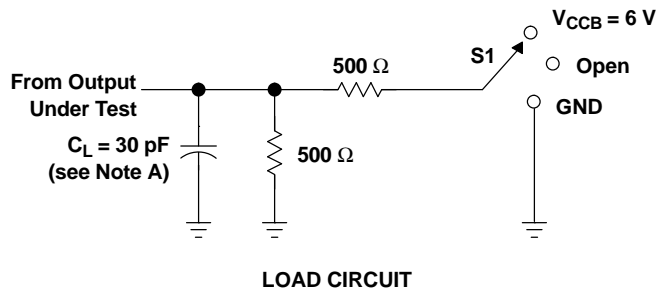
1. Connect ground before any supply voltage is applied.
 2. Power up the control side of the device (V_{CCA} for all four of these devices).
 3. Tie \overline{OE} to V_{CCA} with a pullup resistor so that it ramps with V_{CCA} .
 4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA} . Otherwise, keep DIR low.
- (1) Refer to the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, literature number SCEA021.

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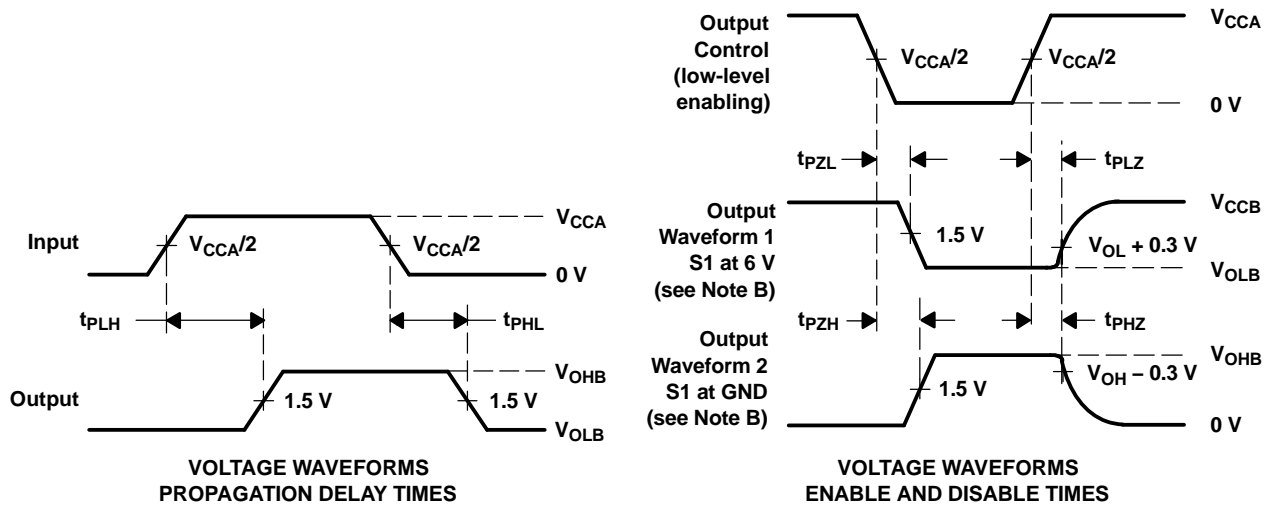
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PARAMETER MEASUREMENT INFORMATION

$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ to $V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$



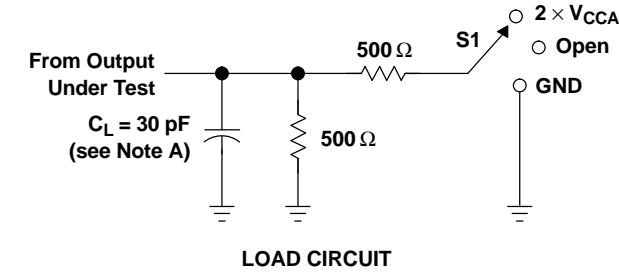
| TEST | S1 |
|-------------------|------------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | $V_{CCB} = 6\text{ V}$ |
| t_{PHZ}/t_{PZH} | GND |



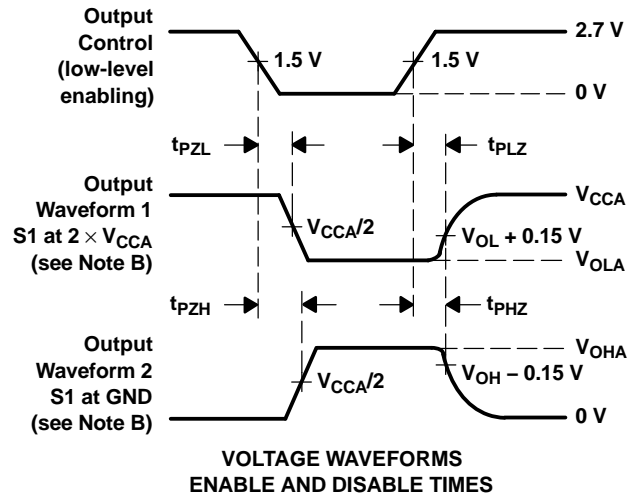
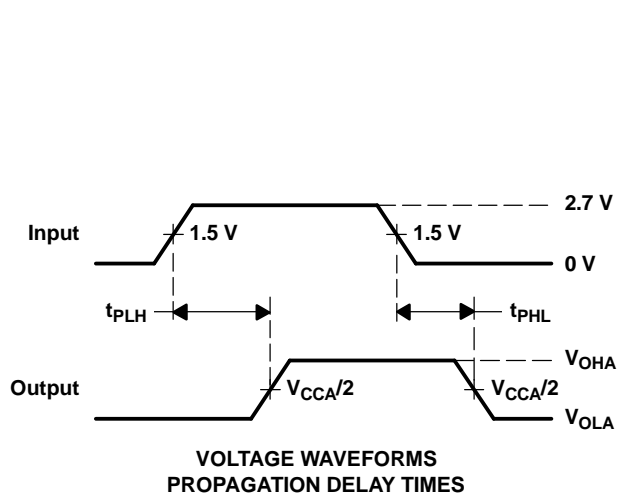
- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$ to $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$



| TEST | S1 |
|-------------------|--------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | 2 $\times V_{CCA}$ |
| t_{PHZ}/t_{PZH} | GND |

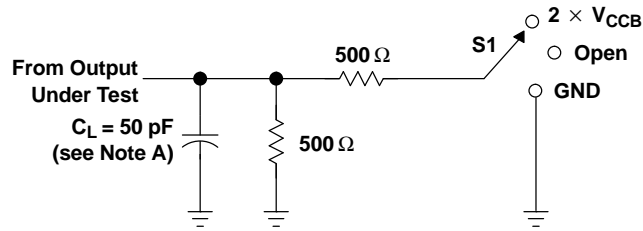


- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

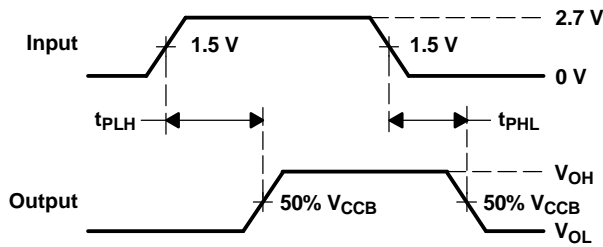
PARAMETER MEASUREMENT INFORMATION

$V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$ to $V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$

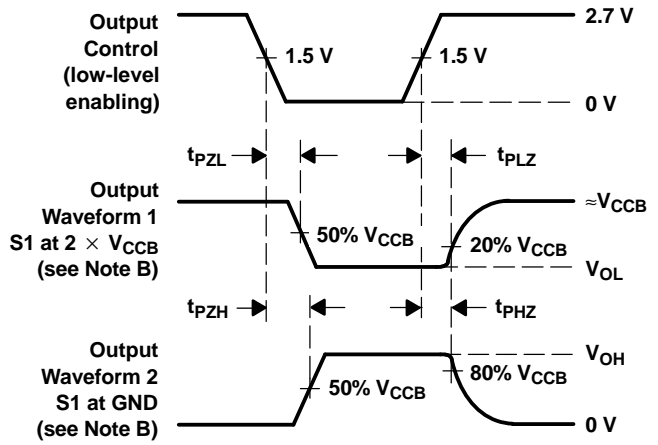


LOAD CIRCUIT

| TEST | S1 |
|-------------------|--------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CCB}$ |
| t_{PHZ}/t_{PZH} | GND |



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

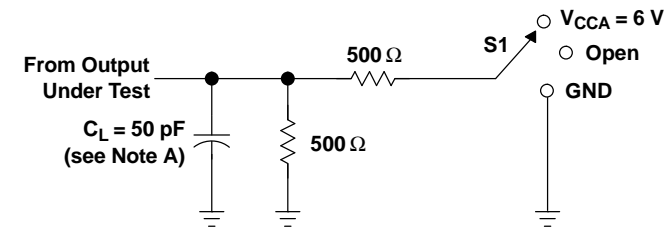


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

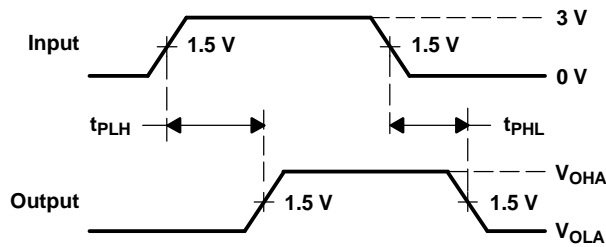
- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$ to $V_{CCA} = 2.7\text{ V}$ and $3.3\text{ V} \pm 0.3\text{ V}$

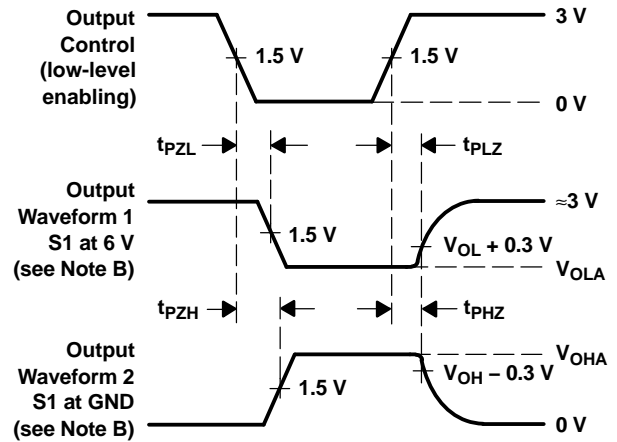


LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

| TEST | S1 |
|-------------------|------------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | $V_{CCA} = 6\text{ V}$ |
| t_{PHZ}/t_{PZH} | GND |



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|--------------------|-----------------------|----------------------------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 74ALVC164245DGGRE4 | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVC164245DGGRG4 | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVC164245DGGTE4 | ACTIVE | TSSOP | DGG | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVC164245DGGTG4 | ACTIVE | TSSOP | DGG | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVC164245DLG4 | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVC164245DLRG4 | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVC164245GRDR | ACTIVE | BGA MI CROSTA R JUNI OR | GRD | 54 | 1000 | TBD | SNPB | Level-1-240C-UNLIM |
| 74ALVC164245ZQLR | ACTIVE | BGA MI CROSTA R JUNI OR | ZQL | 56 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM |
| 74ALVC164245ZRDR | ACTIVE | BGA MI CROSTA R JUNI OR | ZRD | 54 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM |
| SN74ALVC164245DGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVC164245DGGT | ACTIVE | TSSOP | DGG | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVC164245DL | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVC164245DLR | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVC164245KR | ACTIVE | BGA MI CROSTA R JUNI OR | GQL | 56 | 1000 | TBD | SNPB | Level-1-240C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74ALVC164245 :

- Enhanced Product: [SN74ALVC164245-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|----------------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74ALVC164245GRDR | BGA MICROSTAR JUNIOR | GRD | 54 | 1000 | 330.0 | 16.4 | 5.8 | 8.3 | 1.55 | 8.0 | 16.0 | Q1 |
| 74ALVC164245ZQLR | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | 330.0 | 16.4 | 4.8 | 7.3 | 1.45 | 8.0 | 16.0 | Q1 |
| 74ALVC164245ZRDR | BGA MICROSTAR JUNIOR | ZRD | 54 | 1000 | 330.0 | 16.4 | 5.8 | 8.3 | 1.55 | 8.0 | 16.0 | Q1 |
| SN74ALVC164245DGGR | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 15.8 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74ALVC164245DGGT | TSSOP | DGG | 48 | 250 | 330.0 | 24.4 | 8.6 | 15.8 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74ALVC164245DLR | SSOP | DL | 48 | 1000 | 330.0 | 32.4 | 11.35 | 16.2 | 3.1 | 16.0 | 32.0 | Q1 |
| SN74ALVC164245KR | BGA MICROSTAR JUNIOR | GQL | 56 | 1000 | 330.0 | 16.4 | 4.8 | 7.3 | 1.45 | 8.0 | 16.0 | Q1 |

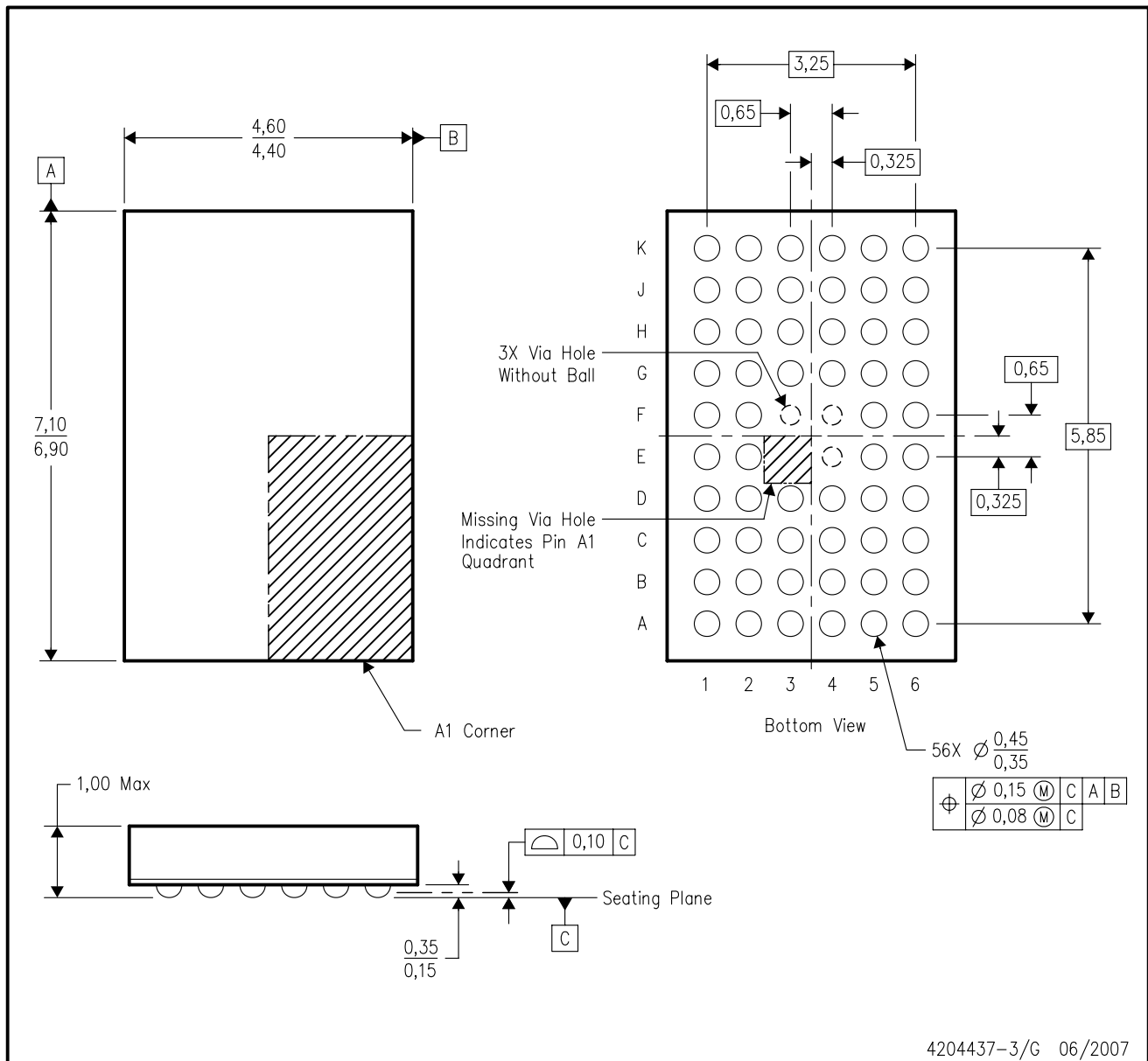
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|----------------------|-----------------|------|------|-------------|------------|-------------|
| 74ALVC164245GRDR | BGA MICROSTAR JUNIOR | GRD | 54 | 1000 | 346.0 | 346.0 | 33.0 |
| 74ALVC164245ZQLR | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | 346.0 | 346.0 | 33.0 |
| 74ALVC164245ZRDR | BGA MICROSTAR JUNIOR | ZRD | 54 | 1000 | 346.0 | 346.0 | 33.0 |
| SN74ALVC164245DGGR | TSSOP | DGG | 48 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74ALVC164245DGGT | TSSOP | DGG | 48 | 250 | 346.0 | 346.0 | 41.0 |
| SN74ALVC164245DLR | SSOP | DL | 48 | 1000 | 346.0 | 346.0 | 49.0 |
| SN74ALVC164245KR | BGA MICROSTAR JUNIOR | GQL | 56 | 1000 | 346.0 | 346.0 | 33.0 |

ZQL (R-PBGA-N56)

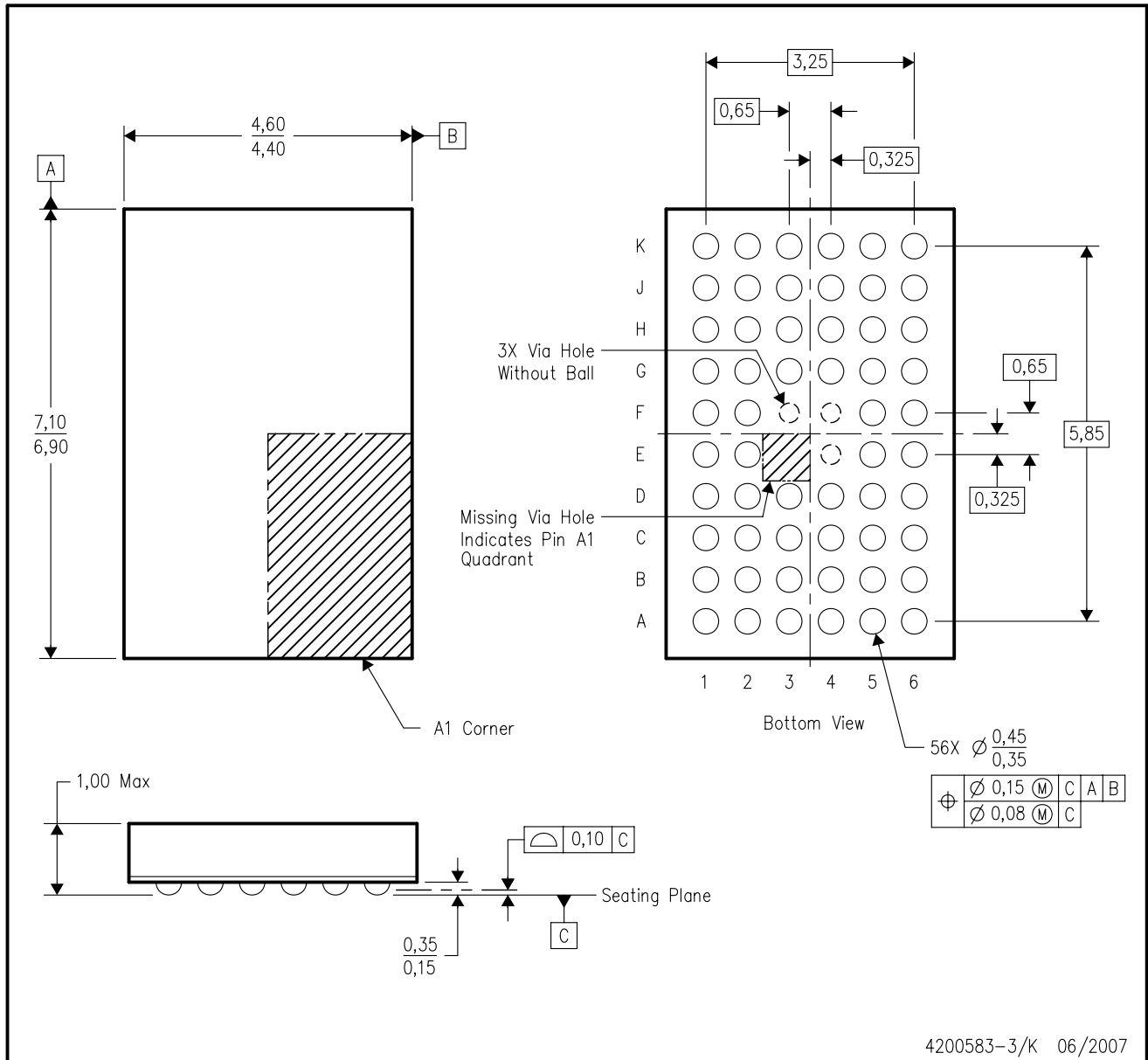
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BA-2.
 - D. This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY

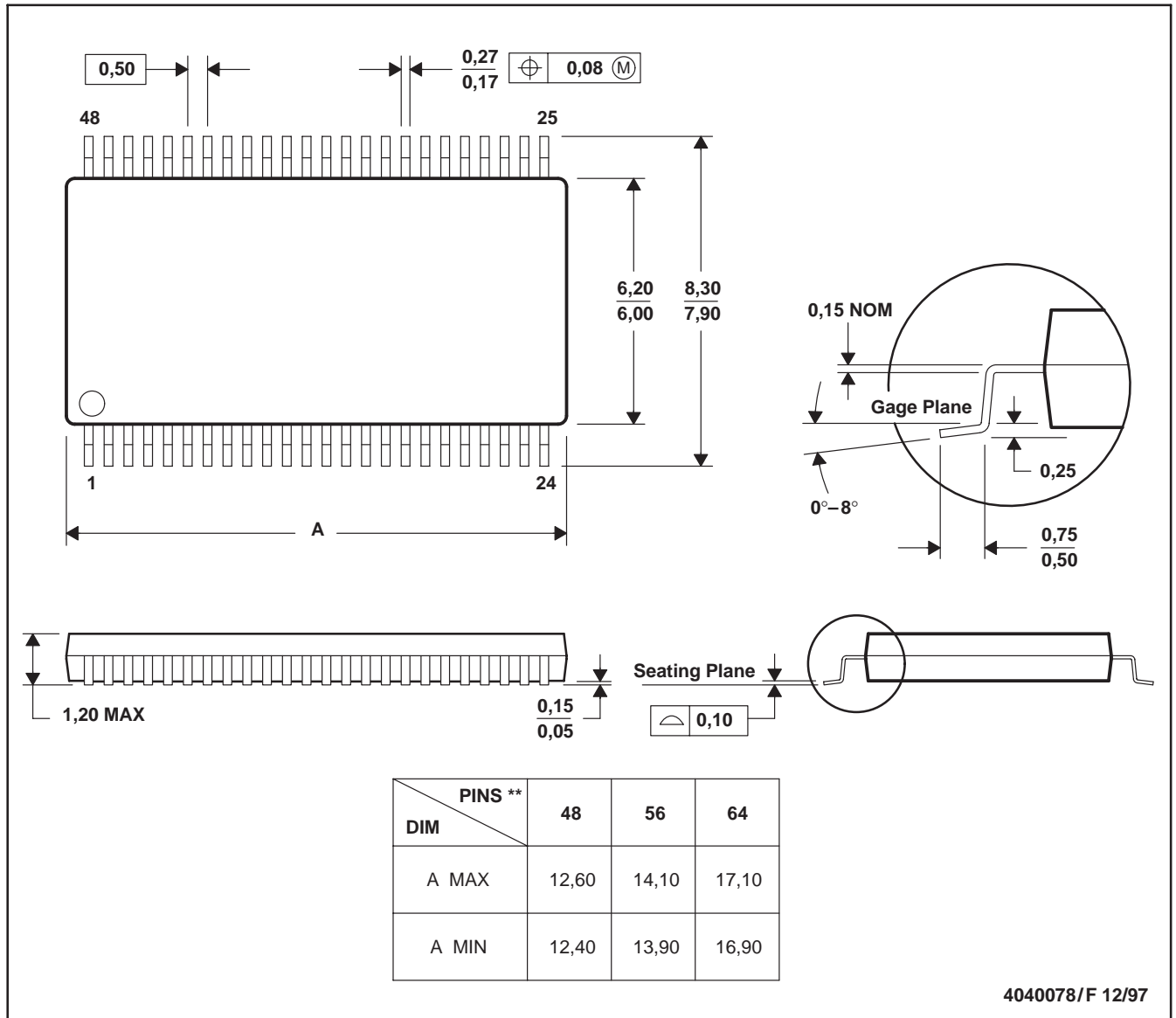


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BA-2.
 - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

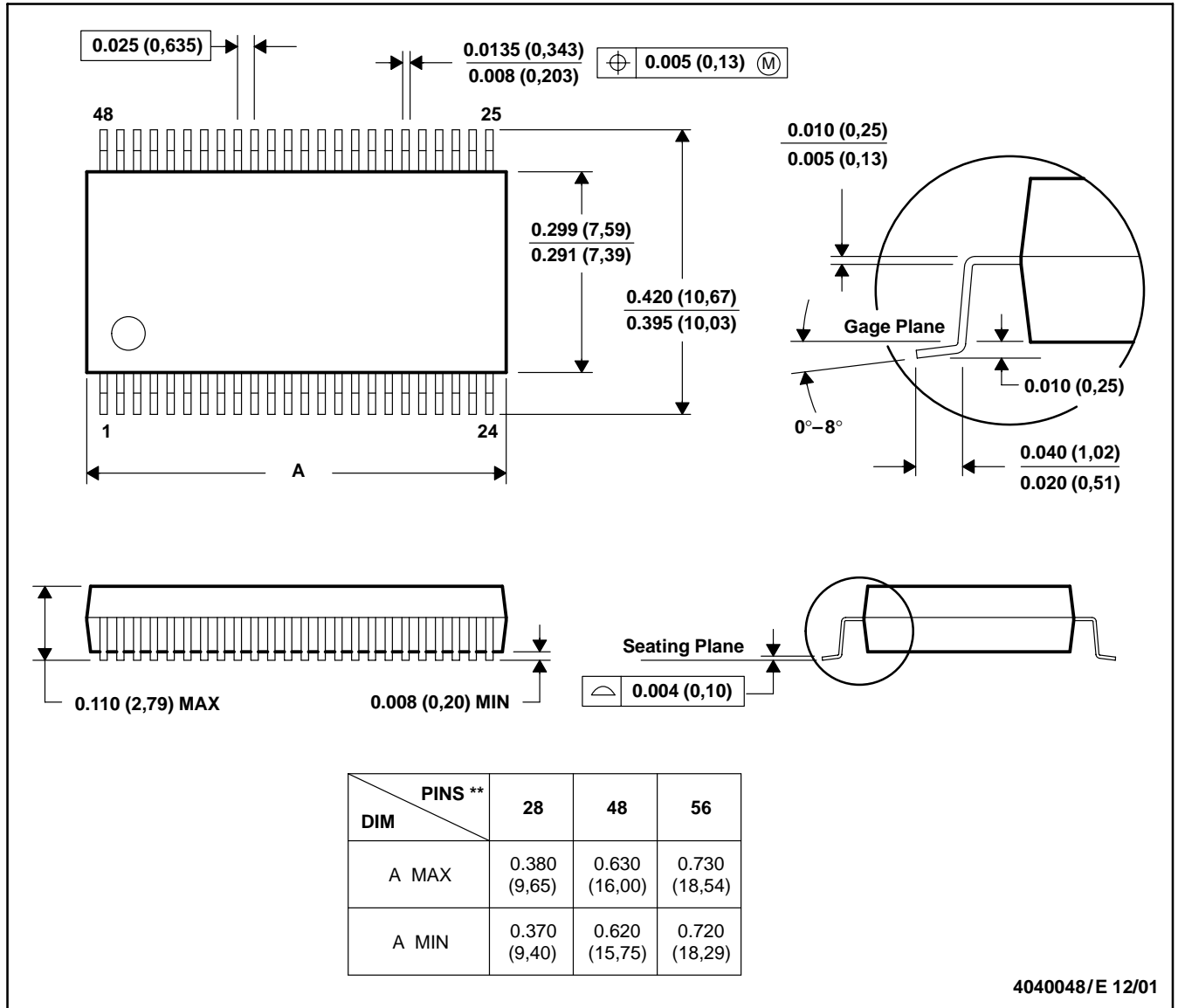


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

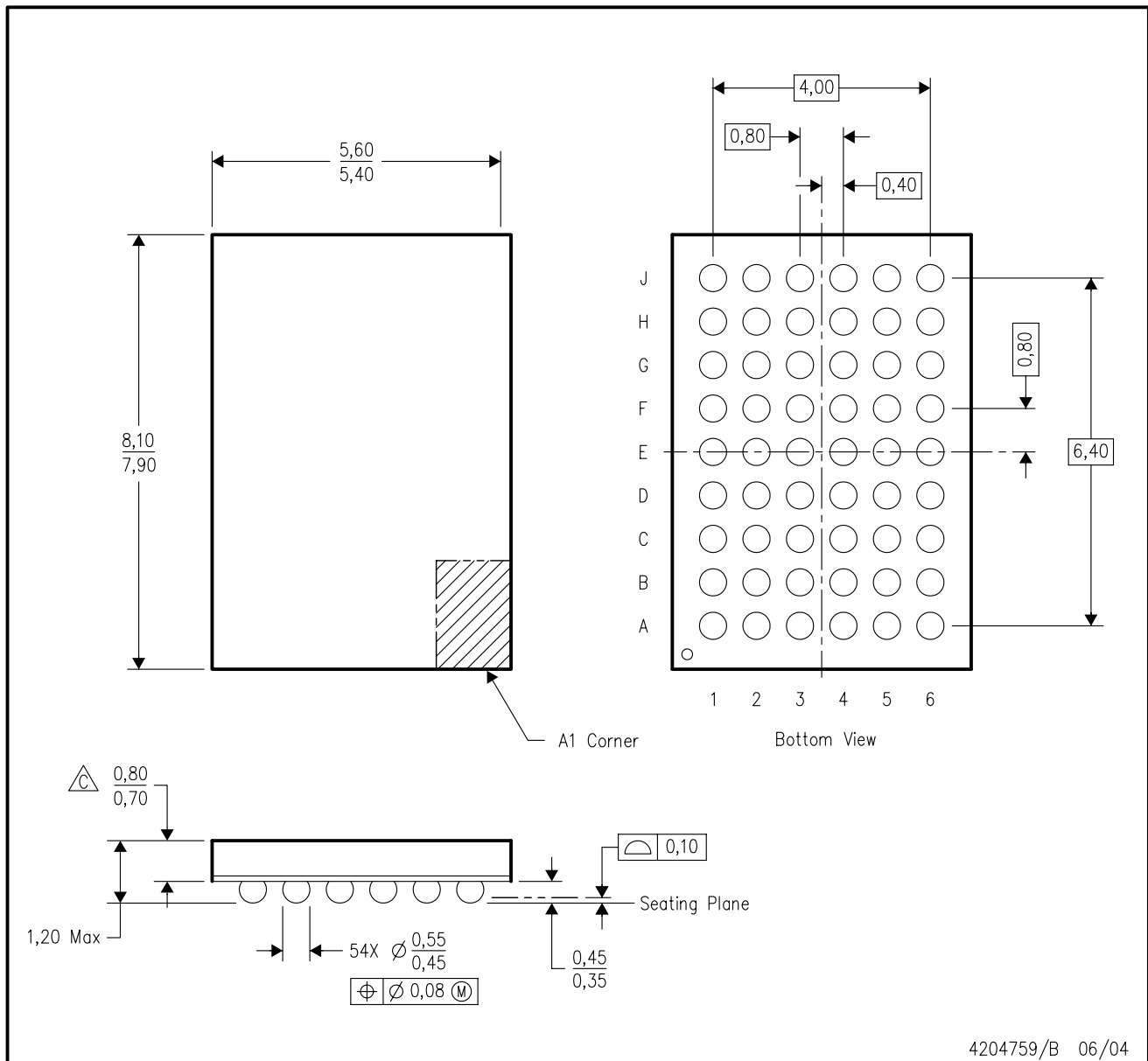
48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

GRD (R-PBGA-N54)

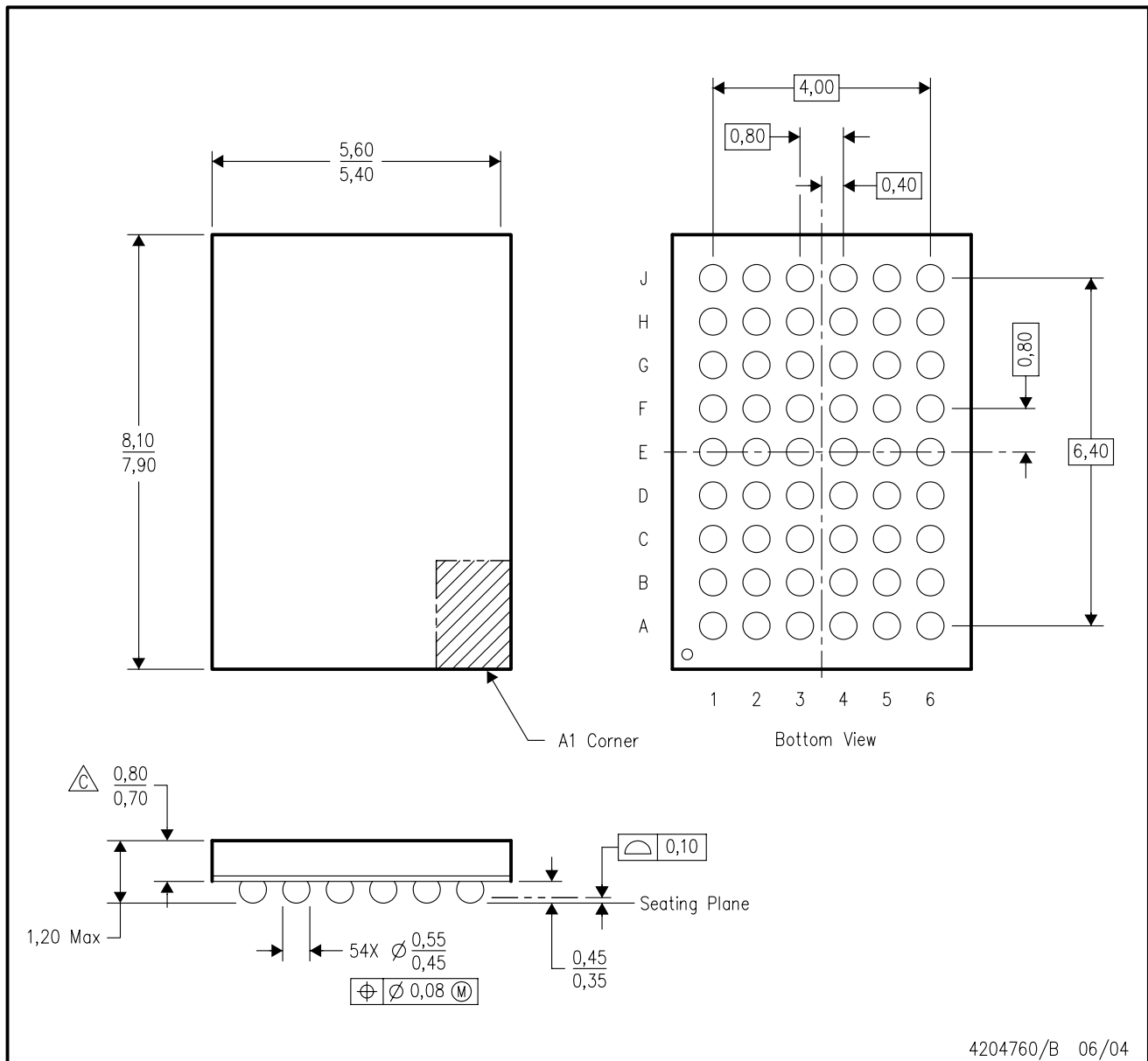
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MO-205 variation DD.
 - D. This package is tin-lead (SnPb). Refer to the 54 ZRD package (drawing 4204760) for lead-free.

ZRD (R-PBGA-N54)

PLASTIC BALL GRID ARRAY



4204760/B 06/04

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - \triangle Falls within JEDEC MO-205 variation DD.
 - D. This package is lead-free. Refer to the 54 GRD package (drawing 4204759) for tin-lead (SnPb).

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