

DATA SHEET



TDA8752

Triple high speed Analog-to-Digital Converter (ADC)

Product specification
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Triple high speed Analog-to-Digital Converter (ADC)

TDA8752

FEATURES

- Triple 8-bit ADC
- Sampling rate up to 100 MHz
- IC controllable via a serial interface, which can be either I²C-bus or 3-wire, selected via a TTL input pin
- IC analog voltage input from 0.4 to 1.2 V (p-p) to produce full-scale ADC input of 1 V (p-p)
- 3 clamps for programming a clamping code between -63.5 and +64 in steps of 1/2LSB
- 3 controllable amplifiers: gain controlled via the serial interface to produce a full scale resolution of 1/2LSB peak-to-peak
- Amplifier bandwidth of 250 MHz
- Low gain variation with temperature
- PLL, controllable via the serial interface to generate the ADC clock, which can be locked to a line frequency from 15 to 280 kHz
- Integrated PLL divider
- Programmable phase clock adjustment cells
- Internal voltage regulators
- TTL compatible digital inputs and outputs
- Chip enable high-impedance ADC output
- Power-down mode
- Possibility to use up to four ICs in the same system, using the I²C-bus interface, or more, using the 3-wire serial interface
- 1 W power dissipation.

APPLICATIONS

- R, G and B high speed digitizing
- LCD panels drive
- LCD projection systems
- VGA and higher resolutions
- Using two ICs in parallel, higher display resolution can be obtained; 200 MHz pixel frequency.

ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | | SAMPLING FREQUENCY (MHz) |
|-------------|---------|-----------------------------------------------------------------------------------|----------|--------------------------|
| | NAME | DESCRIPTION | VERSION | |
| TDA8752H/6 | QFP100 | plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm | SOT317-2 | 60 |
| TDA8752H/8 | | | | 100 |



GENERAL DESCRIPTION

The TDA8752 is a triple 8-bit ADC with controllable amplifiers and clamps for the digitizing of large bandwidth RGB signals.

The clamp level, the gain and all of the other settings are controlled via a serial interface (either I²C-bus or 3-wire serial bus, selected via a logic input).

The IC also includes a PLL that can be locked on the horizontal line frequency and generates the ADC clock. The PLL jitter is minimized for high resolution PC graphics applications. An external clock can also be input to the ADC.

It is possible to set the TDA8752 serial bus address between four fixed values, in the event that several TDA8752 ICs are used in a system, using the I²C-bus interface (for example, two ICs used in an odd/even configuration).

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QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------------|-------------------------------------------------------|-----------------------------------------------------------------------------------------|------|------|------|--------|
| V _{CCA} | analog supply voltage | for R, G and B channels | 4.75 | 5.0 | 5.25 | V |
| V _{DDD} | logic supply voltage | for I ² C-bus and 3-wire | 4.75 | 5.0 | 5.25 | V |
| V _{CCD} | digital supply voltage | | 4.75 | 5.0 | 5.25 | V |
| V _{CCO} | output stages supply voltage | for R, G and B channels | 4.75 | 5.0 | 5.25 | V |
| V _{CCA(PLL)} | analog PLL supply voltage | | 4.75 | 5.0 | 5.25 | V |
| V _{CCO(PLL)} | output PLL supply voltage | | 4.75 | 5.0 | 5.25 | V |
| I _{CCA} | analog supply current | | – | 120 | – | mA |
| I _{DDD} | logic supply current | for I ² C-bus and 3-wire | – | 1.0 | – | mA |
| I _{CCD} | digital supply current | | – | 40 | – | mA |
| I _{CCO} | output stages supply current | f _{CLK} = 100 MHz; ramp input | – | 6 | – | mA |
| I _{CCA(PLL)} | analog PLL supply current | | – | 28 | – | mA |
| I _{CCO(PLL)} | output PLL supply current | | – | 5 | – | mA |
| f _{CLK} | maximum clock frequency | TDA8752/6 | 60 | – | – | MHz |
| | | TDA8752/8 | 100 | – | – | MHz |
| f _{ref(PLL)} | PLL reference clock frequency | | 15 | – | 280 | kHz |
| f _{VCO} | VCO output clock frequency | | 12 | – | 100 | MHz |
| INL | DC integral non linearity | from analog input to digital output; full-scale; ramp input; f _{CLK} = 100 MHz | – | ±0.5 | ±1.5 | LSB |
| DNL | DC differential non linearity | from analog input to digital output; full-scale; ramp input; f _{CLK} = 100 MHz | – | ±0.5 | ±1.0 | LSB |
| ΔG _{amp} /T | amplifier gain stability as a function of temperature | V _{ref} = 2.5 V with 100 ppm/°C maximum | – | – | 200 | ppm/°C |
| B | amplifier bandwidth | –3 dB; T _{amb} = 25 °C | 250 | – | – | MHz |
| t _{set} | settling time of the ADC block plus AGC | input signal settling time < 1 ns; T _{amb} = 25 °C | – | – | 6 | ns |
| DR _{PLL} | PLL divider ratio | | 100 | – | 4095 | |
| P _{tot} | total power consumption | f _{CLK} = 100 MHz; ramp input | – | 1.0 | – | W |
| j _{PLL(rms)} | maximum PLL phase jitter (RMS value) | f _{ref} = 66.67 kHz; f _{CLK} = 100 MHz | – | 0.3 | – | ns |

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BLOCK DIAGRAM

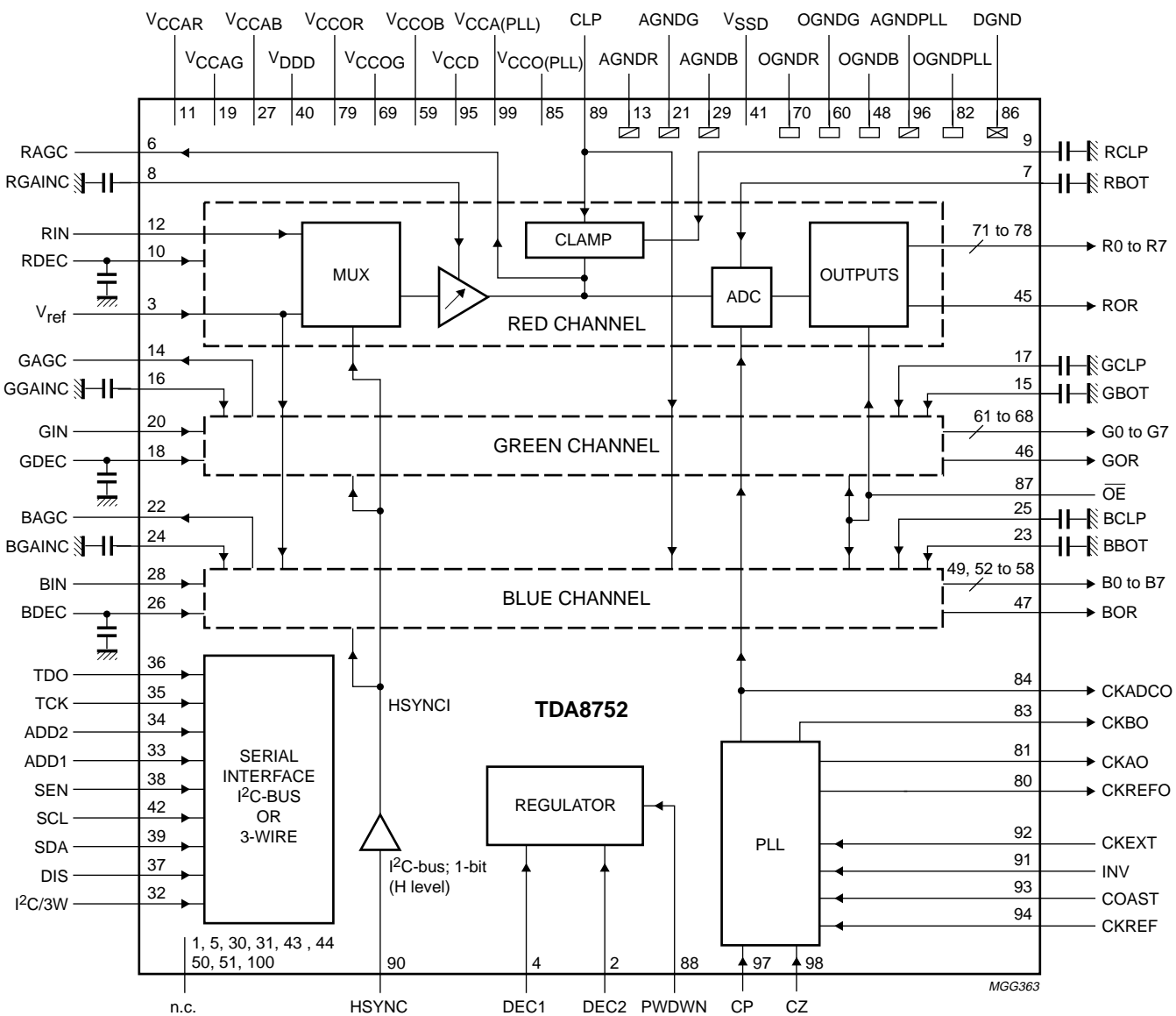


Fig.1 Block diagram.

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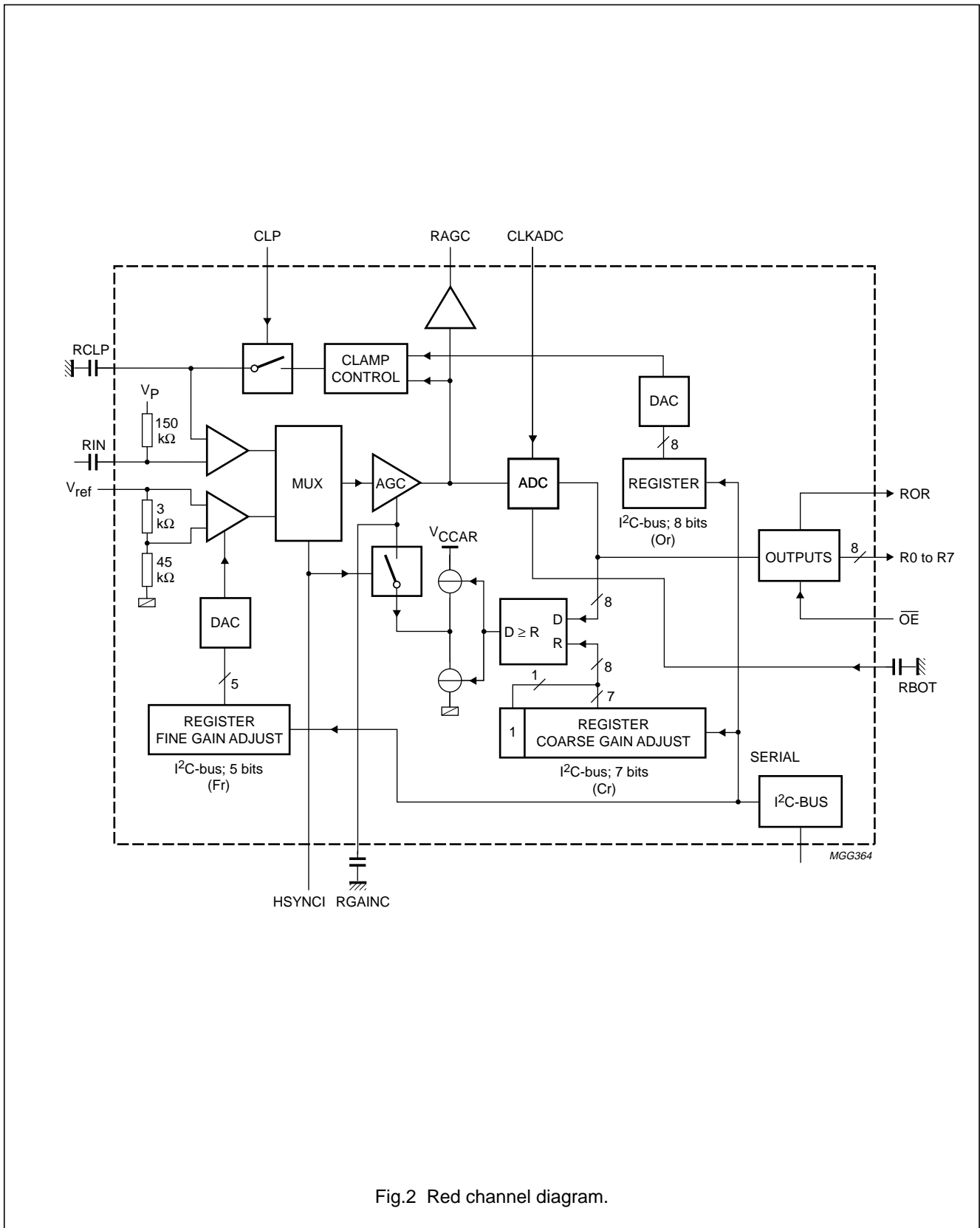


Fig.2 Red channel diagram.

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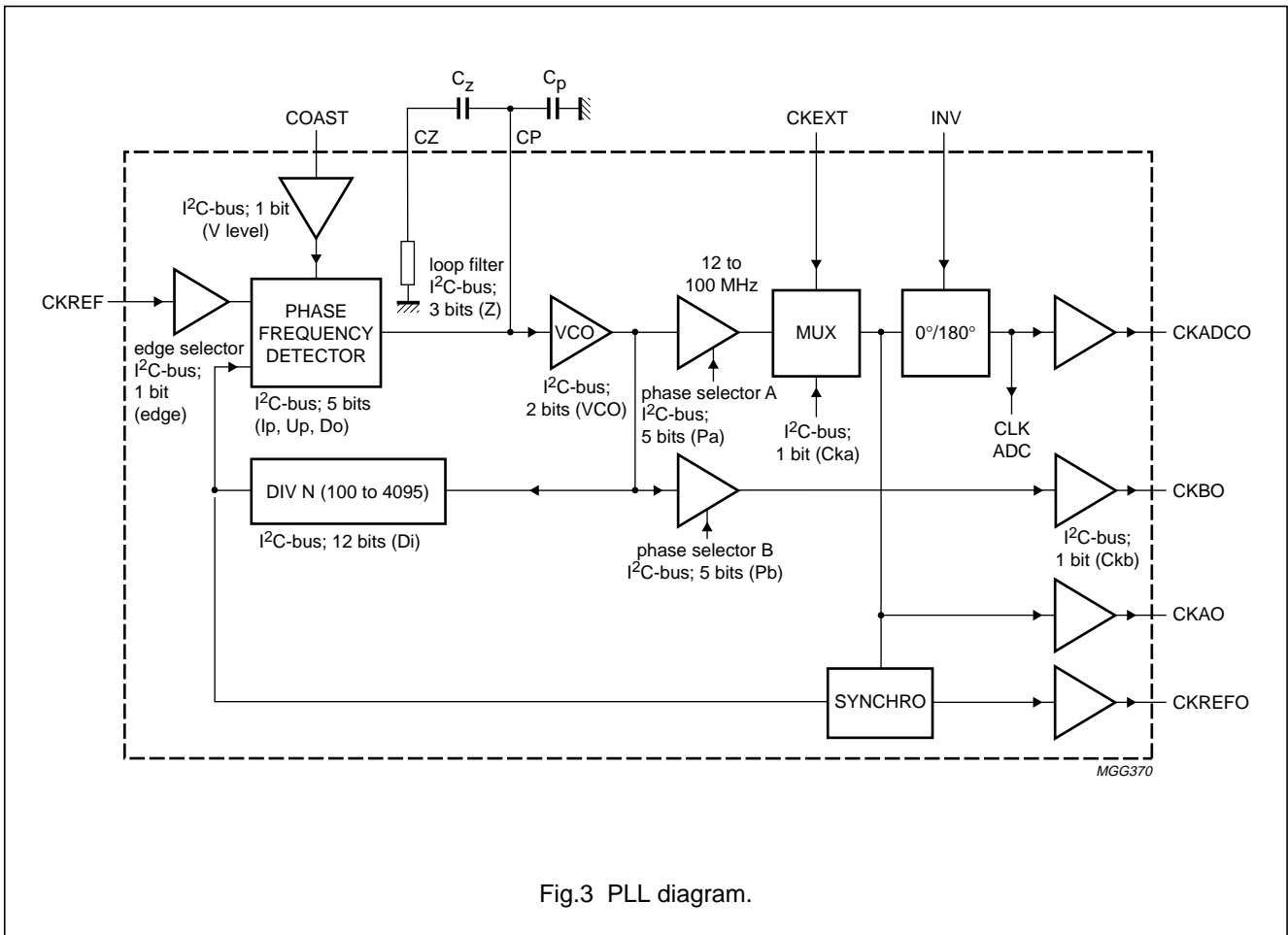


Fig.3 PLL diagram.

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PINNING

| SYMBOL | PIN | DESCRIPTION |
|---------------------|-----|-----------------------------------------------------------------------------------------------|
| n.c. | 1 | not connected |
| DEC2 | 2 | main regulator decoupling input |
| V _{ref} | 3 | gain stabilizer voltage reference input |
| DEC1 | 4 | main regulator decoupling input |
| n.c. | 5 | not connected |
| RAGC | 6 | red channel AGC output |
| RBOT | 7 | red channel ladder decoupling input (BOT) |
| RGAINC | 8 | red channel gain capacitor input |
| RCLP | 9 | red channel gain clamp capacitor input |
| RDEC | 10 | red channel gain regulator decoupling input |
| V _{CCAR} | 11 | red channel gain analog power supply |
| RIN | 12 | red channel gain analog input |
| AGNDR | 13 | red channel gain analog ground |
| GAGC | 14 | green channel AGC output |
| GBOT | 15 | green channel ladder decoupling input (BOT) |
| GGAINC | 16 | green channel gain capacitor input |
| GCLP | 17 | green channel gain clamp capacitor input |
| GDEC | 18 | green channel gain regulator decoupling input |
| V _{CCAG} | 19 | green channel gain analog power supply |
| GIN | 20 | green channel gain analog input |
| AGNDG | 21 | green channel gain analog ground |
| BAGC | 22 | blue channel AGC output |
| BBOT | 23 | blue channel ladder decoupling input (BOT) |
| BGAINC | 24 | blue channel gain capacitor input |
| BCLP | 25 | blue channel gain clamp capacitor input |
| BDEC | 26 | blue channel gain regulator decoupling input |
| V _{CCAB} | 27 | blue channel gain analog power supply |
| BIN | 28 | blue channel gain analog input |
| AGNDB | 29 | blue channel gain analog ground |
| n.c. | 30 | not connected |
| n.c. | 31 | not connected |
| I ² C/3W | 32 | selection input between I ² C-bus (active HIGH) and 3-wire serial bus (active LOW) |
| ADD1 | 33 | I ² C-bus address control input 1 |
| ADD2 | 34 | I ² C-bus address control input 2 |
| TCK | 35 | scan test mode (active HIGH) |

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| SYMBOL | PIN | DESCRIPTION |
|-------------------|-----|-----------------------------------------------------------------------|
| TDO | 36 | scan test output |
| DIS | 37 | I ² C and 3W disable control input (disable at HIGH level) |
| SEN | 38 | select enable for 3-wire serial bus input (see Fig.10) |
| SDA | 39 | I ² C/3W serial data input |
| V _{DDD} | 40 | logic I ² C/3W digital power supply |
| V _{SSD} | 41 | logic I ² C/3W digital ground |
| SCL | 42 | I ² C/3W serial clock input |
| n.c. | 43 | not connected |
| n.c. | 44 | not connected |
| ROR | 45 | red channel ADC output bit out of range |
| GOR | 46 | green channel ADC output bit out of range |
| BOR | 47 | blue channel ADC output bit out of range |
| OGNDB | 48 | blue channel ADC output ground |
| B0 | 49 | blue channel ADC output bit 0 (LSB) |
| n.c. | 50 | not connected |
| n.c. | 51 | not connected |
| B1 | 52 | blue channel ADC output bit 1 |
| B2 | 53 | blue channel ADC output bit 2 |
| B3 | 54 | blue channel ADC output bit 3 |
| B4 | 55 | blue channel ADC output bit 4 |
| B5 | 56 | blue channel ADC output bit 5 |
| B6 | 57 | blue channel ADC output bit 6 |
| B7 | 58 | blue channel ADC output bit 7 (MSB) |
| V _{CCOB} | 59 | blue channel ADC output power supply |
| OGNDG | 60 | green channel ADC output ground |
| G0 | 61 | green channel ADC output bit 0 (LSB) |
| G1 | 62 | green channel ADC output bit 1 |
| G2 | 63 | green channel ADC output bit 2 |
| G3 | 64 | green channel ADC output bit 3 |
| G4 | 65 | green channel ADC output bit 4 |
| G5 | 66 | green channel ADC output bit 5 |
| G6 | 67 | green channel ADC output bit 6 |
| G7 | 68 | green channel ADC output bit 7 (MSB) |
| V _{CCOG} | 69 | green channel ADC output power supply |
| OGNDR | 70 | red channel ADC output ground |
| R0 | 71 | red channel ADC output bit 0 (LSB) |

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| SYMBOL | PIN | DESCRIPTION |
|-----------------------|-----|-------------------------------------------------------------------------------------|
| R1 | 72 | red channel ADC output bit 1 |
| R2 | 73 | red channel ADC output bit 2 |
| R3 | 74 | red channel ADC output bit 3 |
| R4 | 75 | red channel ADC output bit 4 |
| R5 | 76 | red channel ADC output bit 5 |
| R6 | 77 | red channel ADC output bit 6 |
| R7 | 78 | red channel ADC output bit 7 (MSB) |
| V _{CCOR} | 79 | red channel ADC output power supply |
| CKREFO | 80 | reference output clock resynchronized horizontal pulse |
| CKAO | 81 | PLL clock output 3 (in phase with reference output clock) |
| OGNDPLL | 82 | PLL digital ground |
| CKBO | 83 | PLL clock output 2 |
| CKADCO | 84 | PLL clock output 1 (in phase with internal ADC clock) |
| V _{CCO(PLL)} | 85 | PLL output power supply |
| DGND | 86 | digital ground |
| \overline{OE} | 87 | output enable not (when \overline{OE} is HIGH, the outputs are in high-impedance) |
| PWDWN | 88 | power-down control input (IC is in power-down mode when this pin is HIGH) |
| CLP | 89 | clamp pulse input (clamp active HIGH) |
| HSYNC | 90 | horizontal synchronization input pulse |
| INV | 91 | PLL clock output inverter command input (invert when HIGH) |
| CKEXT | 92 | external clock input |
| COAST | 93 | PLL coast command input |
| CKREF | 94 | PLL reference clock input |
| V _{CCD} | 95 | digital power supply |
| AGNDPLL | 96 | PLL analog ground |
| CP | 97 | PLL filter input |
| CZ | 98 | PLL filter input |
| V _{CCAPLL} | 99 | PLL analog power supply |
| n.c. | 100 | not connected |

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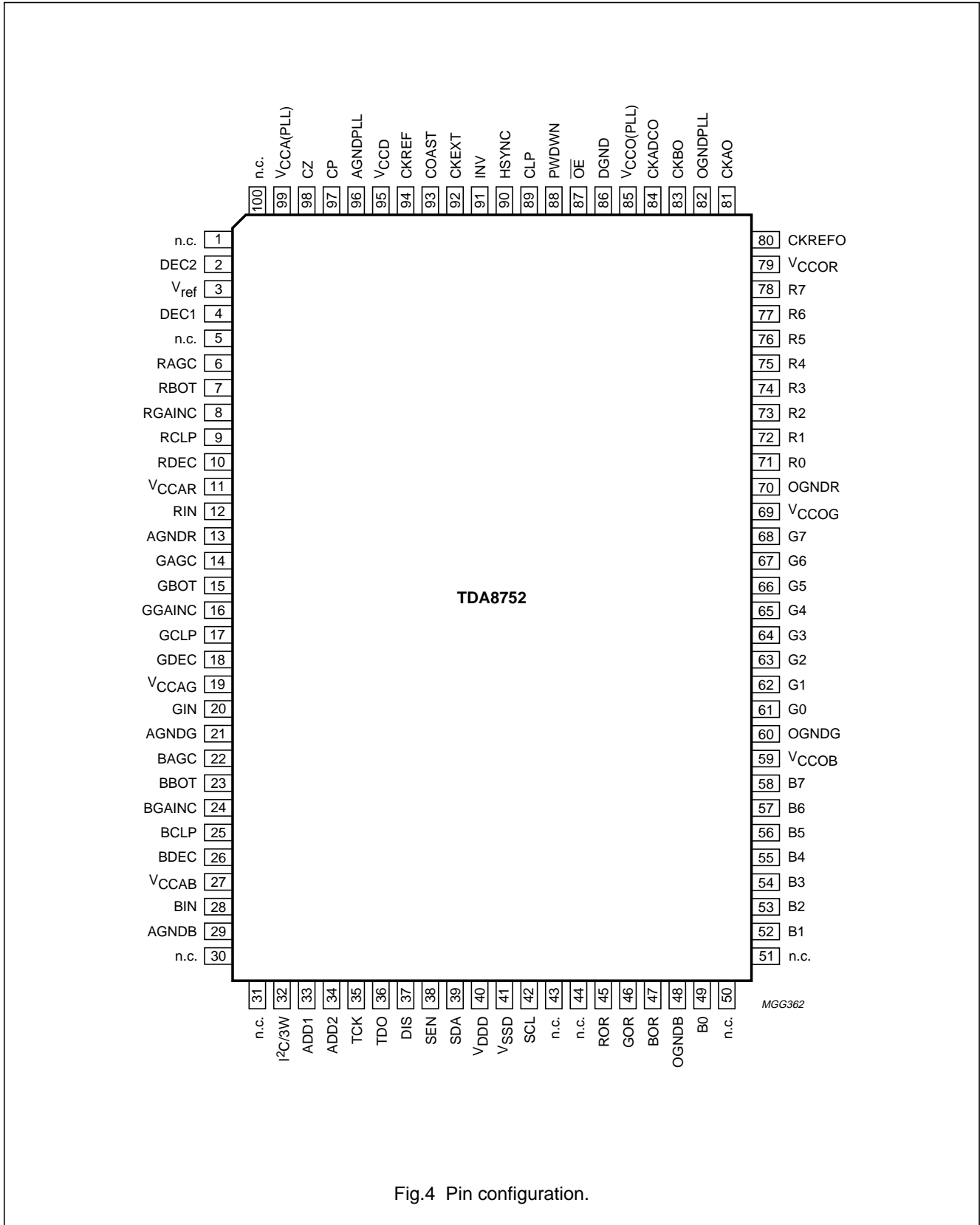


Fig.4 Pin configuration.

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FUNCTIONAL DESCRIPTION

This triple high-speed 8-bit ADC is designed to convert RGB signals, from a PC or work station, into data used by a LCD driver (pixel clock up to 200 MHz, using 2 ICs).

IC analog video inputs

The video inputs are internally DC polarized. These inputs are AC coupled externally.

Clamps

Three independent parallel clamping circuits are used to clamp the video input signals on the black level and to control the brightness level. The clamping code is programmable between code -63.5 and $+64$ in steps of $\frac{1}{2}$ LSB. The programming of the clamp value is achieved via an 8-bit DAC. Each clamp must be able to correct an offset from ± 0.1 V to ± 10 mV within 300 ns, and correct the total offset in 10 lines.

The clamps are controlled by an external TTL positive going pulse (pin CLP). The drop of the video signal is < 1 LSB.

Normally, the circuit operates with a 0 code clamp, corresponding to the 0 ADC code. This clamp code can be changed from -63.5 to $+64$ as represented in Fig.7, in steps of $\frac{1}{2}$ LSB. The digitized video signal is always between code 0 and code 255 of the ADC.

Variable gain amplifier

Three independent variable gain amplifiers are used to provide, to each channel, a full-scale input range signal to the 8-bit ADC. The gain adjustment range is designed so that, for an input range varying from 0.4 to 1.2 V (p-p), the output signal corresponds to the ADC full-scale input of 1 V (p-p).

To ensure that the gain does not vary over the whole operating temperature range, an external reference of $+2.5$ V DC, (V_{ref} with a 100 ppm/ $^{\circ}$ C maximum variation) supplied externally, is used to calibrate the gain at the beginning of each video line before the clamp pulse using the following principle.

A differential of 0.156 V (p-p) ($\frac{1}{16}V_{ref}$) reference signal is generated internally from the reference voltage (V_{ref}). During the synchronization part of the video line, the multiplexer, controlled by the TTL synchronization signal (HSYNCI, coming from HSYNC; see Fig.1) with a width equal to one of the video synchronization signals (e.g. signal coming from a synchronization separator), is switched between the two amplifiers.

The output of the multiplexer is either the normal video signal or the 0.156 V reference signal (during HSYNC).

The corresponding ADC outputs are then compared to a pre-set value loaded in a register. Depending on the result of the comparison, the gain of the variable gain amplifiers is adjusted (coarse gain control; see Figs 2 and 8). The three 7-bit registers receive data via a serial interface to enable the gain to be programmed.

The pre-set value loaded in the 7-bit register is chosen between approximately 67 codes to ensure the full-scale input range (see Fig.8). A contrast control can be achieved using these registers. In this case care should be taken to stay within the allowed code range (32 to 99).

A fine correction using three 5-bit DACs, also controlled via the serial interface, is used to finely tune the gain of the three channels (fine gain control; see Figs 2 and 9) and to compensate the channel-to-channel gain mismatch.

With a full scale ADC input, the resolution of the fine register corresponds to $\frac{1}{2}$ LSB peak-to-peak variation.

To use these gain controls correctly, it is recommended to fix the coarse gain (to have a full-scale ADC input signal) to within 4LSB and then adjust it with the fine gain. The gain is adjusted during HSYNC. During this time the output signal is not related to the amplified input signal. The outputs, when the coarse gain system is stable, is related to the programmed coarse code (see Fig.8).

ADCs

The ADCs are 8-bit with a maximum clock frequency of 100 Msp/s. The ADCs input range is 1 V (p-p) full-scale. One out of range bit exists per channel (ROR, GOR and BOR). It will be at logic 1 when the signal is out of range of the full scale of the ADCs.

Pipeline delay in the ADCs is 1 clock cycle from sampling to data output.

The ADCs reference ladders regulators are integrated.

ADC outputs

ADC outputs are straight binary. An output enable pin (\overline{OE} ; active LOW) enables the output status between active and high-impedance ($\overline{OE} = \text{HIGH}$) to be switched; it is recommended to load the outputs with a 10 pF capacitive load. The timing must be checked very carefully if the capacitive load is more than 10 pF.

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Phase-locked loop

The ADCs are clocked either by an internal PLL locked to the CKREF clock, (all of the PLL is on-chip except the loop filter capacitance) or an external clock, CKEXT. Selection is performed via the serial interface bus.

The reference clock (CKREF) range is between 15 and 280 kHz. Consequently, the VCO minimum frequency is 12 MHz and the maximum frequency 100 MHz for the TDA8752/8 and 60 MHz for the TDA8752/6. The gain of the VCO part can be controlled via the serial interface, depending on the frequency range to which the PLL is locked.

To increase the bandwidth of the PLL, the charge pump current, controlled by the serial interface, must also be increased. The relationship between the frequency and the current is given by the following equation:

$$f_n = \frac{1}{2\pi} \sqrt{\frac{K_O I_P}{(C_z + C_P) N}}$$

Where:

- f_n = the natural PLL frequency
- K_O = the VCO gain
- N = the division number
- C_z and C_P = capacitors of the PLL filter.

The other PLL equation is as follows:

$$f_z = \frac{1}{2\pi \times R \times C_z} \text{ and } \left(\xi = \frac{1}{2} \times \frac{f_n}{f_z} \right)$$

Where:

- f_z = loop filter zero frequency
- R = the chosen resistance for the filter
- ξ = the damping factor.

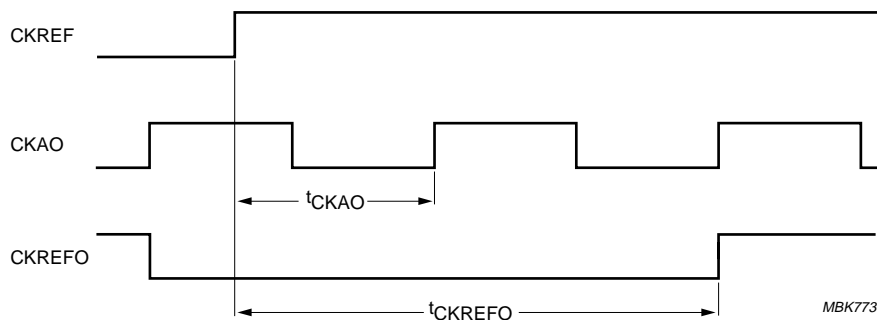
Different resistances for the filter can be programmed via the serial interface. To have better performances, the PLL parameters should be chosen so that:

$$f_n / f_{ref} \cong 0.05$$

$$\xi \cong 1.5.$$

It is possible to control (independently) the phase of the ADC clock and the phase of an additional clock output (which could be used to drive a second TDA8752). For this, two serial interface-controlled digital phase-shift controllers are included (controlled by 5-bit registers, phase shift controller steps are 11.25° each on the whole PLL frequency range).

CKREF is resynchronized, by the synchro block, on the CKAO clock. The output is CKREFO (LOW during 8 clock periods). CKAO is the clock at the output of the phase selector A. This clock can be used as the clocks for CKBO and CKADCO. The timing is given in Fig.5.



$$t_{CKAO} = t_{CLK(buffer)} + t_{phase selector} \quad (t_{CLK(buffer)} = 10 \text{ ns and } t_{phase selector} = \frac{t_{phase selector}}{2\pi} \times T_{CLK(pixel)}).$$

$$t_{CKREFO} = \text{either } t_{CKAO} \text{ if phase A } \geq 01000 \text{ or } t_{CKAO} + T_{CLK(pixel)} \text{ if phase A } < 01000.$$

Fig.5 Timing.

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The COAST pin is used to disconnect the PLL phase frequency detector during the frame flyback or the unavailability of the CKREF signal. This signal can normally be derived from the VSYNC signal.

The clock output is able to drive an external 10 pF load (for the on-chip ADCs).

The PLL can be used in three different methods:

1. The IC can be used as stand-alone with a sampling frequency of up to 100 MHz for the TDA8752/8 and up to 60 MHz for the TDA8752/6.
2. When an RGB signal is at a pixel frequency exceeding 100 to 200 MHz, it is possible to follow one of the two possibilities given below;
 - a) Using one TDA8752; the sampling rate can be reduced by a factor of two, by sampling the even pixels in the even frame and the odd pixels in the odd frame. The INV pin is used to toggle between frames.

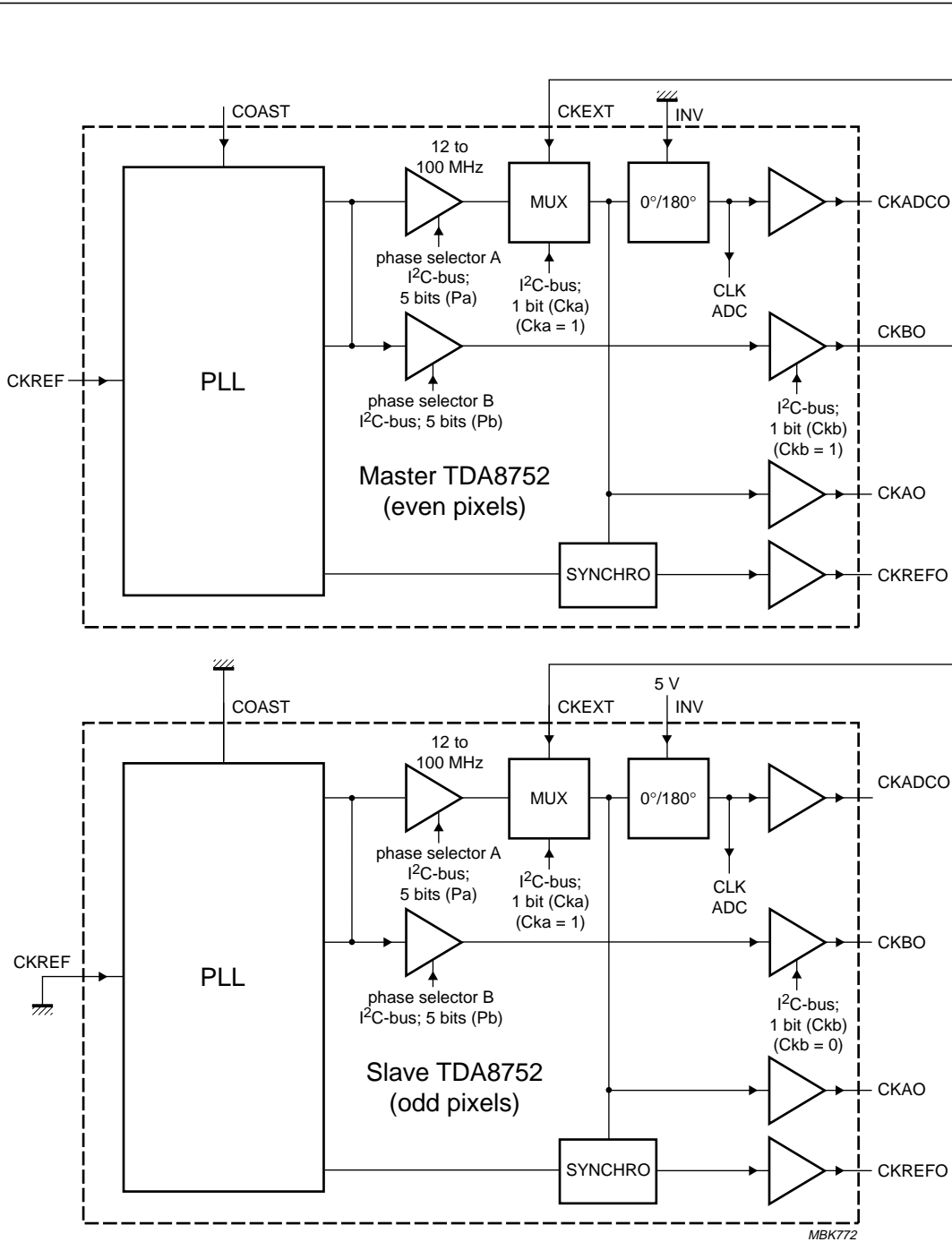
- b) Using two TDA8752s the PLL of the master TDA8752 is used to drive both ADC clocks. The PLL of the slave TDA8752 is disconnected and the CKBO of the master TDA8752 is connected to pin CKEXT of both TDA8752.

The master TDA8752 is used to sample the even pixels and the slave TDA8752 for odd pixels, using a 180° phase shift between the clocks (CKADCO pins). The master chip has its INV pin LOW while the slave chip has its INV pin HIGH, which guarantees the 180° shift ADC clock drive. It is then necessary to adjust phase B of the master chip. Special care should be taken with the quality of the input signal (input setting time).

If CKREFO output signal at the master chip is needed, it is possible to use one of the two phase A values in order to avoid set-up and hold problems in the SYNCHRO function; e.g. PHASEA = 100000 and PHASEA = 111111.

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Slave at 180° phase shift with respect to pin CKADCO of the master TDA8752.

Fig.6 Dual TDA8752 solution for pixel clock rate with a single phase adjustment (100 to 200 MHz).

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I²C-bus and 3-wire serial bus interface

The I²C-bus and 3-wire serial buses control the status of the different control DACs and registers. Control pin DIS enables or disables the full serial interface function (disable at HIGH level). Four ICs can be used in the same system and programmed by the same bus. Therefore, two pins (ADD1 and ADD2) are available to set each address respectively, for use with the I²C-bus interface. All programming is described in Chapter "I²C-bus and 3-wire interfaces".

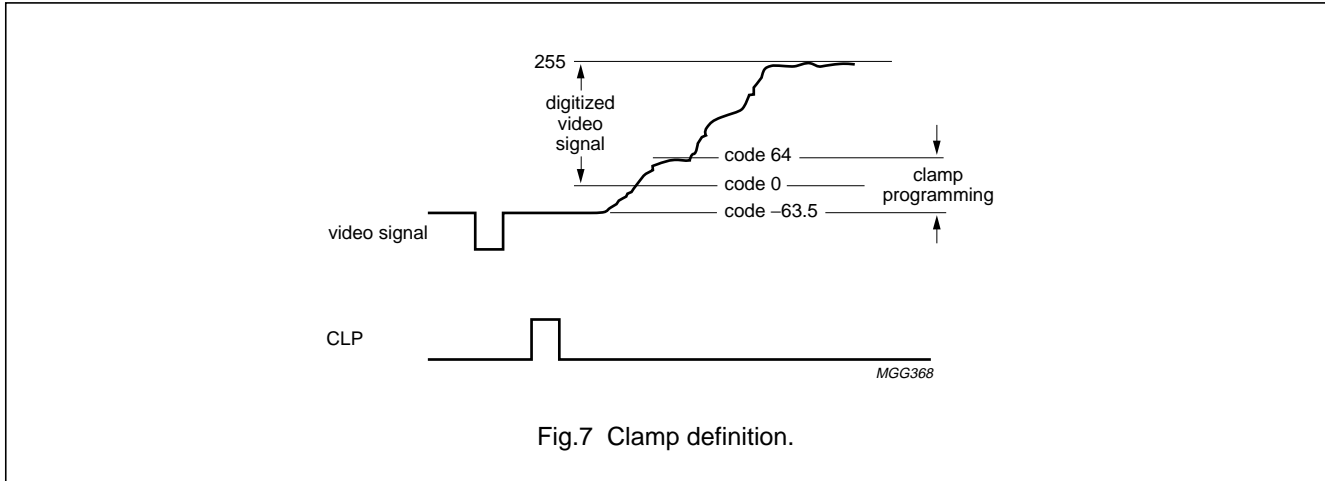


Fig.7 Clamp definition.

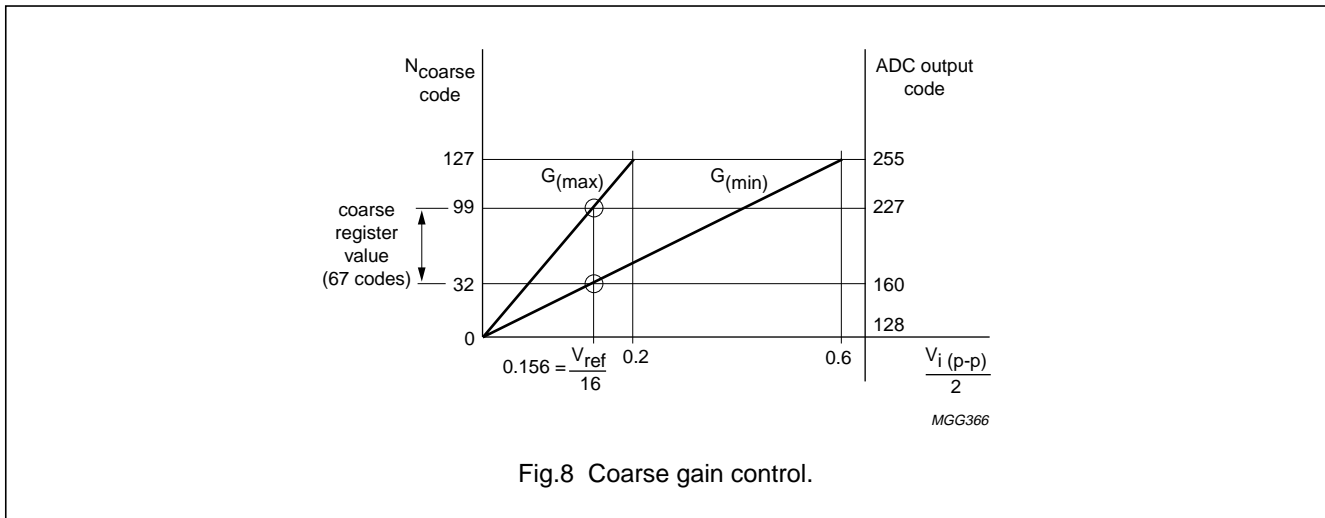


Fig.8 Coarse gain control.

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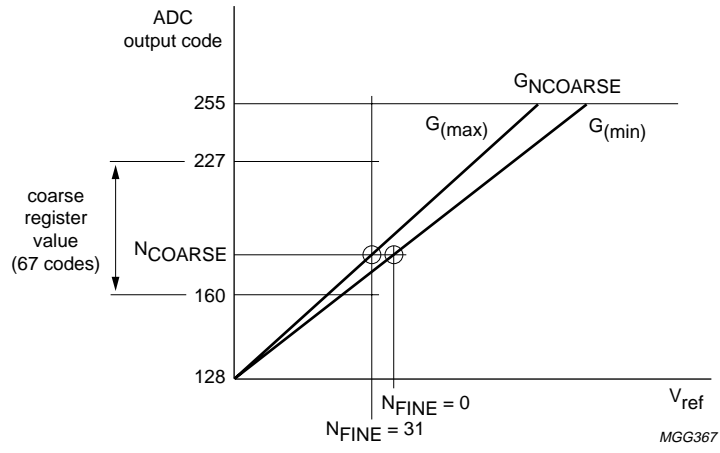


Fig.9 Fine gain correction for a coarse gain $G_{NCOARSE}$.

I²C-BUS AND 3-WIRE INTERFACES

Register definitions

The configuration of the different registers is as follows:

Table 1 I²C-bus and 3-wire registers

| FUNCTION NAME | SUB-ADDRESS | | | | | | | | BIT DEFINITION | | | | | | | | DEFAULT VALUE |
|---------------|-------------|----|----|----|----|----|----|----|----------------|---------|------|------|------|------|------|-----|---------------|
| | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | MSB | | | | | | | LSB | |
| SUBADDR | – | – | – | – | – | – | – | – | X | X | X | Mode | Sa3 | Sa2 | Sa1 | Sa0 | xxx1 0000 |
| OFFSETR | X | X | X | X | 0 | 0 | 0 | 0 | Or7 | Or6 | Or5 | Or4 | Or3 | Or2 | Or1 | Or0 | 0111 1111 |
| COARSER | X | X | X | X | 0 | 0 | 0 | 1 | X | Cr6 | Cr5 | Cr4 | Cr3 | Cr2 | Cr1 | Cr0 | x010 0000 |
| FINER | X | X | X | X | 0 | 0 | 1 | 0 | X | X | X | Fr4 | Fr3 | Fr2 | Fr1 | Fr0 | xxx0 0000 |
| OFFSETG | X | X | X | X | 0 | 0 | 1 | 1 | Og7 | Og6 | Og5 | Og4 | Og3 | Og2 | Og1 | Og0 | 0111 1111 |
| COARSEG | X | X | X | X | 0 | 1 | 0 | 0 | X | Cg6 | Cg5 | Cg4 | Cg3 | Cg2 | Cg1 | Cg0 | x010 0000 |
| FINEG | X | X | X | X | 0 | 1 | 0 | 1 | X | X | X | Fg4 | Fg3 | Fg2 | Fg1 | Fg0 | xxx0 0000 |
| OFFSETB | X | X | X | X | 0 | 1 | 1 | 0 | Ob7 | Ob6 | Ob5 | Ob4 | Ob3 | Ob2 | Ob1 | Ob0 | 0111 1111 |
| COARSEB | X | X | X | X | 0 | 1 | 1 | 1 | X | Cb6 | Cb5 | Cb4 | Cb3 | Cb2 | Cb1 | Cb0 | x010 0000 |
| FINEB | X | X | X | X | 1 | 0 | 0 | 0 | X | X | X | Fb4 | Fb3 | Fb2 | Fb1 | Fb0 | xxx0 0000 |
| CONTROL | X | X | X | X | 1 | 0 | 0 | 1 | V level | H level | edge | Up | Do | Ip2 | Ip1 | Ip0 | 0000 0100 |
| VCO | X | X | X | X | 1 | 0 | 1 | 0 | Z2 | Z1 | Z0 | Vco1 | Vco0 | Di11 | Di10 | Di9 | 0110 0001 |
| DIVIDER (LSB) | X | X | X | X | 1 | 0 | 1 | 1 | Di8 | Di7 | Di6 | Di5 | Di4 | Di3 | Di2 | Di1 | 1001 0000 |
| PHASEA | X | X | X | X | 1 | 1 | 0 | 0 | X | Di0 | Cka | Pa4 | Pa3 | Pa2 | Pa1 | Pa0 | x000 0000 |
| PHASEB | X | X | X | X | 1 | 1 | 0 | 1 | X | X | Ckb | Pb4 | Pb3 | Pb2 | Pb1 | Pb0 | xx00 0000 |

All the registers are defined by a sub-address of 8 bits; bit A4 refers to the mode which is used with the I²C-bus interface; bits Sa3 to Sa0 are the subaddresses of each register.

The bit mode, used only with the I²C-bus, enables two modes to be programmed:

- If Mode = 0, each register is programmed independently by giving its sub-address and its content
- If Mode = 1, all the registers are programmed one after the other by giving this initial condition (xxx1 1111) as the sub-address state; thus, the registers are charged following the predefined sequence of 16 bytes (from sub-address 0000 to 1101).

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OFFSET REGISTER

This register controls the clamp level for the RGB channels. The relationship between the programming code and the level of the clamp code is given in Table 2.

Table 2 Coding

| PROGRAMMED CODE | CLAMP CODE | ADC OUTPUT |
|-----------------|------------|------------|
| 0 | -63.5 | underflow |
| 1 | -63 | |
| 2 | -62.5 | |
| ↓ | ↓ | |
| 127 | 0 | 0 |
| ↓ | ↓ | ↓ |
| 254 | 63.5 | 63 or 64 |
| 255 | 64 | 64 |

The default programmed value is:

- Programmed code = 127
- Clamp code = 0
- ADC output = 0.

COARSE AND FINE REGISTERS

These two registers enable the gain control, the AGC gain with the coarse register and the reference voltage with the fine register. The coarse register programming equation is as follows:

$$GAIN = \frac{N_{COARSE} + 1}{V_{ref} \left(1 - \frac{N_{FINE}}{32 \times 16} \right)} \times \frac{1}{16} = \frac{N_{COARSE} + 1}{V_{ref} (512 - N_{FINE})} \times 32$$

Where: $V_{ref} = 2.5 \text{ V}$.

The gain correspondence is given in Table 3. The gain is linear with reference to the programming code ($N_{FINE} = 0$).

Table 3 Gain correspondence (COARSE)

| N _{COARSE} | GAIN | V _i TO BE FULL-SCALE |
|---------------------|-------|---------------------------------|
| 32 | 0.825 | 1.212 |
| 99 | 2.5 | 0.4 |

The default programmed value is as follows:

- $N_{COARSE} = 32$
- Gain = 0.825
- V_i to be full-scale = 1.212.

To modulate this gain, the fine register is programmed using the above equation. With a full-scale ADC input, the fine register resolution is a 1/2LSB peak-to-peak (see Table 4 for $N_{COARSE} = 32$).

Table 4 Gain correspondence (FINE)

| N _{FINE} | GAIN | V _i TO BE FULL-SCALE |
|-------------------|-------|---------------------------------|
| 0 | 0.825 | 1.212 |
| 31 | 0.878 | 1.139 |

The default programmed value is: $N_{FINE} = 0$.

CONTROL REGISTER

COAST and HSYNC signals can be inverted by setting the I²C-bus control bits V level and H level respectively. When V level and H level are set to zero respectively, COAST and HSYNC are active HIGH.

The bit 'edge' defines the rising or falling edge of CKREF to synchronise the PLL. It will be on the rising edge if the bit is at logic 0 and on the falling edge if the bit is at logic 1.

The bits Up and Do are used for the test, to force the charge pump current. These bits have to be logic 0 during normal use.

The bits Ip0, Ip1 and Ip2 control the charge pump current, to increase the bandwidth of the PLL, as shown in Table 5.

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Table 5 Charge-pump current control

| Ip2 | Ip1 | Ip0 | CURRENT (μA) |
|-----|-----|-----|--------------|
| 0 | 0 | 0 | 6.25 |
| 0 | 0 | 1 | 12.5 |
| 0 | 1 | 0 | 25 |
| 0 | 1 | 1 | 50 |
| 1 | 0 | 0 | 100 |
| 1 | 0 | 1 | 200 |
| 1 | 1 | 0 | 400 |
| 1 | 1 | 1 | 700 |

The default programmed value is as follows:

- Charge pump current = 100 μA
- Test bits: no test mode; bits Up and Do at logic 0
- Rising edge of CKREF: bit edge at logic 0
- COAST and HSYNC inputs are active HIGH: V level and H level at logic 0.

VCO REGISTER

The bits Z2, Z1 and Z0 enable the internal resistance for the VCO filter to be selected.

Table 6 VCO register bits

| Z2 | Z1 | Z0 | RESISTANCE (kΩ) |
|----|----|----|-----------------|
| 0 | 0 | 0 | high impedance |
| 0 | 0 | 1 | 128 |
| 0 | 1 | 0 | 32 |
| 0 | 1 | 1 | 16 |
| 1 | 0 | 0 | 8 |
| 1 | 0 | 1 | 4 |
| 1 | 1 | 0 | 2 |
| 1 | 1 | 1 | 1 |

Table 7 VCO gain control

| V _{CO1} | V _{CO0} | VCO gain (MHz/V) | PIXEL CLOCK FREQUENCY RANGE (MHz) |
|------------------|------------------|------------------|-----------------------------------|
| 1 | 0 | 60 | 10 to 17 |
| 0 | 1 | 30 | 17 to 35 |
| 1 | 0 | 60 | 35 to 60 |
| 1 | 1 | 100 | 60 to 100 |

The bits V_{CO1} and V_{CO0} control the VCO gain.

The default programmed value is as follows:

- Internal resistance = 16 kΩ
- VCO gain = 15 MHz/V.

DIVIDER REGISTER

This register controls the PLL frequency. The bits are the LSB bits.

The default programmed value is 0011 0010 0000 = 800.

The MSB bits (Di11, Di10, Di9) and the LSB bit (Di0) have to be programmed before the bits Di8 to Di1 to have the required divider ratio. The bit Di0 is used for the parity divider number = Di0 = 0 = even number Di0 = 1 = odd number. It should be noted that if the I²C-bus programming is done in mode = 1 and the bit Di0 has to be toggled, then the registers have to be loaded twice to have the update divider ratio.

POWER-DOWN MODE

- When the supply is completely switched off, the registers are set to their default values; in that event they have to be reprogrammed if the required settings are different (e.g. through an EEPROM)
- When the device is in power-down mode, the previously programmed register values remain unaffected.

PHASEA AND PHASEB REGISTERS

The bit Cka is logic 0 when the used clock is the PLL clock, and logic 1 when the used clock is the external clock.

The bit Ckb is logic 0 when the second clock is not used.

The bits Pa4 to Pa0 and Pb4 to Pb0 are used to program the phase shift for the clock, CKADCO, CKAO and CKBO (see Table 8).

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Table 8 Phase registers bits

| Pa4, Pb4 | Pa3, Pb3 | Pa2, Pb2 | Pa1, Pb1 | Pa0, Pb0 | PHASE SHIFT (°) |
|----------|----------|----------|----------|----------|-----------------|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 11.25 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| 1 | 1 | 1 | 1 | 0 | 337.5 |
| 1 | 1 | 1 | 1 | 1 | 348.75 |

The default programmed value is as follows:

- No external clock: CKA at logic 0
- No use of the second clock: CKB at logic 0
- Phase shift for CKAO and CKADCO = 0°
- Phase shift for CKBO = 0°.

I²C-bus protocol

Table 9 I²C-bus address

| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|----|----|----|----|----|------|------|----|
| 1 | 0 | 0 | 1 | 1 | ADD2 | ADD1 | 0 |

The I²C-bus address of the circuit is 10011 xx0.

Bits A2 and A1 are fixed by the potential on pins ADD1 and ADD2. Thus, four TDA8752s can be used on the same system, using the addresses for ADD1 and ADD2 with the I²C-bus. The A0 bit must always be equal to logic 0 because it is not possible to read the data in the register. The timing and protocol for the I²C-bus are standard. Two sequences are available, see Tables 10 and 11.

Table 10 Address sequence for mode 0

| | | | | | | | | | | |
|---|------------|-----|----------------------|-----|------------------------------|-----|----------------------|-----|------|---|
| S | IC ADDRESS | ACK | SUBADDRESS REGISTER1 | ACK | DATA REGISTER1 (see Table 1) | ACK | SUBADDRESS REGISTER2 | ACK | | P |
|---|------------|-----|----------------------|-----|------------------------------|-----|----------------------|-----|------|---|

Where: S = START condition, ACK = acknowledge and P = STOP condition.

Table 11 Address sequence for mode 1

| | | | | | | | | | | |
|---|------------|-----|----------------------|-----|------------------------------|-----|----------------|-----|------|---|
| S | IC ADDRESS | ACK | SUBADDRESS xxx1 1111 | ACK | DATA REGISTER1 (see Table 1) | ACK | DATA REGISTER2 | ACK | | P |
|---|------------|-----|----------------------|-----|------------------------------|-----|----------------|-----|------|---|

Where: S = START condition, ACK = acknowledge and P = STOP condition.

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3-wire protocol

For the 3-wire serial bus the first byte refers to the register address which is programmed. The second byte refers to the data to be sent to the chosen register (see Table 1). The acquisition is achieved via SEN.

Using the 3-wire interface, an indefinite number of ICs can operate on the same system. Pin SEN is used to validate the circuits.

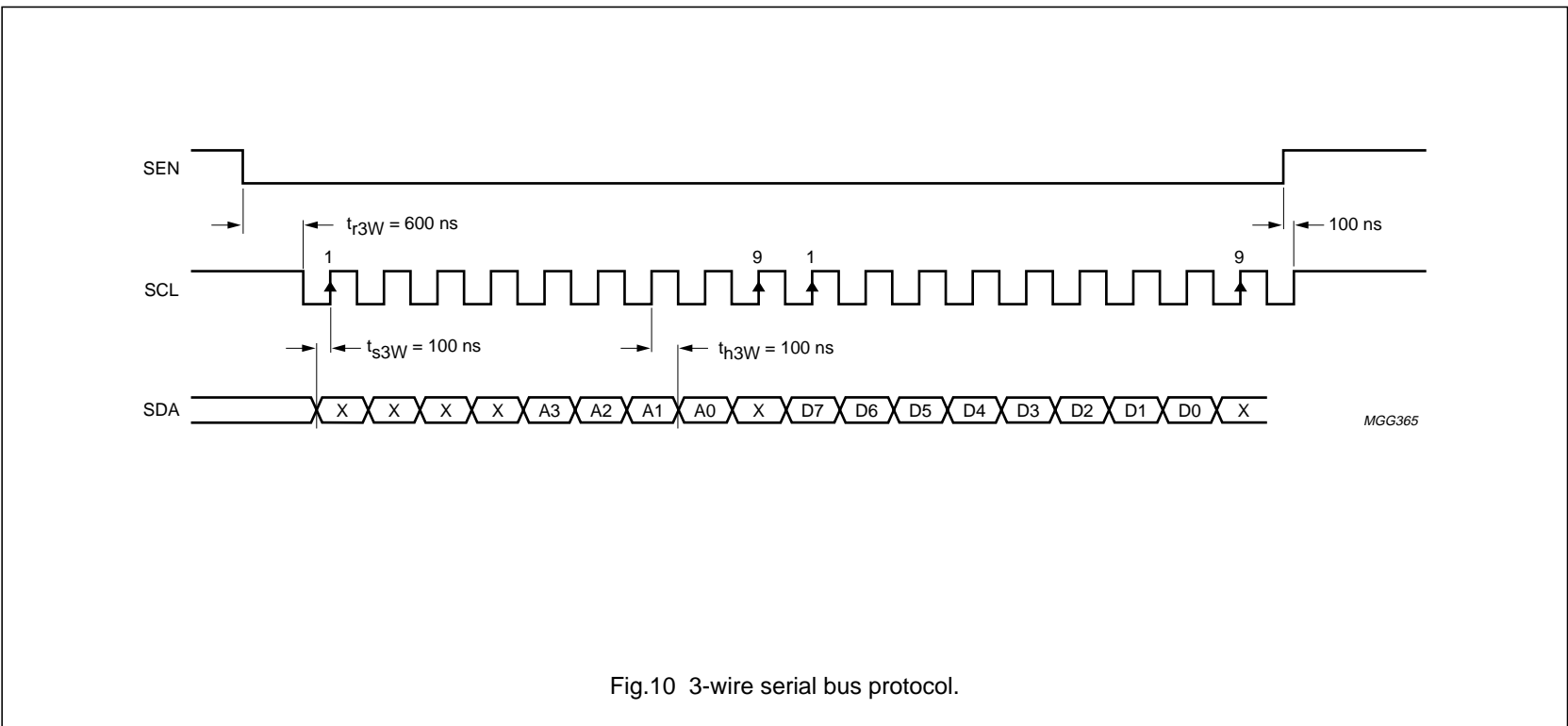


Fig.10 3-wire serial bus protocol.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|------------------------------|------------------------------|------------------|
| V_{CCA} | analog supply voltage | | -0.3 | +7.0 | V |
| V_{CCD} | digital supply voltage | | -0.3 | +7.0 | V |
| V_{DDD} | logic input voltage | | -0.3 | +7.0 | V |
| V_{CCO} | output stages supply voltage | | -0.3 | +7.0 | V |
| ΔV_{CC} | supply voltage differences $V_{CCA} - V_{CCD}$ $V_{CCO} - V_{CCD}$, $V_{CCO} - V_{DDD}$ $V_{CCA} - V_{DDD}$, $V_{CCD} - V_{DDD}$ $V_{CCA} - V_{CCO}$ | | -1.0 -1.0 -1.0 -1.0 | +1.0 +1.0 +1.0 +1.0 | V V V V |
| $V_{i(RGB)}$ | RGB input voltage range | referenced to AGND | -0.3 | +7.0 | V |
| I_o | output current | | - | 10 | mA |
| T_{stg} | storage temperature | | -55 | +150 | °C |
| T_{amb} | operating ambient temperature | | 0 | 70 | °C |
| T_j | junction temperature | | - | 150 | °C |

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|---------------|---------------------------------------------|-------------|-------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 52 | K/W |

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CHARACTERISTICS

$V_{CCA} = V11$ (or $V19$, $V27$ or $V99$) referenced to $AGND$ ($V13$, $V21$, $V29$ or $V96 = 4.75$ to 5.25 V; $V_{CCD} = V95$ referenced to $DGND$ ($V86$) = 4.75 to 5.25 V; $V_{DDD} = V40$ referenced to V_{SSD} ($V41$) = 4.75 to 5.25 V; $V_{CCO} = V59$ (or $V69$, $V79$ or $V85$) referenced to $OGND$ ($V48$, $V60$, $V70$ or $V82$) = 4.75 to 5.25 V; $AGND$, $DGND$, $OGND$ and V_{SSD} short circuited together. $T_{amb} = 0$ to 70 °C; typical values measured at $V_{CCA} = V_{DDD} = V_{CCD} = V_{CCO} = 5$ V and $T_{amb} = 25$ °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------------------------|----------------------------------------------------------|--------------------------------------------------------------------------------------------------------|-------|-------|-------|------|
| Supplies | | | | | | |
| V_{CCA} | analog supply voltage | | 4.75 | 5.0 | 5.25 | V |
| V_{CCD} | digital supply voltage | | 4.75 | 5.0 | 5.25 | V |
| V_{DDD} | logic supply voltage | | 4.75 | 5.0 | 5.25 | V |
| V_{CCO} | output stages supply voltage | | 4.75 | 5.0 | 5.25 | V |
| I_{CCA} | analog supply current | | – | 120 | – | mA |
| I_{DDD} | logic supply current for I ² C-bus and 3-wire | | – | 1.0 | – | mA |
| I_{CCD} | digital supply current | | – | 40 | – | mA |
| I_{CCO} | output stages supply current | ramp input; $f_{CLK} = 100$ MHz | – | 6 | – | mA |
| $I_{CCO(PLL)}$ | output PLL supply current | | – | 5 | – | mA |
| $I_{CCA(PLL)}$ | analog PLL supply current | | – | 28 | – | mA |
| ΔV_{CC} | supply voltage differences | | | | | |
| | $V_{CCA} - V_{CCD}$ | | –0.25 | – | +0.25 | V |
| | $V_{CCO} - V_{CCD}$, $V_{CCO} - V_{DDD}$ | | –0.25 | – | +0.25 | V |
| | $V_{CCA} - V_{DDD}$, $V_{CCD} - V_{DDD}$ | | –0.25 | – | +0.25 | V |
| | $V_{CCA} - V_{CCO}$ | | –0.25 | – | +0.25 | V |
| P_{tot} | total power consumption | ramp input; $f_{CLK} = 100$ MHz | – | 1.0 | – | W |
| P_{pd} | power consumption in power-down mode | | – | 87 | – | mW |
| R, G and B amplifiers | | | | | | |
| B | bandwidth | –3 dB; $T_{amb} = 25$ °C | 250 | – | – | MHz |
| t_{set} | settling time of the block ADC plus AGC | full-scale (black-to-white) transition; input signal settling time < 1 ns; 1 to 99%; $T_{amb} = 25$ °C | – | 4.5 | 6 | ns |
| $G_{NCOARSE}$ | coarse gain range | $V_{ref} = 2.5$ V; minimum coarse gain register; code = 32; (see Fig.8) | – | –1.67 | – | dB |
| | | maximum coarse gain register; code = 99; (see Fig.8) | – | 8 | – | dB |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--------------------------|----------------------------------------------------------|----------------------------------------------------------------------------------------------|------|-------|------|--------|
| G _{FINE} | fine gain correction range | fine register input code = 0; (see Fig.9) | – | 0 | – | dB |
| | | fine register input code = 31; (see Fig.9) | – | –0.5 | – | dB |
| $\Delta G_{amp}/T$ | amplifier gain stability as a function of temperature | V _{ref} = 2.5 V with 100 ppm/°C maximum variation | – | – | 200 | ppm/°C |
| I _{GC} | gain current | | – | ±20 | – | µA |
| t _{stab} | amplifier gain adjustment speed | HSYNC active; capacitors on pins 8, 16 and 24 = 22 nF | – | 25 | – | mdB/µs |
| V _{i(p-p)} | input voltage range (peak-to-peak value) | corresponding to full-scale output | 0.4 | – | 1.2 | V |
| t _{r(Vi)} | input voltage rise time | f _i = 100 MHz; square wave | – | – | 2.5 | ns |
| t _{f(Vi)} | input voltage fall time | f _i = 100 MHz; square wave | – | – | 2.5 | ns |
| G _{E(rms)} | channel-to-channel gain matching (RMS value) | maximum coarse gain; T _{amb} = 25 °C | – | 1 | – | % |
| | | minimum coarse gain; T _{amb} = 25 °C | – | 2 | – | % |
| Clamps | | | | | | |
| P _{CLP} | precision | black level noise on RGB channels = 10 mV (max.) (RMS value); T _{amb} = 25 °C | –1 | – | +1 | LSB |
| t _{COR1} | clamp correction time to within ±10 mV | ±100 mV black level input variation; clamp capacitor = 4.7 nF | – | – | 300 | ns |
| t _{COR2} | clamp correction time to less than 1 LSB | ±100 mV black level input variation; clamp capacitor = 4.7 nF | – | – | 10 | lines |
| t _{W(CLP)} | clamp pulse width | | 500 | – | 2000 | ns |
| CLP _E | channel-to-channel clamp matching | | –1 | – | +1 | LSB |
| A _{off} | code clamp reference | clamp register input code = 0 | – | –63.5 | – | LSB |
| | | clamp register input code = 255 | – | 64 | – | LSB |
| Phase-locked loop | | | | | | |
| j _{PLL(rms)} | long term PLL jitter (RMS value) | f _{CLK} = 60 MHz; see Table 13 | – | 450 | – | ps |
| | | f _{CLK} = 100 MHz; see Table 13 | – | 360 | – | ps |
| DR | divider ratio | | 100 | – | 4095 | |
| f _{ref} | reference clock frequency range | | 15 | – | 280 | kHz |
| f _{PLL} | output clock frequency range | | 12 | – | 100 | MHz |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------------------------------------------------|---------------------------------|------------------------------------------------------------------------------------------------------------------------|------|----------------------------|-----------|-------|
| t_{COASTmax} | maximum coast mode time | | – | – | 40 | lines |
| t_{recap} | PLL recapture time | when coast mode is aborted | – | 3 | – | lines |
| t_{cap} | PLL capture time | in start-up conditions | – | – | 5 | ms |
| Φ_{step} | phase shift step | $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$ | – | 11.25 | – | deg |
| ADCs | | | | | | |
| f_{s} | maximum sampling frequency | TDA8752/6 | 60 | – | – | MHz |
| | | TDA8752/8 | 100 | – | – | MHz |
| INL | DC integral non linearity | from IC analog input to digital output; ramp input; $f_{\text{CLK}} = 100\text{ MHz}$ | – | ± 0.5 | ± 1.5 | LSB |
| DNL | DC differential non linearity | from IC analog input to digital output; ramp input; $f_{\text{CLK}} = 100\text{ MHz}$ | – | ± 0.5 | ± 1.0 | LSB |
| ENOB | effective number of bits | from IC analog input to digital output; 10 kHz sine wave input; ramp input; $f_{\text{CLK}} = 100\text{ MHz}$; note 1 | – | 7.4 | – | bits |
| Signal-to-noise ratio | | | | | | |
| S/N | signal-to-noise ratio | maximum gain; $f_{\text{CLK}} = 100\text{ MHz}$ | – | 45 | – | dB |
| | | minimum gain; $f_{\text{CLK}} = 100\text{ MHz}$ | – | 44 | – | dB |
| Spurious free dynamic range | | | | | | |
| SFDR | spurious free dynamic range | maximum gain; $f_{\text{CLK}} = 100\text{ MHz}$ | – | 60 | – | dB |
| | | minimum gain; $f_{\text{CLK}} = 100\text{ MHz}$ | – | 60 | – | dB |
| Clock timing output (CKADCO, CKBO and CKA0) | | | | | | |
| η_{ext} | ADC clock duty cycle | 100 MHz output | 45 | 50 | 55 | % |
| $f_{\text{CLK(max)}}$ | maximum clock frequency | | 100 | – | – | MHz |
| Clock timing input (CKEXT) | | | | | | |
| $f_{\text{CLK(max)}}$ | maximum clock frequency | | 100 | – | – | MHz |
| t_{CPH} | clock pulse width HIGH | | 3.6 | – | – | ns |
| t_{CPL} | clock pulse width LOW | | 4.5 | – | – | ns |
| $t_{\text{d(CLKO)}}$ | delay from CKEXT to CKADCO | INV set to LOW | 13.6 | 14.7 | 15.2 | ns |
| | | INV set to HIGH | – | $\frac{t_{\text{CLK}}}{2}$ | – | ns |
| Δt_{sample} | time difference between samples | operating in the same supply and temperature condition | – | 0.1 | 0.3 | ns |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------------------------------------------------------------------------------------|-------------------------------------------------------------|--------------------------|------|-----------|------|------------------|
| Data timing (see Fig.11); $f_{CLK} = 100 \text{ MHz}$; $C_L = 10 \text{ pF}$; note 2 | | | | | | |
| $t_{d(s)}$ | sampling delay time | referenced to CKADCO | – | – | – | ns |
| $t_{d(o)}$ | output delay time | | – | –3.3 | –2.6 | ns |
| $t_{h(o)}$ | output hold time | | 4.6 | 5.5 | – | ns |
| 3-state output delay time; (see Fig.12) | | | | | | |
| t_{dZH} | output enable HIGH | | – | 12 | – | ns |
| t_{dZL} | output enable LOW | | – | 10 | – | ns |
| t_{dHZ} | output disable HIGH | | – | 50 | – | ns |
| t_{dLZ} | output disable LOW | | – | 65 | – | ns |
| PLL clock output | | | | | | |
| V_{OL} | LOW-level output voltage | $I_o = 1 \text{ mA}$ | – | 0.3 | 0.8 | V |
| V_{OH} | HIGH-level output voltage | $I_o = -1 \text{ mA}$ | 2.4 | 3.5 | – | V |
| I_{OL} | LOW-level output current | $V_{OL} = 0.4 \text{ V}$ | – | 2 | – | mA |
| I_{OH} | HIGH-level output current | $V_{OH} = 2.7 \text{ V}$ | – | –0.4 | – | mA |
| ADC data outputs | | | | | | |
| V_{OL} | LOW-level output voltage | $I_o = 1 \text{ mA}$ | – | 0 | 0.8 | V |
| V_{OH} | HIGH-level output voltage | $I_o = -1 \text{ mA}$ | 2.4 | V_{CCD} | – | V |
| I_{OL} | LOW-level output current | $V_{OL} = 0.4 \text{ V}$ | – | 2 | – | mA |
| I_{OH} | HIGH-level output current | $V_{OH} = 2.7 \text{ V}$ | – | –0.5 | – | mA |
| TTL digital inputs (CKREF, COAST, CKEXT, INV, HSYNC and CLP) | | | | | | |
| V_{IL} | LOW level input voltage | | – | – | 0.8 | V |
| V_{IH} | HIGH level input voltage | | 2.0 | – | – | V |
| I_{IL} | LOW level input current | $V_{IL} = 0.4 \text{ V}$ | 400 | – | – | μA |
| I_{IH} | HIGH level input current | $V_{IH} = 2.7 \text{ V}$ | – | – | 100 | μA |
| Z_i | input impedance | | – | 4 | – | $\text{k}\Omega$ |
| C_i | input capacitance | | – | 4.5 | – | pF |
| 3-wire serial bus | | | | | | |
| t_{reset} | reset time of the chip before 3-wire communication | | – | 600 | – | ns |
| t_{su} | data set-up time | | – | 100 | – | ns |
| t_h | data hold time | | – | 100 | – | ns |
| I²C-bus; see note 3 | | | | | | |
| f_{SCL} | clock frequency | | 0 | – | 100 | kHz |
| t_{BUF} | time the bus must be free before new transmission can start | | 4.7 | – | – | μs |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---------------|-----------------------------------|-------------------------|------|------|------|---------|
| $t_{HD;STA}$ | start condition hold time | | 4.0 | – | – | μs |
| $t_{SU;STA}$ | start condition set-up time | repeated start | 4.7 | – | – | μs |
| t_{CKL} | LOW level clock period | | 4.7 | – | – | μs |
| t_{CKH} | HIGH level clock period | | 4.0 | – | – | μs |
| $t_{SU;DAT}$ | data set-up time | | 250 | – | – | ns |
| $t_{HD;DAT}$ | data hold time | | 0 | – | – | ns |
| t_r | SDA and SCL rise time | for $f_{SCL} = 100$ kHz | – | – | 1.0 | μs |
| t_f | SDA and SCL fall time | for $f_{SCL} = 100$ kHz | – | – | 300 | ns |
| $t_{SU;STOP}$ | stop condition set-up time | | 4.0 | – | – | μs |
| $C_{L(bus)}$ | capacitive load for each bus line | | – | – | 400 | pF |

Notes to the characteristics

1. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8000 acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half clock frequency (NYQUIST frequency). Conversion-to-noise ratio: $S/N = EB \times 6.02 + 1.76$ dB.
2. Output data acquisition is available after the maximum delay time $t_{d(o)}$, which is the time during which the data is available. All the timings are given for a 10 pF capacitive load. A higher load can be used but the timing must then be rechecked.
3. The I²C-bus timings are given for a frequency of 100 kbit/s (100 kHz). This bus can be used at a frequency of 400 kbit/s (400 kHz).

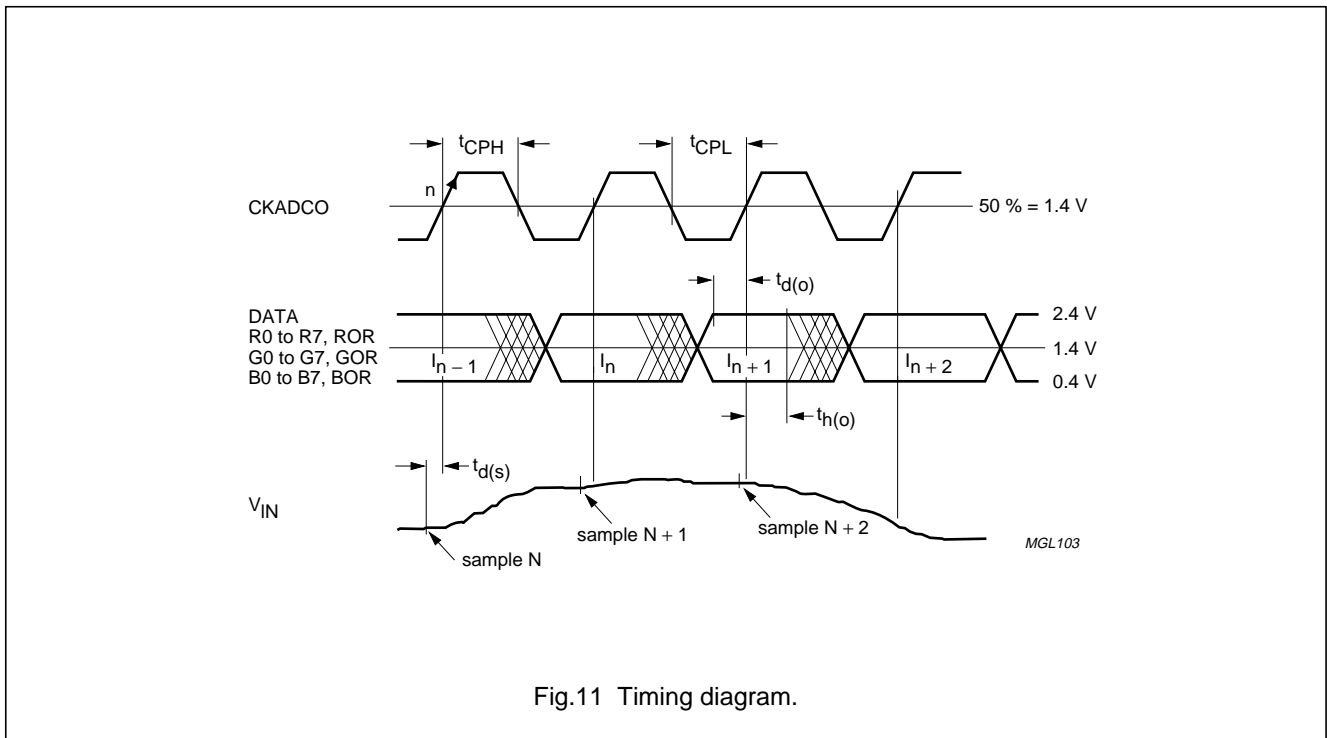


Fig.11 Timing diagram.

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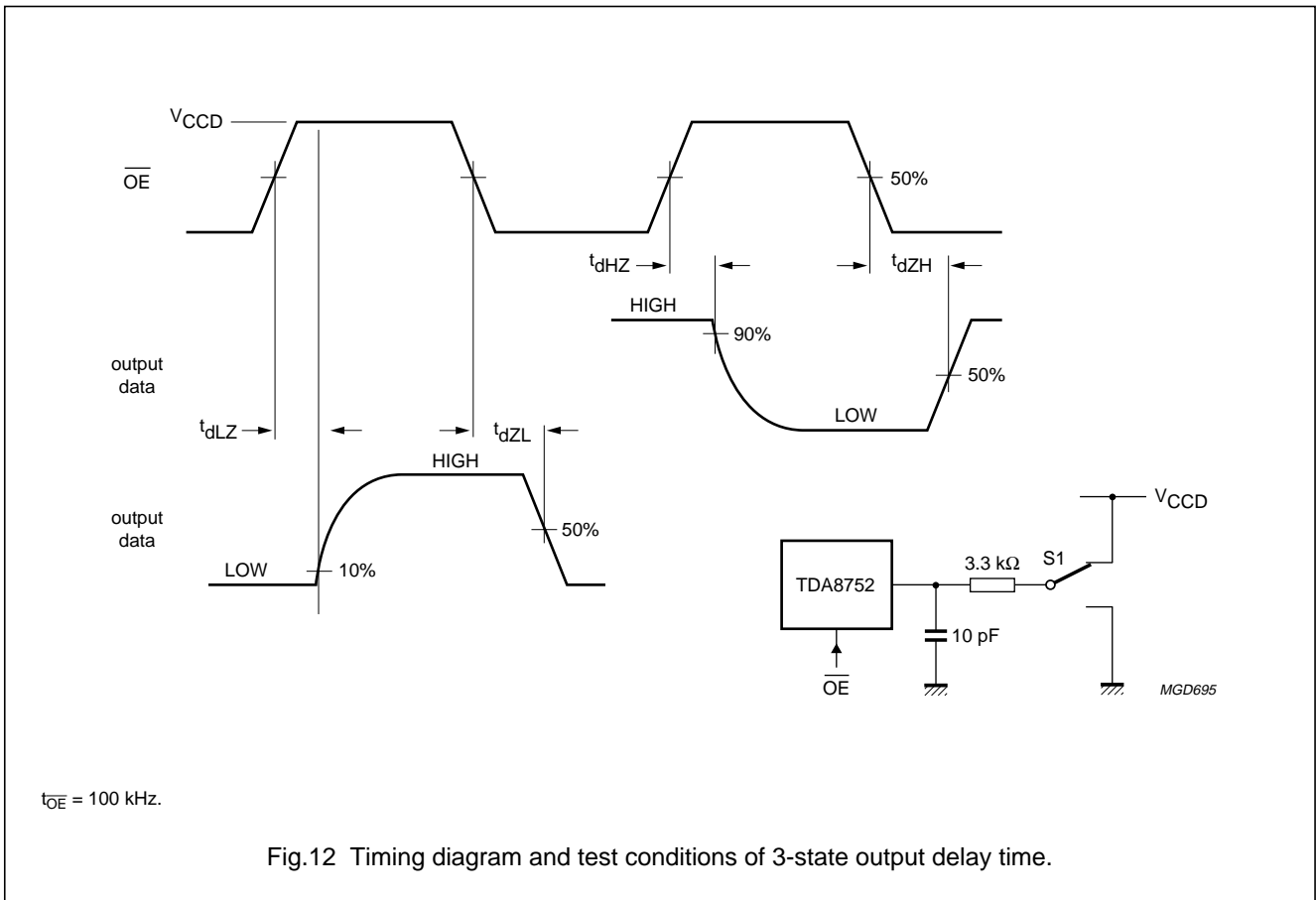


Table 12 Test conditions for Fig.12

| TEST | SWITCH S1 |
|-----------|-----------|
| t_{dLZ} | V_{CCD} |
| t_{dZL} | V_{CCD} |
| t_{dHZ} | GND |
| t_{dZH} | GND |

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APPLICATION INFORMATION

Table 13 Examples of PLL settings and performances; note 1

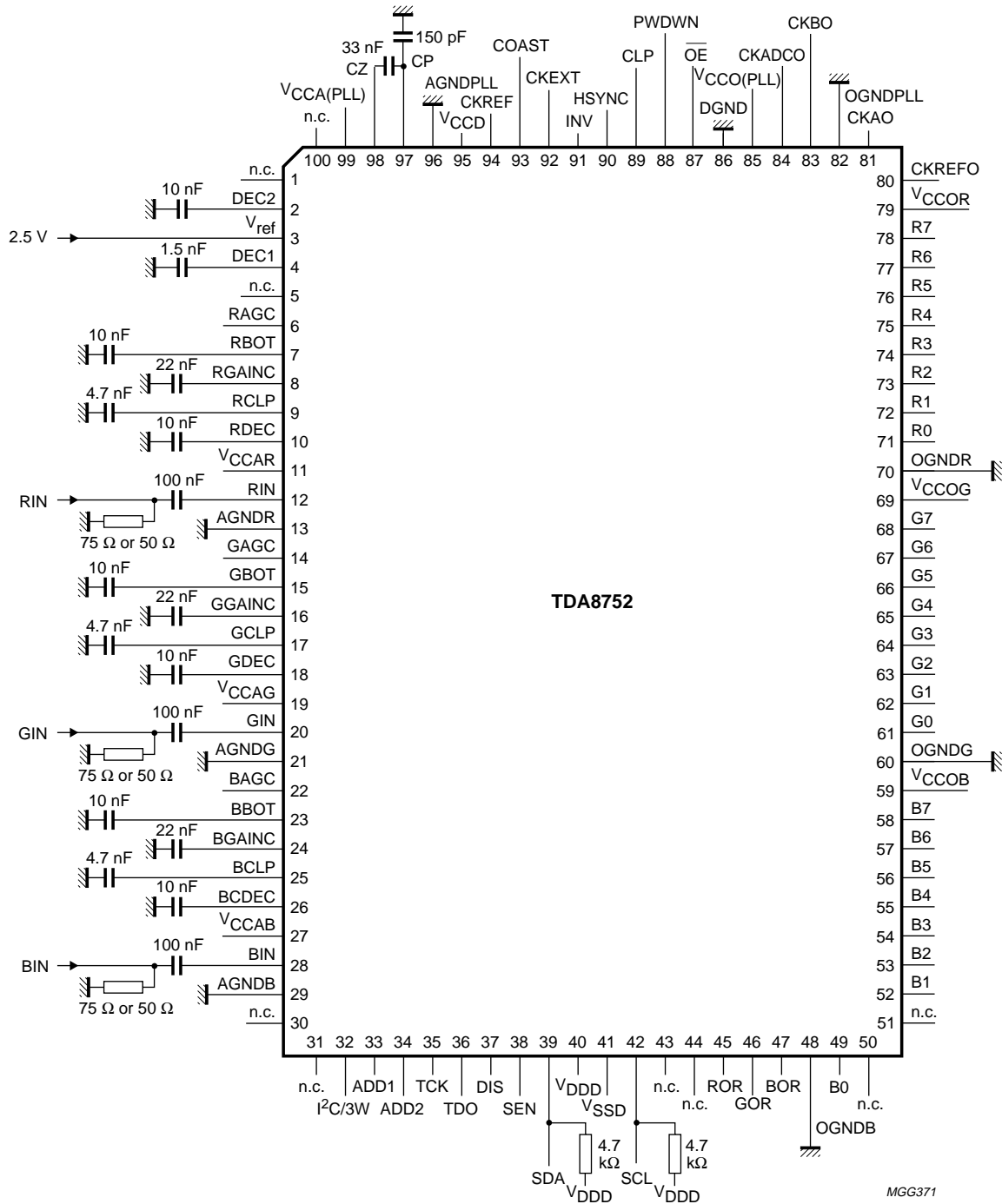
| VIDEO STANDARDS | f _{ref} (kHz) | f _{CLK} (MHz) | N | KO (MHz/V) | CZ (nF) | CP (nF) | I _P (μA) | Z (kΩ) | LONG TIME JITTER ⁽²⁾ | | PLL PHASE DRIFT ⁽³⁾ (ns) |
|------------------|------------------------|------------------------|------|------------|---------|---------|---------------------|--------|---------------------------------|----------|-------------------------------------|
| | | | | | | | | | ps (RMS) | ns (p-p) | |
| CGA: 640 × 200 | 15.75 | 14.3 | 912 | 15 | 150 | 1 | 200 | 4 | – | – | 1.2 |
| VGA: 640 × 480 | 31.5 | 25.2 | 800 | 30 | 150 | 1 | 400 | 2 | 610 | 3.6 | 0.7 |
| VESA: 800 × 600 | 48.08 | 50 | 1040 | 60 | 150 | 1 | 700 | 1 | 480 | 2.9 | 0.55 |
| VESA: 1024 × 768 | 60.02 | 78.8 | 1312 | 100 | 150 | 1 | 700 | 1 | 380 | 2.3 | 0.3 |
| SUN: 1152 × 900 | 66.67 | 100 | 1500 | 100 | 150 | 1 | 700 | 1 | 360 | 2.2 | 0.3 |

Notes

1. Values measured at $V_{CCA} = V_{DDD} = V_{CCD} = V_{CCO} = 5\text{ V}$ and $T_{amb} = 25^{\circ}\text{C}$.
2. PLL long-term time jitter is measured at the end of the video line, where it is at its maximum.
3. Measured between 0 and 70 °C.

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All supply pins have to be decoupled, with two capacitors: one for high frequencies (approximately 1 nF) and one for the low frequencies (approximately 100 nF or higher).

Fig.13 Application diagram.

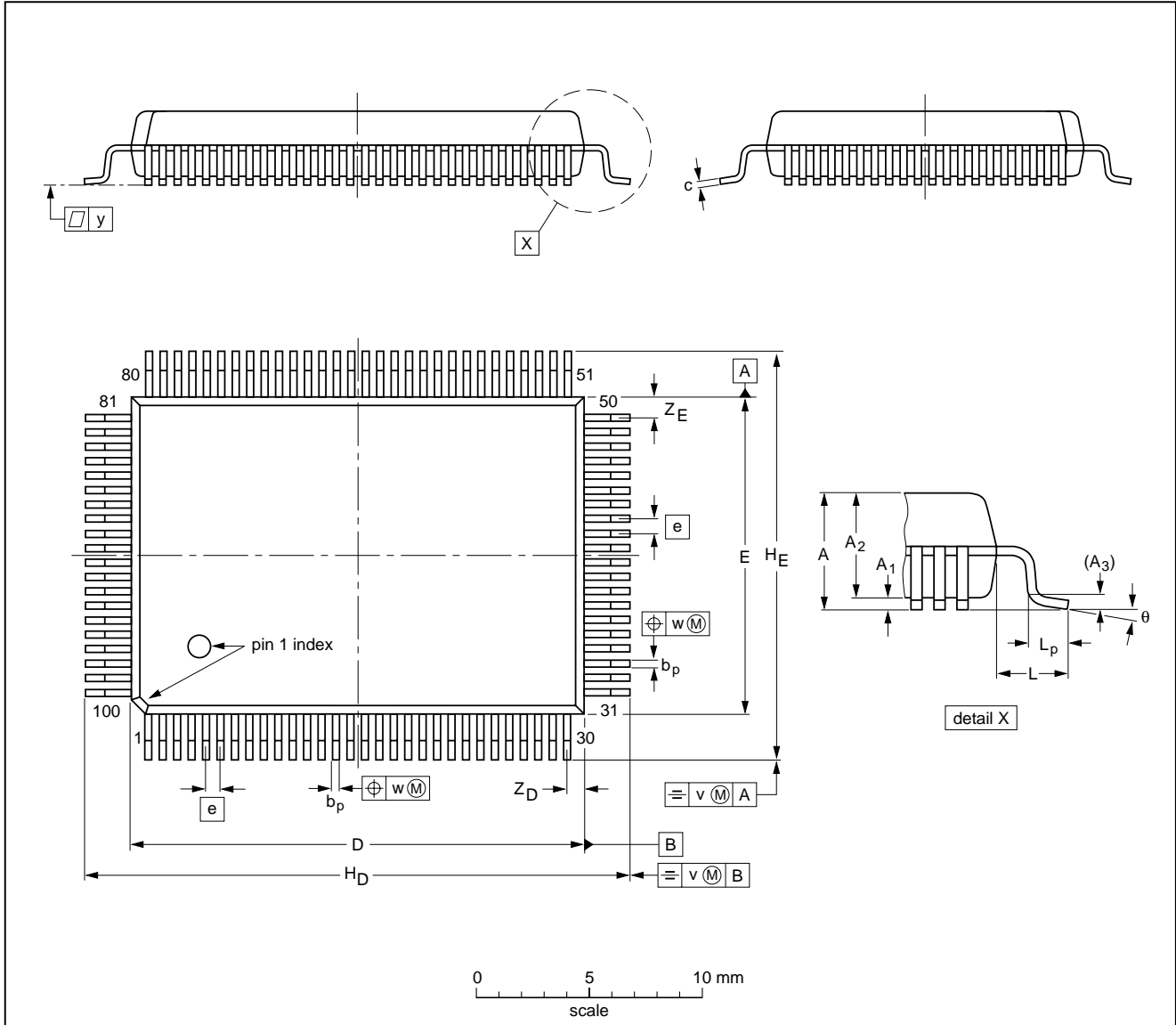
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PACKAGE OUTLINE

QFP100: plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm

SOT317-2



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _D | H _E | L | L _p | v | w | y | Z _D ⁽¹⁾ | Z _E ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|----------------|------|----------------|-----|------|-----|-------------------------------|-------------------------------|----------|
| mm | 3.20 | 0.25 0.05 | 2.90 2.65 | 0.25 | 0.40 0.25 | 0.25 0.14 | 20.1 19.9 | 14.1 13.9 | 0.65 | 24.2 23.6 | 18.2 17.6 | 1.95 | 1.0 0.6 | 0.2 | 0.15 | 0.1 | 0.8 0.4 | 1.0 0.6 | 7° 0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|------|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | |
| SOT317-2 | | | | | 95-02-04 97-08-01 |

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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE | SOLDERING METHOD | |
|---------------------------------|-----------------------------------|-----------------------|
| | WAVE | REFLOW ⁽¹⁾ |
| BGA, SQFP | not suitable | suitable |
| HLQFP, HSQFP, HSOP, HTSSOP, SMS | not suitable ⁽²⁾ | suitable |
| PLCC ⁽³⁾ , SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended ⁽³⁾⁽⁴⁾ | suitable |
| SSOP, TSSOP, VSO | not recommended ⁽⁵⁾ | suitable |

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DEFINITIONS

| | |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| Data sheet status | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
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