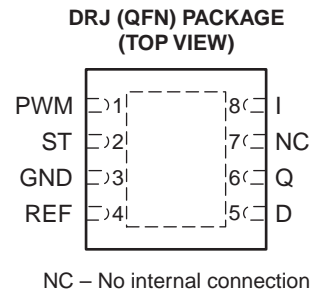


ADJUSTABLE LED DRIVER

FEATURES

- Adjustable Constant Current up to 500 mA ($\pm 5\%$)
- Wide Input Voltage Range up to 42 V
- Low Drop Voltage
- Open-Load Detection
- Overtemperature Protection
- Short-Circuit Proof
- Reverse-Polarity Proof
- Wide Temperature Range: -40°C to 150°C



DESCRIPTION/ORDERING INFORMATION

The TL4242 is an integrated adjustable constant-current source, driving loads up to 500 mA. The output current level can be adjusted via an external resistor. The device is designed to supply high-power LEDs (for example, OSRAM Dragon LA W57B) under the severe conditions of automotive applications, resulting in constant brightness and extended LED lifetime. It is provided in the DRJ (QFN) package. Protection circuits prevent damage to the device in case of overload, short circuit, reverse polarity, and overheat. The connected LEDs are protected against reverse polarity as well as excess voltages up to 45 V.

The integrated PWM input of the TL4242 permits LED brightness regulation by pulse-width modulation (PWM). Due to the high input impedance of the PWM input, the LED driver can be operated as a protected high-side switch.

The TL4242 is characterized for operation from -40°C to 150°C .

An external shunt resistor in the ground path of the connected LEDs is used to sense the LED current. A regulation loop holds the voltage drop at the shunt resistor at a constant level of 177 mV (typ). The constant-current level can be adjusted by selecting the shunt resistance, R_{REF} . Calculate the typical output current using the equation:

$$I_{Q,\text{typ}} = V_{\text{REF}}/R_{\text{REF}}$$

where V_{REF} is the reference voltage (typically 177 mV) (see *Reference Electrical Characteristics*). The equation applies for $R_{\text{REF}} = 0.39 \Omega$ to 10Ω .

The output current is shown as a function of the reference resistance in Figure 1. With the PWM input, the LED brightness can be regulated via duty cycle. Also, PWM = L sets the TL4242 in sleep mode, resulting in a very low current consumption of $<1 \mu\text{A}$ (typ). Due to the high impedance of the PWM input (see Figure 4), the PWM pin also can be used as an enable input.

ORDERING INFORMATION⁽¹⁾

T_J	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 150°C	QFN – DRJ	Reel of 1000	TL4242DRJR	T4242

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

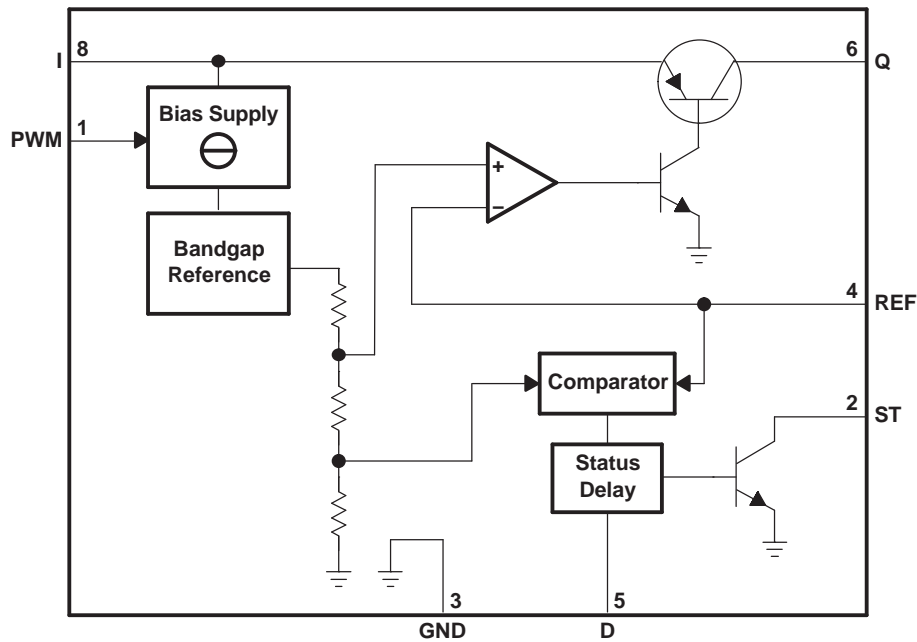


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TERMINAL FUNCTIONS

NO.	NAME	DESCRIPTION
1	PWM	Pulse-width modulation input. If not used, connect to I.
2	ST	Status output. Open-collector output. Connect to an external pullup resistor ($R_{PULLUP} \geq 4.7 \text{ k}\Omega$).
3	GND	Ground
4	REF	Reference input. Connect to a shunt resistor.
5	D	Status delay. To set status reaction delay, connect to GND with a capacitor. If no delay is needed, leave open.
6	Q	Output
7	NC	No internal connection
8	I	Input. Connect directly to GND as close as possible to the device with a 100-nF ceramic capacitor.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V _{CC}	Supply voltage range ⁽²⁾	-42	45	V	
V _I	Input voltage range	D	-0.3	7	V
		PWM	-40	40	V
		REF	-1	16	V
V _O	Output voltage range	Q	-1	41	V
		ST	-0.3	40	V
I _O	Output current range	PWM		±1	mA
		REF		±2	mA
		ST		±5	mA
θ _{JA}	Thermal impedance, junction to ambient ⁽³⁾	JESD 51-5 ⁽⁴⁾		49.5	°C/W
		JESD 51-7 ⁽⁵⁾		114.4	
θ _{JP}	Thermal impedance, junction to pad ⁽³⁾			4.4	°C/W
T _J	Virtual-junction temperature range	-40	150	°C	
T _{stg}	Storage temperature range	-50	150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground terminal.
- (3) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_J(max) - T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-5.
- (5) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4.5	42	V
V _{ST}	Status (ST) output voltage		16	V
V _{PWM}	PWM voltage	0	40	V
C _D	Status delay (D) capacitance	0	2.2	μF
R _{REF}	Reference (REF) resistor	0	10	Ω
T _J	Virtual-junction temperature	-40	150	°C

OVERALL DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, V_I = 13.5 V, R_{REF} = 0.47 Ω, V_{PWM,H}, T_J = -40°C to 150°C, all voltages with respect to ground (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{qL}	Supply current		12	22	mA
I _{qOFF}	Supply current, off mode		0.1	2	μA

OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, $V_I = 13.5\text{ V}$, $R_{REF} = 0.47\ \Omega$, $V_{PWM,H}$, $T_J = -40^\circ\text{C}$ to 150°C , all voltages with respect to ground (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Output current	$V_Q - V_{REF}^{(1)} = 6.6\text{ V}$	357	376	395	mA
		$V_Q - V_{REF} = 6.6\text{ V}$, $R_{REF} = 1\ \Omega$	168	177	185	
		$V_Q - V_{REF} = 6.6\text{ V}$, $R_{REF} = 0.39\ \Omega$	431	454	476	
		$V_Q - V_{REF} = 5.4\text{ V}$ to 7.8 V , $V_I = 9\text{ V}$ to 16 V	357	376	395	
I_{Qmax}	Output current limit	$R_{REF} = 0\ \Omega$		600		mA
V_{dr}	Drop voltage	$I_Q = 300\text{ mA}$		0.35	0.7	V

(1) $V_Q - V_{REF}$ equals the forward voltage sum of the connected LEDs (see [Figure 3](#)).

PWM INPUT ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, $V_I = 13.5\text{ V}$, $R_{REF} = 0.47\ \Omega$, $V_{PWM,H}$, $T_J = -40^\circ\text{C}$ to 150°C , all voltages with respect to ground (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{PWM,H}$	High-level PWM voltage		2.6			V
$V_{PWM,L}$	Low-level PWM voltage				0.7	V
$I_{PWM,H}$	High-level PWM input current	$V_{PWM} = 5\text{ V}$		220	500	μA
$I_{PWM,L}$	Low-level PWM input current	$V_{PWM} = 0\text{ V}$	-1		1	μA
$t_{PWM,ON}$	Delay time, turn on	70% of I_{Qnom} , See Figure 6	0	15	40	μs
$t_{PWM,OFF}$	Delay time, turn off	30% of I_{Qnom} , See Figure 6	0	15	40	μs

REFERENCE (REF) ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, $V_I = 13.5\text{ V}$, $R_{REF} = 0.47\ \Omega$, $V_{PWM,H}$, $T_J = -40^\circ\text{C}$ to 150°C , all voltages with respect to ground (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage	$R_{REF} = 0.39\ \Omega$ to $1\ \Omega$	168	177	185	mV
I_{REF}	Reference input current	$V_{REF} = 180\text{ mV}$	-1	0.1	1	μA

STATUS OUTPUT (ST) ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, $V_I = 13.5\text{ V}$, $R_{REF} = 0.47\ \Omega$, $V_{PWM,H}$, $T_J = -40^\circ\text{C}$ to 150°C , all voltages with respect to ground (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IQL}	Lower status-switching threshold	ST = L	15	25		mV
V_{IQH}	Upper status-switching threshold	ST = H		30	40	mV
V_{STL}	Low-level status voltage	$I_{ST} = 1.5\text{ mA}$			0.4	V
I_{STLK}	Leakage current	$V_{ST} = 5\text{ V}$			5	μA

STATUS DELAY (D) ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, $V_I = 13.5\text{ V}$, $R_{REF} = 0.47\ \Omega$, $V_{PWM,H}$, $T_J = -40^\circ\text{C}$ to 150°C , all voltages with respect to ground (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STHL}	Delay time, status reaction	$C_D = 47\text{ nF}$, ST H→L	6	10	14	ms
t_{STLH}	Delay time, status release	$C_D = 47\text{ nF}$, ST L→H		10	20	μs

TYPICAL CHARACTERISTICS

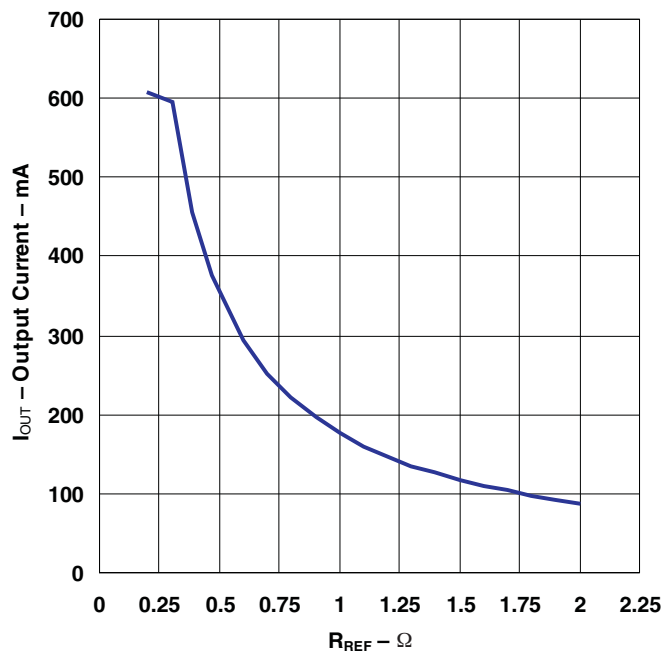


Figure 1. Output Current vs External Resistor

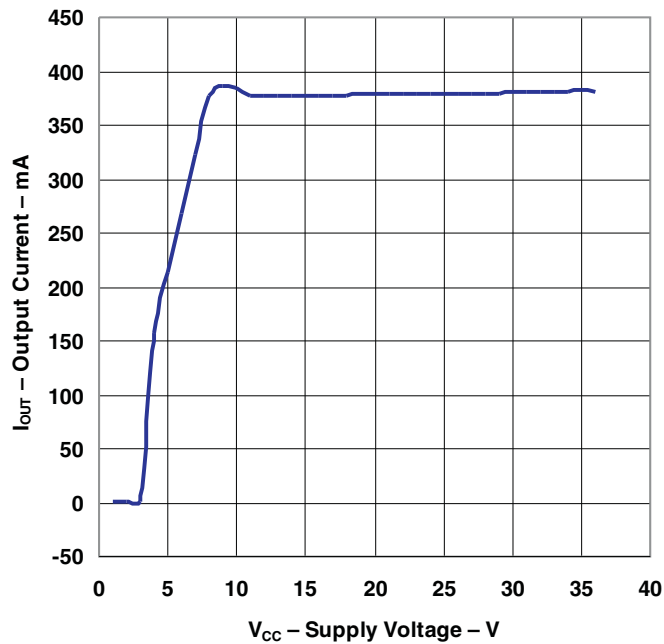


Figure 2. Output Current vs Supply Voltage

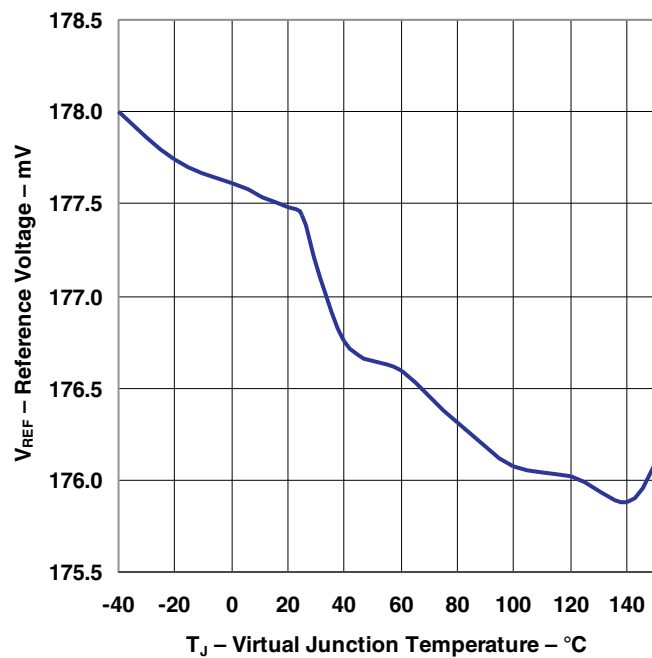


Figure 3. Reference Voltage vs Junction Temperature

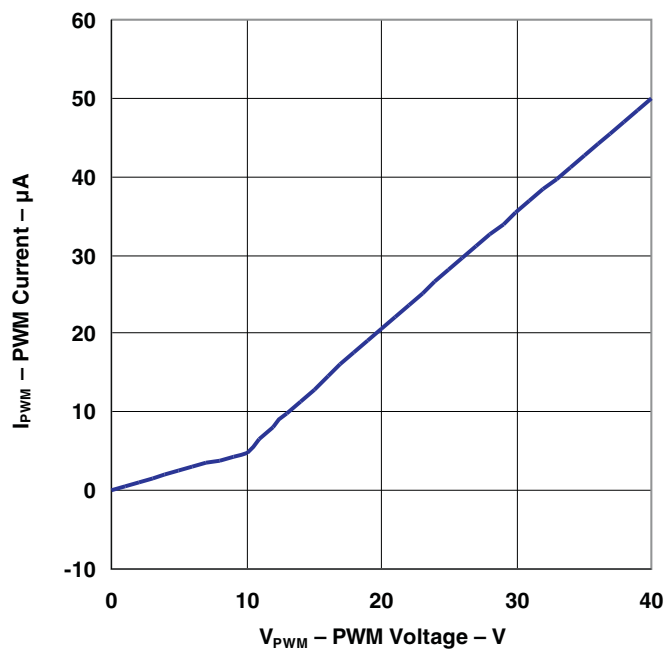


Figure 4. PWM Pin Input Current vs PWM Voltage

APPLICATION INFORMATION

Figure 5 shows a typical application with the TL4242 LED driver. The three LEDs are driven by a supply current that is adjusted by the resistor, R_{REF} , preventing brightness variations due to forward voltage spread of the LEDs. The luminosity spread arising from the LED production process can be compensated via software by an appropriate duty cycle applied to the PWM pin. Therefore, it is not necessary to select LEDs for forward voltage or luminosity classes. The minimum supply voltage calculates as the sum of the LED forward voltages, the TL4242 drop voltage (maximum 0.7 V at a LED current of 300 mA) and the maximum voltage drop at the shunt resistor R_{REF} of 185 mV (max).

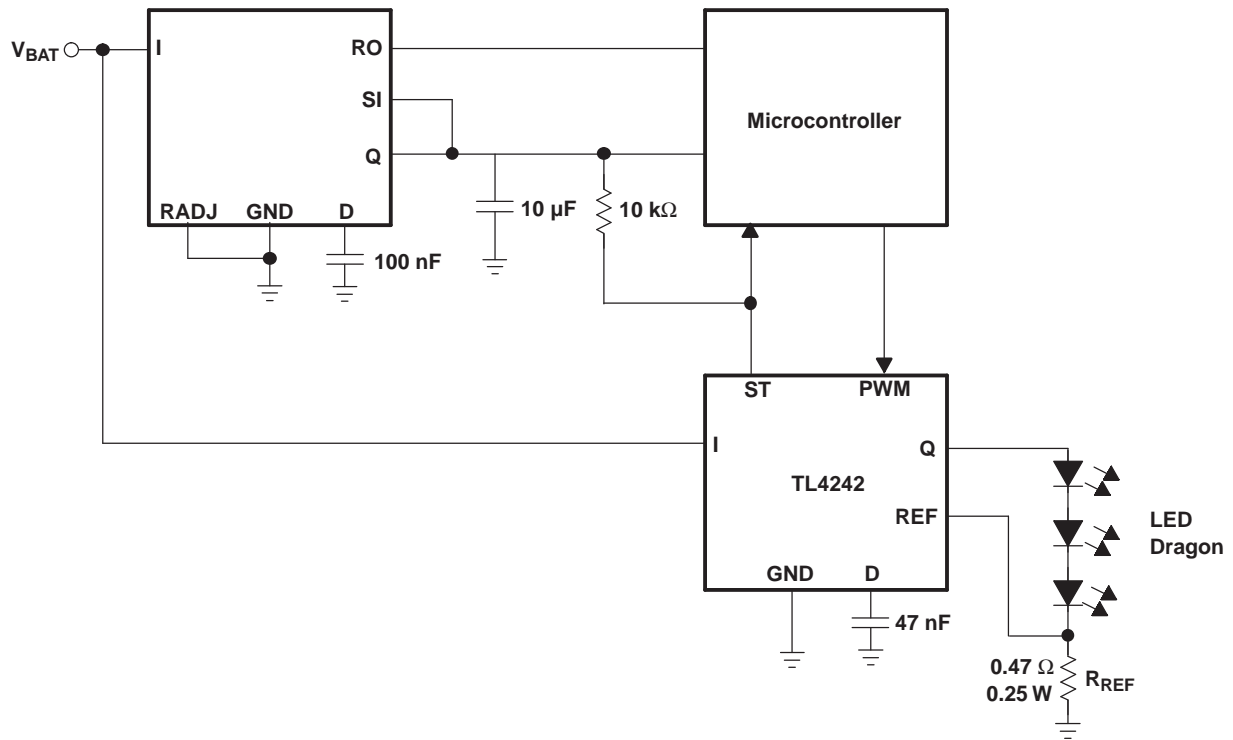


Figure 5. Application Circuit

The status output of the LED driver (ST) detects an open-load condition, enabling supervision of correct LED operation. An LED failure is detected as a voltage drop at the shunt resistor (R_{REF}) below 25 mV (typ). In this case, the status output pin (ST) is set low after a delay time adjustable by an optional capacitor connected to pin D.

The functionality and timing of ST and PWM are shown in Figure 6. The status delay can be adjusted via the capacitor connected to pin D. Delay time scales linearly with capacitance, C_D :

$$t_{STHL,typ} = \frac{C_D}{47 \text{ nF}} \times 10 \text{ ms}$$

$$t_{STLH,typ} = \frac{C_D}{47 \text{ nF}} \times 10 \text{ }\mu\text{s}$$

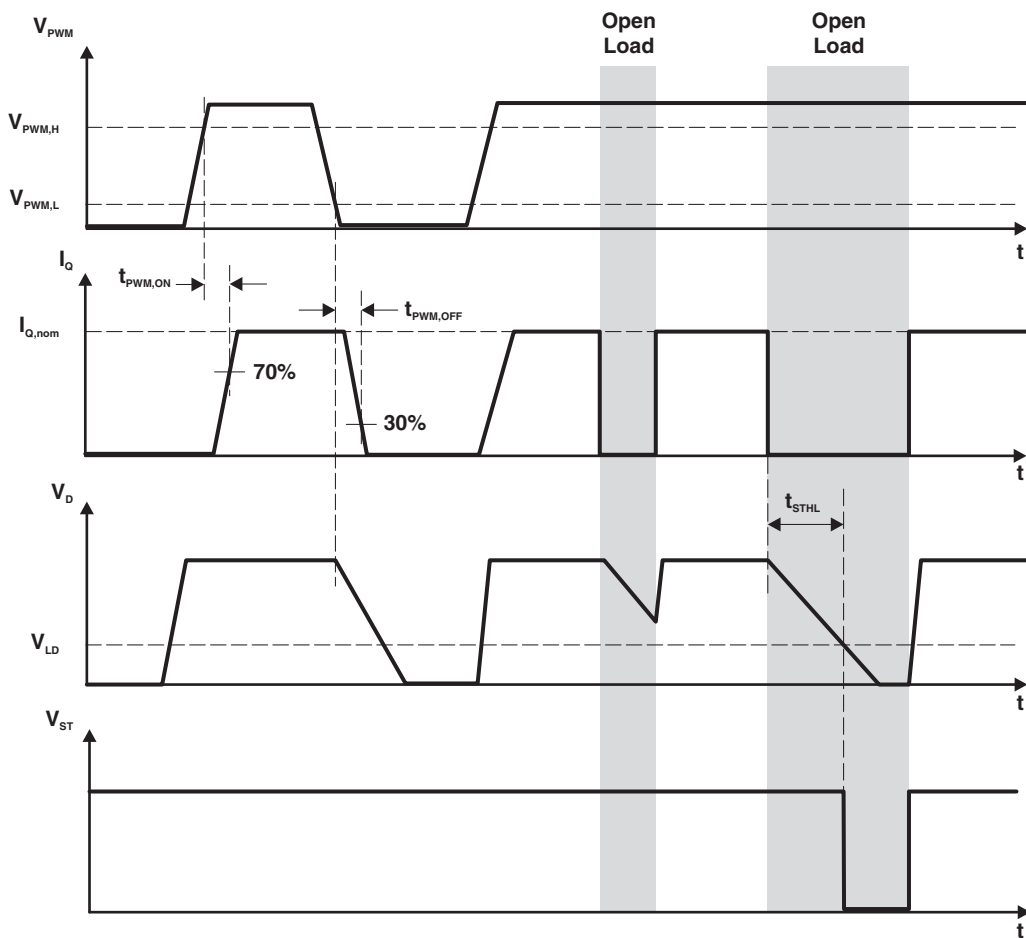


Figure 6. Function and Timing Diagram

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TL4242DRJR	ACTIVE	SON	DRJ	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL4242DRJR	SON	DRJ	8	1000	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

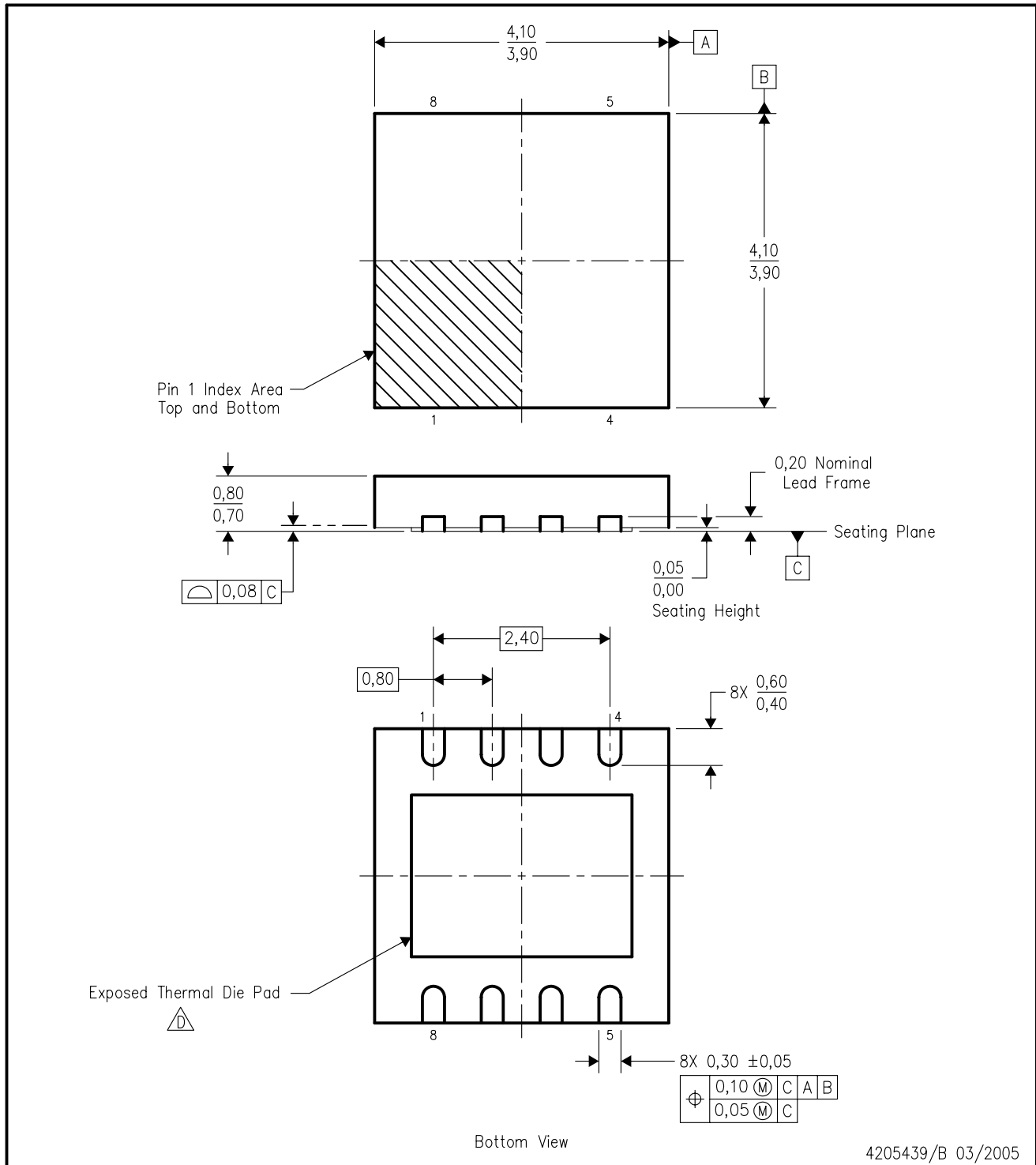


*All dimensions are nominal


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL4242DRJR	SON	DRJ	8	1000	190.5	212.7	31.8

DRJ (S-PDSO-N8)

PLASTIC SMALL OUTLINE



4205439/B 03/2005

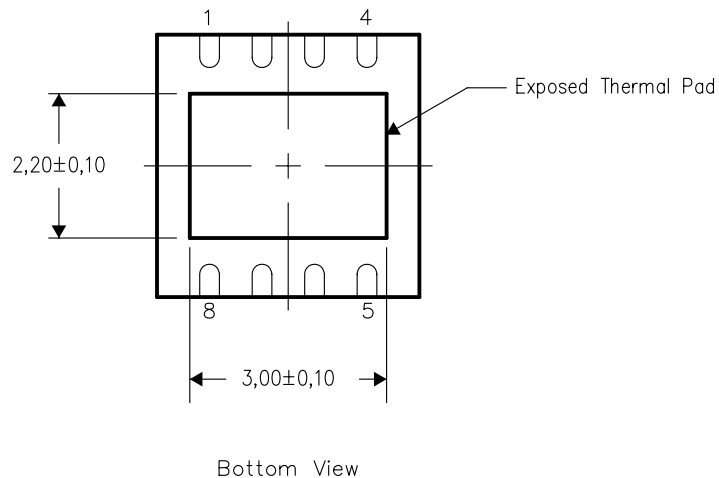
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Package complies to JEDEC MO-229 variation WGGB.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

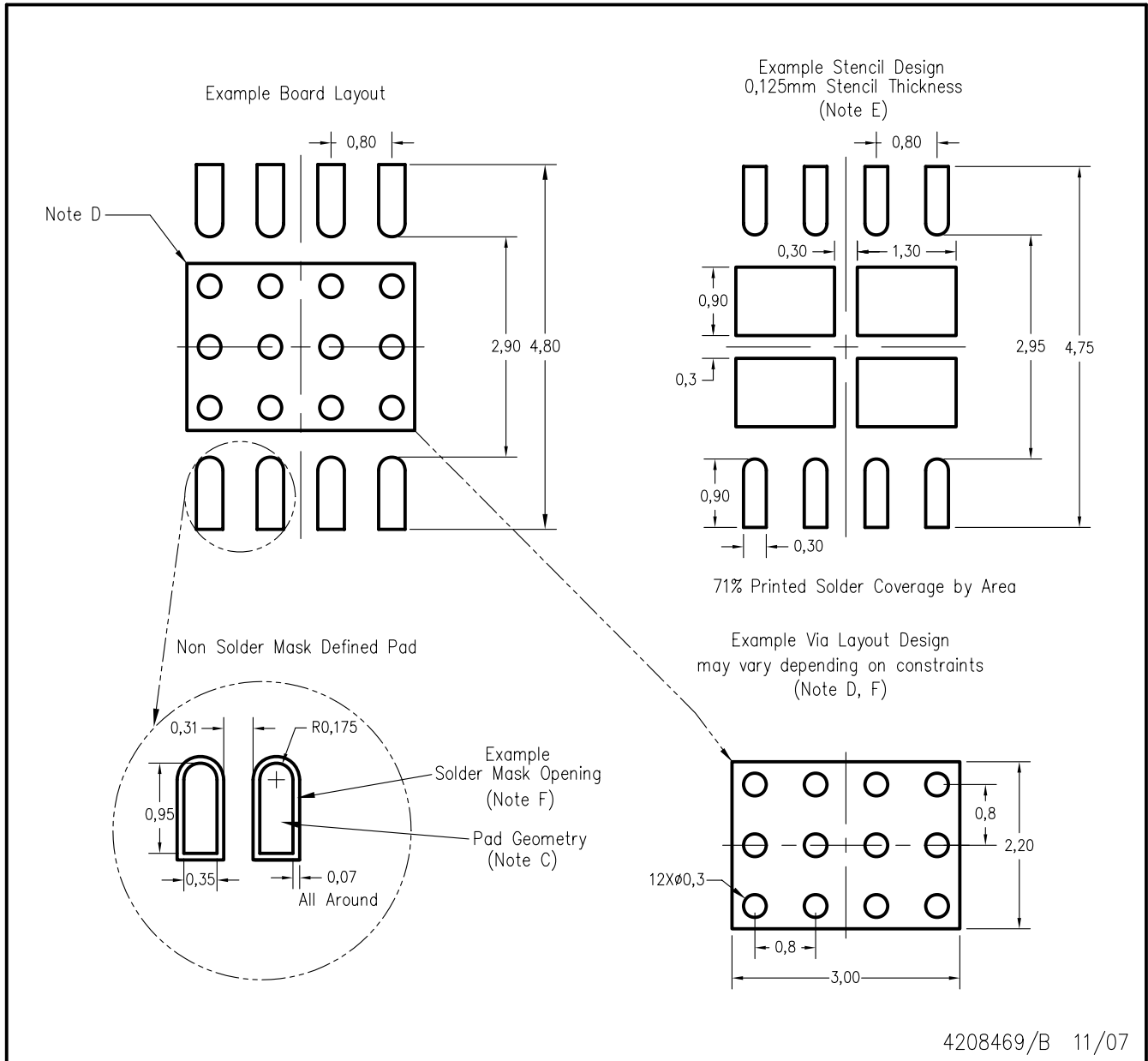
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRJ (S-PDSO-N8)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances and vias tenting recommendations for vias placed in the thermal pad.

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