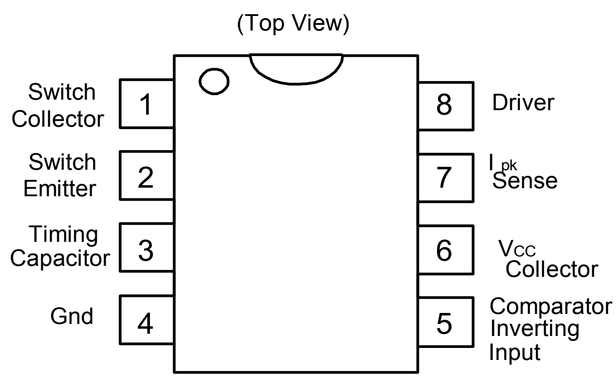
Features

- Operation from 3.0V to 40V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.6A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference

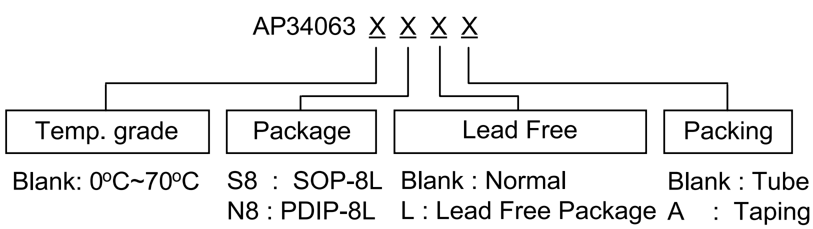
General Description

The AP34063 Series is a monolithic control circuit containing the primary functions required for DC-to-DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series is specifically designed for incorporating in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components.

Pin Connections



Ordering Information



■ Maximum Ratings

Parameter		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	40	V
Comparator Input Voltage Range		V_{IR}	-0.3 ~ +40	V
Switch Collector Voltage		$V_{C(switch)}$	40	V
Switch Emitter Voltage(V_{Pin} 1 = 40V)		$V_{E(switch)}$	40	V
Switch Collector to Emitter Voltage		$V_{CE(switch)}$	40	V
Driver Collector Voltage		$V_{C(driver)}$	40	V
Driver Collector Current (Note 1)		$I_{C(driver)}$	100	mA
Switch Current		I_{SW}	1.6	A
Power Dissipation and Thermal Characteristics	PDIP: T_A = 25°C	P_D	1.25	W
	Thermal Resistance	θ_{JA}	100	°C/W
	SOP: T_A = 25°C	P_D	600	mW
	Thermal Resistance	$R_{\theta JA}$	160	°C/W
Operating Junction Temperature		T_J	+150	°C
Operating Ambient Temperature Range		T_A	0 ~ +70	°C
Storage Temperature Range		T_{stg}	-65 ~ +150	°C

Notes: 1.Maximum package power dissipation limits must be observed.
2.ESD data available upon request.

■ Electrical Characteristics (V_{CC} = 5.0V, unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency(V_{Pin} 5 =0V, C_T =1.0nF, T_A =25°C)	f_{osc}	24	33	42	kHz
Charge Current(V_{CC} =5.0V to 40V, T_A =25°C)	I_{chg}	24	30	42	μA
Discharge Current(V_{CC} =5.0V to 40V, T_A =25°C)	I_{dischg}	140	200	260	μA
Discharge to Charge Current Ratio(Pin 7 to V_{CC}, T_A =25°C)	I_{dischg} / I_{chg}	5.2	6.5	7.5	-
Current Limit Sense Voltage(I_{chg} = I_{dischg}, T_A =25°C)	$V_{ipk(sense)}$	300	400	450	mV
OUTPUT SWITCH (Note 3)					
Saturation Voltage, Darlington Connection (I_{SW} =1.0A, Pins 1,8 connected)	$V_{CE(sat)}$	-	1.0	1.3	V
Saturation Voltage, Darlington Connection (I_{SW} =1.0A, ID = 50mA, Forced ß ≈ 20)	$V_{CE(sat)}$	-	0.45	0.7	V
DC Current Gain(I_{SW} =1.0A, V_{CE} =5.0V, T_A =25°C)	h_{FE}	50	75	-	-
Collector Off-State Current (V_{CE} =40V)	$I_{C(off)}$	-	0.01	100	μA
COMPARATOR					
Threshold Voltage	V_{th}				V
T_A = 25°C		1.225	1.25	1.275	
T = 0°C ~ 75°C		1.21	-	1.29	
Threshold Voltage Line Regulation(V_{CC} =3.0V to 40V)	Reg_{line}	-	1.4	6.0	mV
TOTAL DEVICE					
Supply Current(V_{CC} =5.0V to 40V, C_T =1.0nF, Pin 7 = V_{CC}, $V_{Pin\ 5}$ > V_{th} Pin 2 = Gnd, remaining pins open)	I_{CC}	-	-	3.5	mA

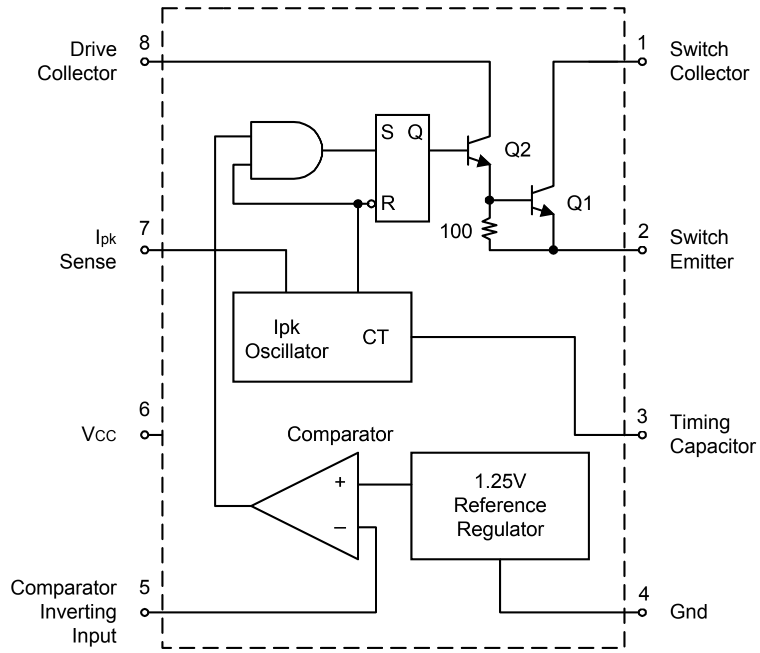
Note: 3.Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

4.If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents (≤300mA) and high driver currents (≥ 30mA), it may take up to 2.0 µs for it to come out of saturation.? This condition will shorten the off time at frequencies ≥ 30kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended:

Forced ß of output switch : $\dfrac{I_C \text{ output}}{I_C \text{ driver - 7.0mA*}} \geq 10$

*The 100Ω resistor in the emitter of the driver device requires about 7.0mA before the output switch conducts.

■ Representative Schematic Diagram



(Bottom View)

Figure 1. Vce(sat) versus Ie

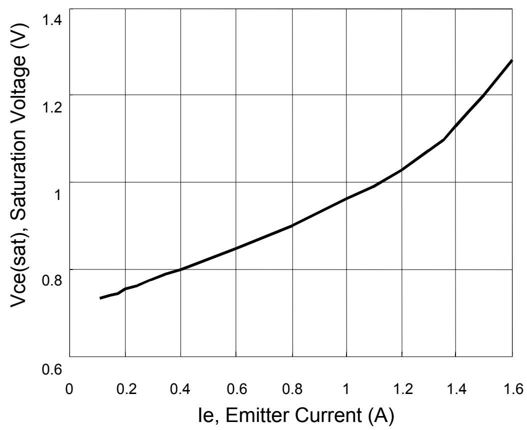


Figure 2. Reference Voltage versus Temp.

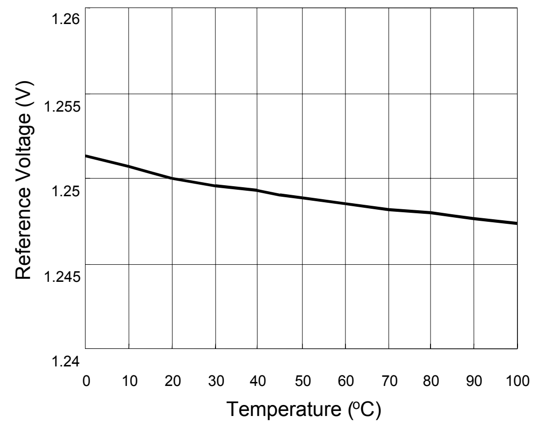


Figure 3. Current Limit Sense Voltage versus Temperature

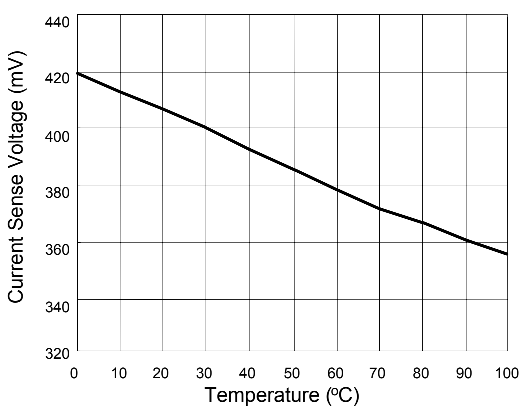


Figure 4. Standby Supply Current versus Supply Voltage

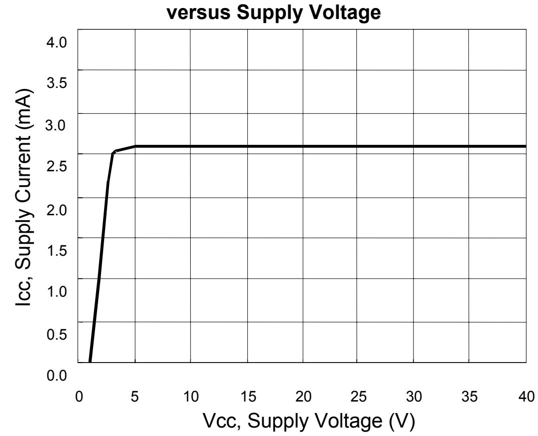


Figure 5. Emitter Follower Configuration Output Saturation Voltage vs. Emitter Current

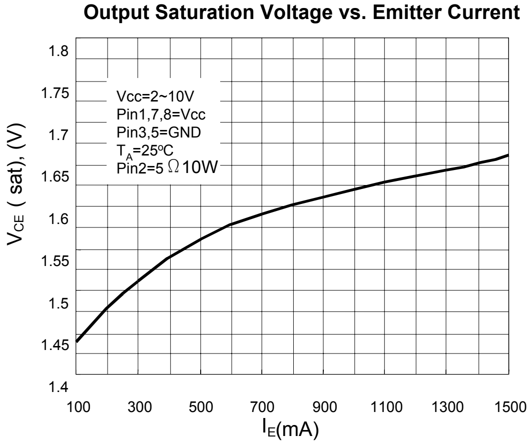
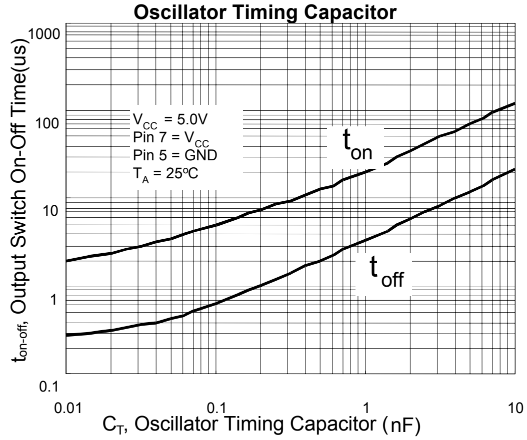
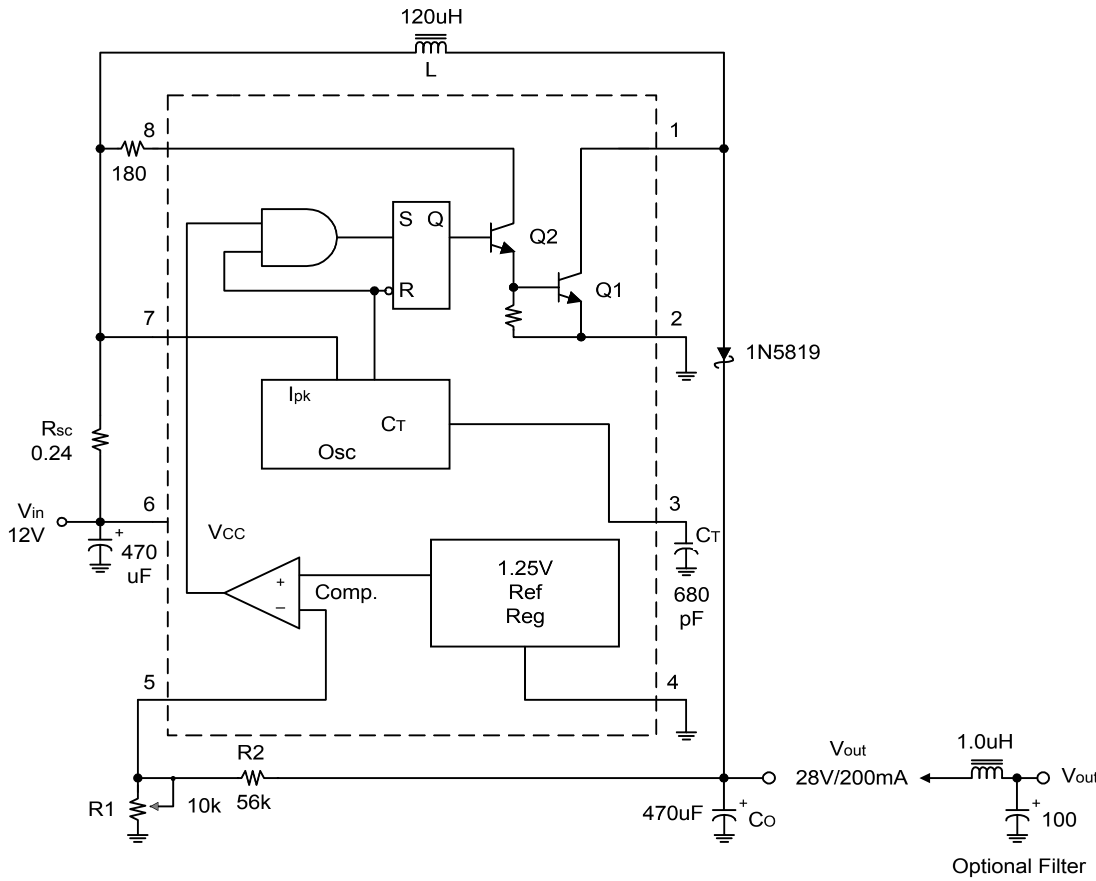


Figure 6.Output Switch On-Off Time versus Oscillator Timing Capacitor



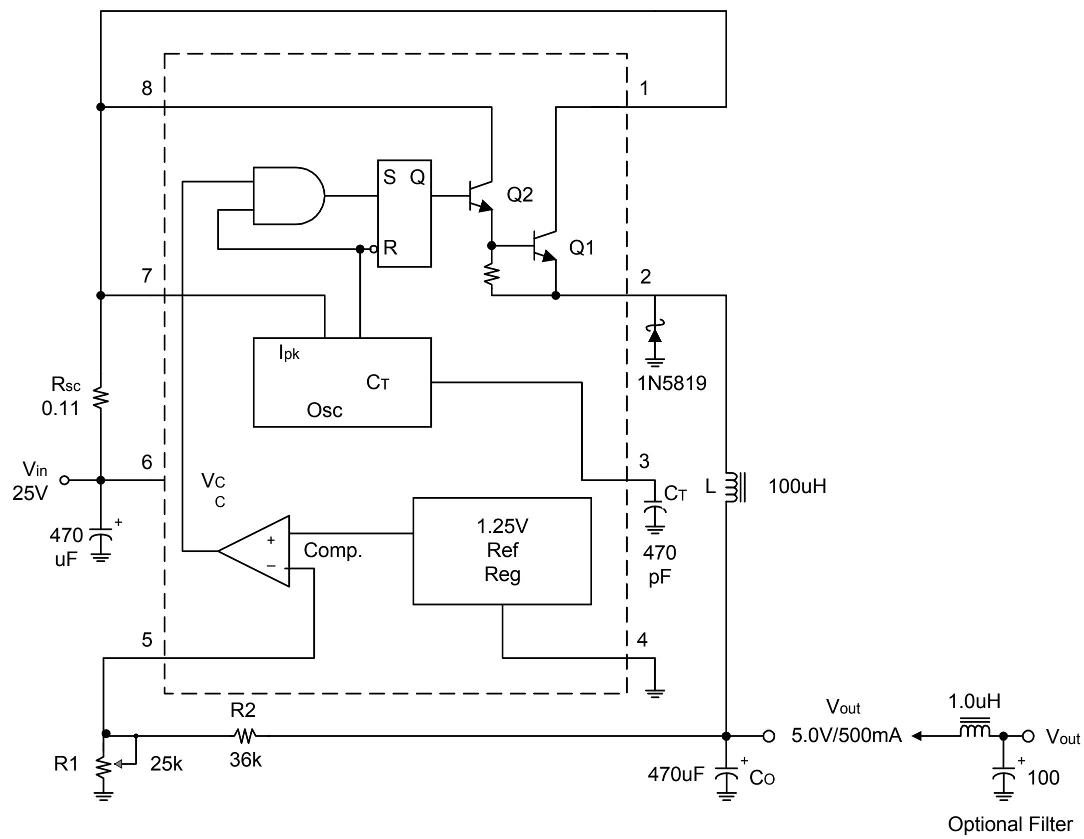
■ Application Circuit

(1) Step-Up Converter



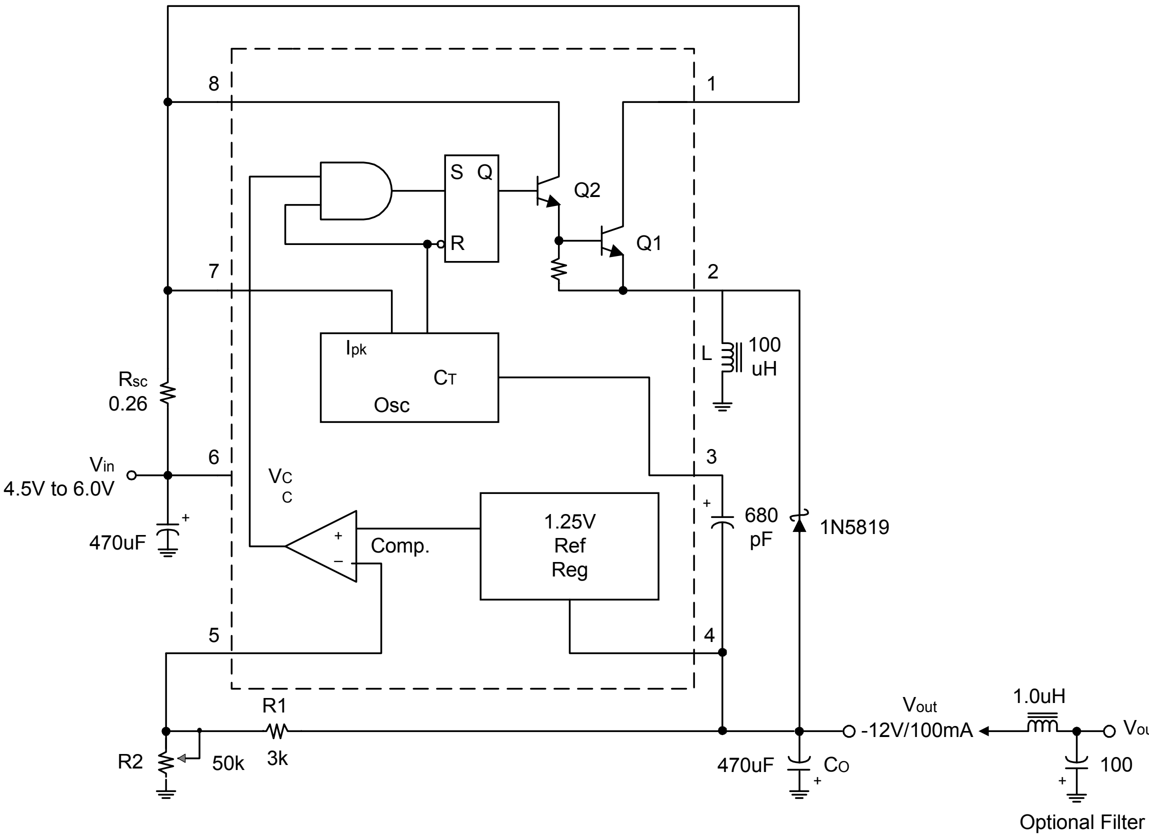
Test	Conditions	Results
Line Regulation	V_{in} =9V to 12V, I_O =200mA	20mV = ± 0.035%
Load Regulation	V_{in} =12V, I_O =50mA to 200mA	15mV = ± 0.035%
Output Ripple	V_{in} =12V, I_O =200mA	500mV_{PP}
Efficiency	V_{in} =12V, I_O =200mA	80%

(2) Step-Down Converter



Test	Conditions	Results
Line Regulation	V_{in} =12V to 24V, I_O =500mA	20mV = ± 0.2%
Load Regulation	V_{in} =24V, I_O =50mA to 500mA	5mV = ± 0.05%
Output Ripple	V_{in} =24V, I_O =500mA	160mV$_{PP}$
Efficiency	V_{in} =24V, I_O =500mA	82%

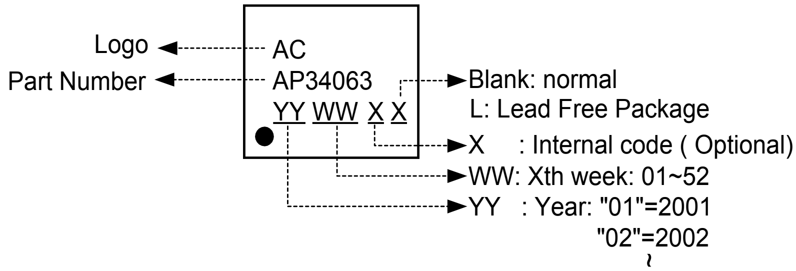
(3) Voltage Inverting Converter



Test	Conditions	Results
Line Regulation	V_{in} =4.5V to 6.0V, I_O =100mA	20mV = ± 0.08%
Load Regulation	V_{in} =5.0V, I_O =20mA to 100mA	30mV = ± 0.12%
Output Ripple	V_{in} =5.0V, I_O =100mA	500mV$_{PP}$
Efficiency	V_{in} =5.0V, I_O =100mA	60%

■ Marking Information

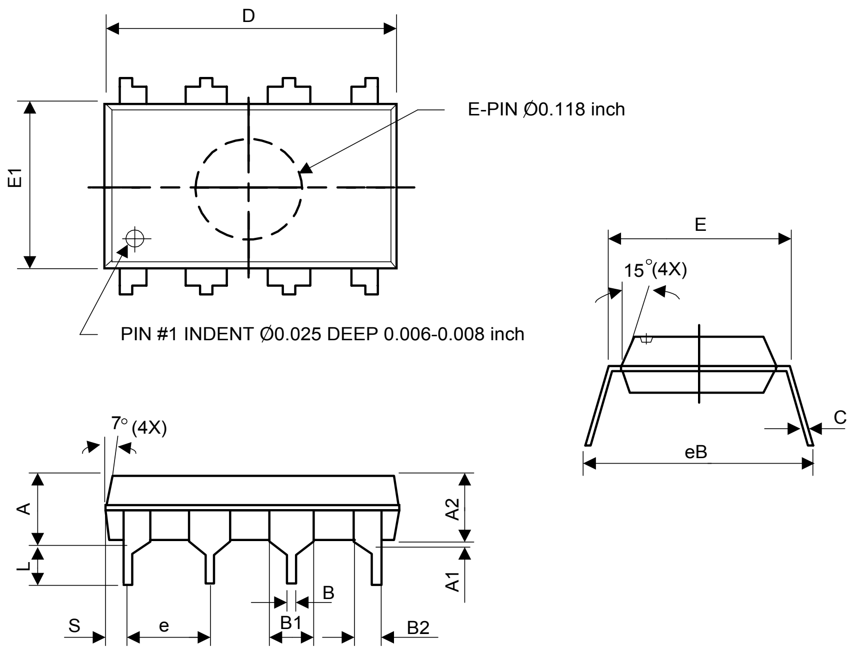
(Top View)



(SOP-8L / PDIP-8L)

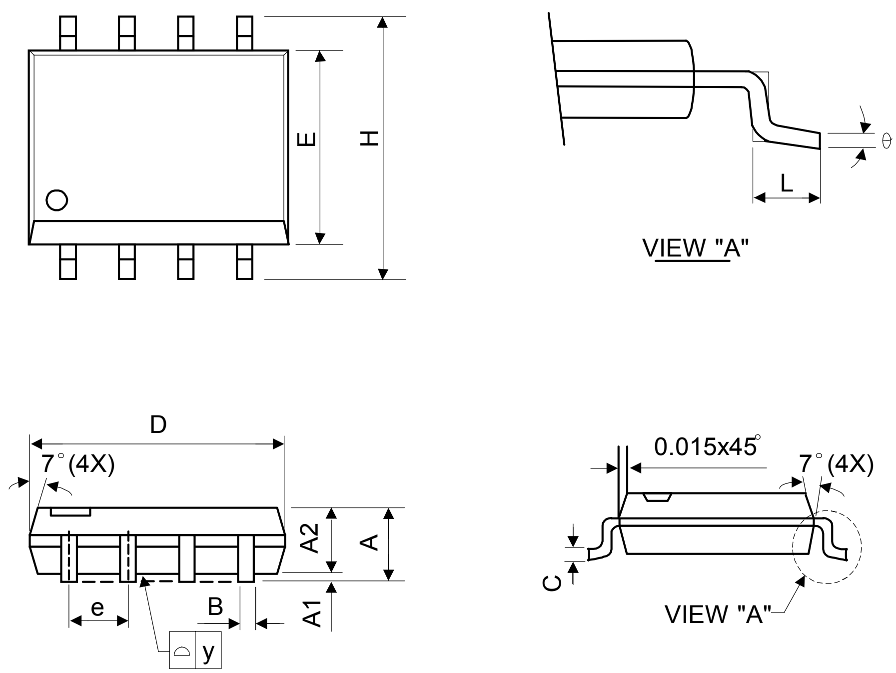
■ Package Dimension

(1) PDIP-8L



Symbol	Dimensions in millimeters			Dimensions in inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.33	-	-	0.210
A1	0.38	-	-	0.015	-	-
A2	3.1	3.30	3.5	0.122	0.130	0.138
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.4	1.52	1.65	0.055	0.060	0.065
B2	0.81	0.99	1.14	0.032	0.039	0.045
C	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	9.53	0.355	0.365	0.375
E	7.62	7.94	8.26	0.300	0.313	0.325
E1	6.15	6.35	6.55	0.242	0.250	0.258
e	-	2.54	-	-	0.100	-
L	2.92	3.3	3.81	0.115	0.130	0.150
eB	8.38	8.89	9.40	0.330	0.350	0.370
S	0.71	0.84	0.97	0.028	0.033	0.038

(2) SOP-8L



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.40	1.60	1.75	0.055	0.063	0.069
A1	0.10	-	0.25	0.040	-	0.100
A2	1.30	1.45	1.50	0.051	0.057	0.059
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.010
D	4.80	5.05	5.30	0.189	0.199	0.209
E	3.70	3.90	4.10	0.146	0.154	0.161
e	-	1.27	-	-	0.050	-
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
y	-	-	0.10	-	-	0.004
θ	0^{o}	-	8^{o}	0^{o}	-	8^{o}

■ Design Formula Table

Calculation	Step-Up	Step-Down	Voltage-Inverting
t_{on}/t_{off}	$\dfrac{V_{out}+V_F-V_{in(min)}}{V_{in(min)}-V_{sat}}$	$\dfrac{V_{out}+V_F}{V_{in(min)}-V_{sat}-V_{out}}$	$\dfrac{\lvert V_{out}\rvert+V_F}{V_{in}-V_{sat}}$
$(t_{on}+t_{off})$	$1/f$	$1/f$	$1/f$
t_{off}	$\dfrac{t_{on}+t_{off}}{\dfrac{t_{on}}{t_{off}}+1}$	$\dfrac{t_{on}+t_{off}}{\dfrac{t_{on}}{t_{off}}+1}$	$\dfrac{t_{on}+t_{off}}{\dfrac{t_{on}}{t_{off}}+1}$
t_{on}	$(t_{on}+t_{off})-t_{off}$	$(t_{on}+t_{off})-t_{off}$	$(t_{on}+t_{off})-t_{off}$
C_T	$4.0\times10^{-5}t_{on}$	$4.0\times10^{-5}t_{on}$	$4.0\times10^{-5}t_{on}$
$I_{pk}(switch)$	$2I_{out(max)}(t_{on}/t_{off}+1)$	$2I_{out(max)}$	$2I_{out(max)}(t_{on}/t_{off}+1)$
R_{sc}	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$
$L_{(min)}$	$\dfrac{(V_{in(min)}-V_{sat})}{I_{pk(switch)}}t_{on(max)}$	$\dfrac{(V_{in(min)}-V_{sat}-V_{out})}{I_{pk(switch)}}t_{on(max)}$	$\dfrac{(V_{in(min)}-V_{sat})}{I_{pk(switch)}}t_{on(max)}$
C_O	$9\dfrac{I_{out}t_{on}}{V_{ripple(pp)}}$	$\dfrac{I_{pk(switch)}(t_{off}+t_{on})}{8V_{ripple(pp)}}$	$9\dfrac{I_{out}t_{on}}{V_{ripple(pp)}}$

V_{sat} = Saturation voltage of the output switch.
V_F = Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:
V_{in} -Nominal input voltage.
V_{out} -Desired output voltage, $|V_{out}|=1.25(1+R2/R1)$
I_{out} -Desired output current.
f_{min} -Minimum desired output switching frequency at the selected values of V_{in} and I_o.
$V_{ripple(pp)}$ -Desired peak-to-peak output ripple voltage, In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.