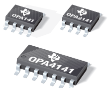
TEXAS INSTRUMENTS



OPA141
OPA2141
OPA4141

Single-Supply, 10MHz, Rail-to-Rail Output, Low-Noise, JFET Amplifier

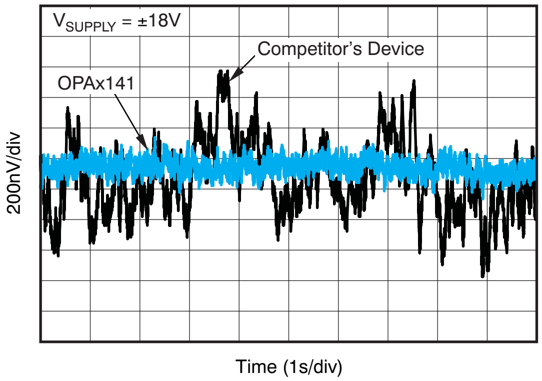
Check for Samples: OPA141, OPA2141, OPA4141

FEATURES

- **Low Supply Current: 2.3mA max**
- **Low Offset Drift: 10µV/°C max**
- **Low Input Bias Current: 20pA max**
- **Very Low 1/f Noise: 250nV_{PP}**
- **Low Noise: 6.5nV/$\sqrt{Hz}$**
- **Wide Bandwidth: 10MHz**
- **Slew Rate: 20V/µs**
- **Input Voltage Range Includes V–**
- **Rail-to-Rail Output**
- **Single-Supply Operation: 4.5V to 36V**
- **Dual-Supply Operation: ±2.25V to ±18V**
- **No Phase Reversal**
- **MSOP-8, TSSOP Packages**

APPLICATIONS

- **Battery-Powered Instruments**
- **Industrial Controls**
- **Medical Instrumentation**
- **Photodiode Amplifiers**
- **Active Filters**
- **Data Acquisition Systems**
- **Portable Audio**
- **Automatic Test Systems**



0.1Hz to 10Hz NOISE

DESCRIPTION

The OPA141, OPA2141, and OPA4141 amplifier family is a series of low-power JFET input amplifiers that feature good drift and low input bias current. The rail-to-rail output swing and input range that includes V– allow designers to take advantage of the low-noise characteristics of JFET amplifiers while also interfacing to modern, single-supply, precision analog-to-digital converters (ADCs) and digital-to-analog converters (DACs).

The OPA141 achieves 10MHz unity-gain bandwidth and 20V/µs slew rate while consuming only 1.8mA (typ) of quiescent current. It runs on a single 4.5 to 36V supply or dual ±2.25V to ±18V supplies.

All versions are fully specified from –40°C to +125°C for use in the most challenging environments. The OPA141 (single) and OPA2141 (dual) versions are available in both MSOP-8 and SO-8 packages; the OPA4141 (quad) is available in the SO-14 and TSSOP-14 packages.

RELATED PRODUCTS

FEATURES	PRODUCT
Precision, Low-Power, 10MHz FET Input Industrial Op Amp	OPA140(1)
2.2nV/$\sqrt{Hz}$, Low-Power, 36V Operational Amplifier in SOT-23 Package	OPA209(1)
Low-Noise, High-Precision, JFET-Input Operational Amplifier	OPA827
Low-Noise, Low I_Q Precision Operational Amplifier	OPA376
High-Speed, FET-Input Operational Amplifier	OPA132

1. Preview product; estimated availability in Q3 2010.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		VALUE	UNIT
Supply Voltage		±20	V
Signal Input Terminals	Voltage(2)	(V–) –0.5 to (V+) +0.5	V
	Current(2)	±10	mA
Output Short-Circuit(3)		Continuous	
Operating Temperature, T_A		–55 to +150	°C
Storage Temperature, T_A		–65 to +150	°C
Junction Temperature, T_J		+150	°C
ESD Ratings	Human Body Model (HBM)	2000	V
	Charged Device Model (CDM)	500	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to $V_S/2$ (ground in symmetrical dual-supply setups), one amplifier per package.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA141	SO-8	D	O141A
	MSOP-8	DGK	141
OPA2141	SO-8	D	O2141A
	MSOP-8	DGK	2141
OPA4141	TSSOP-14	PW	O4141A
	SO-14	D	O4141AG4

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

THERMAL INFORMATION

THERMAL METRIC		OPA141, OPA2141	OPA141, OPA2141	UNITS
		D (SO)	DGK (MSOP)(1)	
		8	8	
θ_{JA}	Junction-to-ambient thermal resistance(2)	160	180	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance(3)	75	55	
θ_{JB}	Junction-to-board thermal resistance(4)	60	130	
ψ_{JT}	Junction-to-top characterization parameter(5)	9	n/a	
ψ_{JB}	Junction-to-board characterization parameter(6)	50	120	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance(7)	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

THERMAL INFORMATION

THERMAL METRIC		OPA4141	OPA4141	UNITS
		D (SO)	PW (TSSOP)(1)	
		14	14	
θ_{JA}	Junction-to-ambient thermal resistance(2)	97	135	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance(3)	56	45	
θ_{JB}	Junction-to-board thermal resistance(4)	53	66	
ψ_{JT}	Junction-to-top characterization parameter(5)	19	n/a	
ψ_{JB}	Junction-to-board characterization parameter(6)	46	60	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance(7)	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
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(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS: V_S = +4.5V to +36V; ±2.25V to ±18V

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C**.
At T_A = +25°C, R_L = 2kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER	CONDITIONS	OPA141, OPA2141, OPA4141			UNIT
		MIN	TYP	MAX	
OFFSET VOLTAGE					
Offset Voltage, RTI V_{OS}	V_S = ±18V		±1	±3.5	mV
Over Temperature	**V_S = ±18V**			**±4.3**	**mV**
Drift dV_{OS}/dT	**V_S = ±18V**		**±2**	**±10**	**μV/°C**
vs Power Supply PSRR	V_S = ±2.25V to ±18V		±0.14	±2	μV/V
Over Temperature	**V_S = ±2.25V to ±18V**			**±4**	**μV/V**
INPUT BIAS CURRENT					
Input Bias Current I_B			±2	±20	pA
Over Temperature				**±5**	**nA**
Input Offset Current I_{OS}			±2	±20	pA
Over Temperature				**±1**	**nA**
NOISE					
Input Voltage Noise					
f = 0.1Hz to 10Hz			250		nV_{PP}
f = 0.1Hz to 10Hz			42		nV_{RMS}
Input Voltage Noise Density e_n					
f = 10Hz			12		nV/√Hz
f = 100Hz			6.5		nV/√Hz
f = 1kHz			6.5		nV/√Hz
Input Current Noise Density i_n					
f = 1kHz			0.8		fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range V_{CM}		**(V–) –0.1**		**(V+)–3.5**	**V**
Common-Mode Rejection Ratio CMRR	V_S = ±18V, V_{CM} = (V–) –0.1V to (V+) – 3.5V	120	126		dB
Over Temperature	**V_S = ±18V, V_{CM} = (V–) –0.1V to (V+) – 3.5V**	**120**			**dB**
INPUT IMPEDANCE					
Differential			10^{13} || 8		Ω || pF
Common-Mode	V_{CM} = (V–) –0.1V to (V+) –3.5V		10^{13} || 6		Ω || pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain A_{OL}	V_O = (V–)+0.35V to (V+)–0.35V, R_L = 2kΩ	114	126		dB
Over Temperature	**V_O = (V–)+0.35V to (V+)–0.35V, R_L = 2kΩ**	**108**			**dB**
FREQUENCY RESPONSE					
Gain Bandwidth Product BW			10		MHz
Slew Rate			20		V/μs
Settling Time, 12-bit (0.024)			880		ns
THD+N	1kHz, G = 1, V_O = $3.5V_{RMS}$		0.00005		%
Overload Recovery Time			600		ns

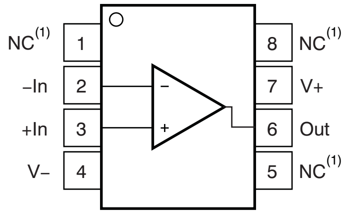
ELECTRICAL CHARACTERISTICS: V_S = +4.5V to +36V; ±2.25V to ±18V (continued)

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C**.
At T_A = +25°C, R_L = 2kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		CONDITIONS	OPA141, OPA2141, OPA4141			UNIT
			MIN	TYP	MAX	
OUTPUT						
Voltage Output	**V_O**	**R_L = 10kΩ**	**(V–)+0.2**		**(V+)–0.2**	**V**
		R_L = 2kΩ	**(V–)+0.35**		**(V+)–0.35**	**V**
Short-Circuit Current	I_{SC}	Source		+36		mA
		Sink		–30		mA
Capacitive Load Drive	C_{LOAD}		See Figure 19 and Figure 20			
Open-Loop Output Impedance	R_O	f = 1MHz, I_O = 0 (See Figure 18)		10		Ω
POWER SUPPLY						
Specified Voltage Range	V_S		±2.25		±18	V
Quiescent Current (per amplifier)	I_Q	I_O = 0mA		1.8	2.3	mA
Over Temperature					**3.1**	**mA**
CHANNEL SEPARATION						
Channel Separation		At dc		0.02		µV/V
		At 100kHz		10		µV/V
TEMPERATURE RANGE						
Specified Range			–40		+125	°C
Operating Range			–55		+150	°C

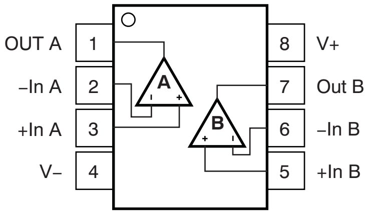
PIN ASSIGNMENTS

OPA141
SO-8, MSOP-8
(TOP VIEW)

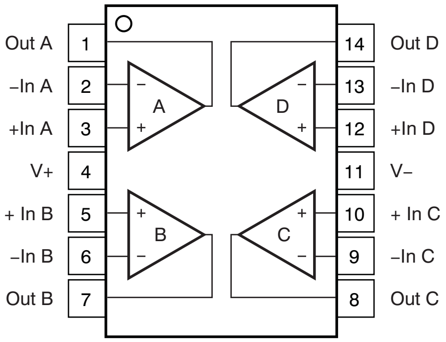


(1) NC denotes no internal connection.

OPA2141
SO-8, MSOP-8
(TOP VIEW)



OPA4141
SO-14, TSSOP-14
(TOP VIEW)



SIMPLIFIED BLOCK DIAGRAM

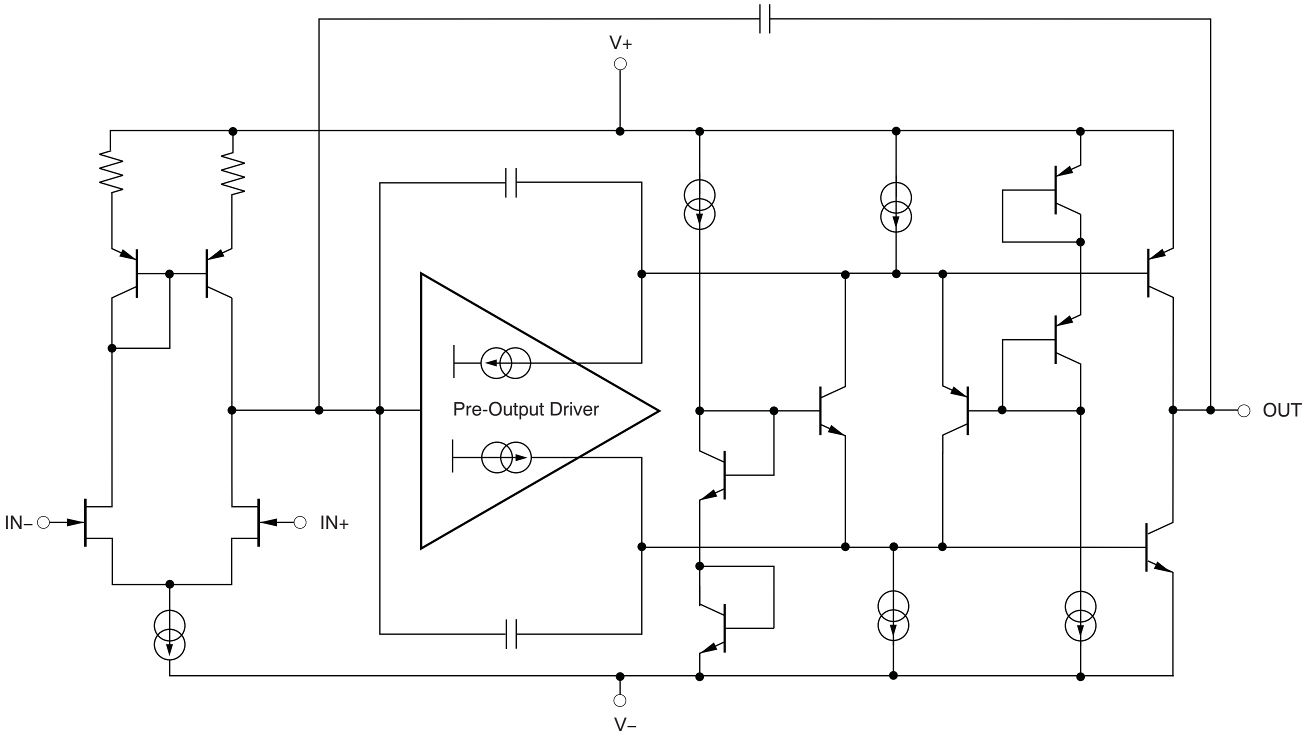


Figure 1.

TYPICAL CHARACTERISTICS SUMMARY

TABLE OF GRAPHS

Table 1. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 2
Offset Voltage Drift Distribution	Figure 3
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Large-Signal Step Response (G = +1)	Figure 26
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Short-Circuit Current vs Temperature	Figure 28
Maximum Output Voltage vs Frequency	Figure 29
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TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = ±18V, R_L = 2kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

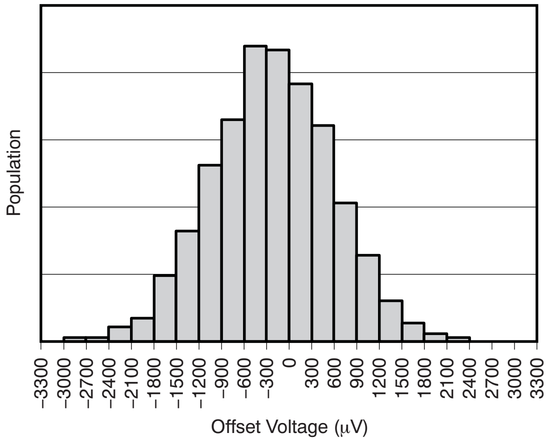


Figure 2.

OFFSET VOLTAGE DRIFT DISTRIBUTION

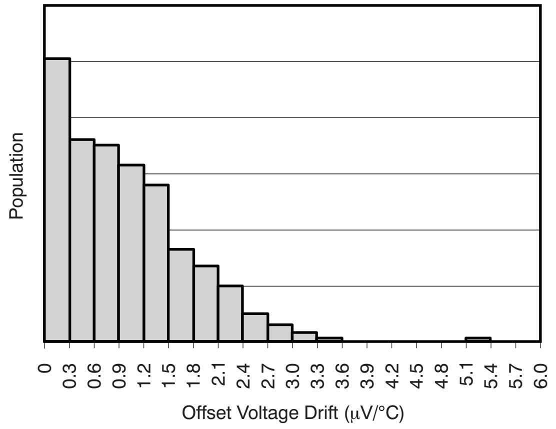


Figure 3.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

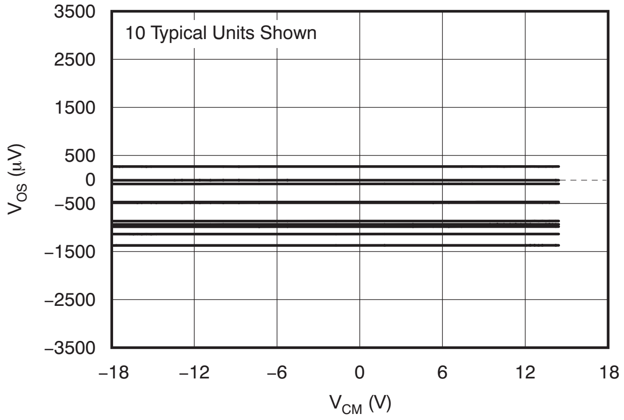


Figure 4.

I_B AND I_{OS} vs COMMON-MODE VOLTAGE

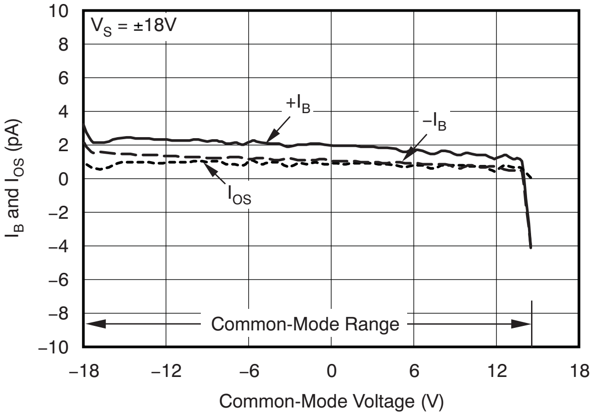


Figure 5.

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT (MAX SUPPLY)

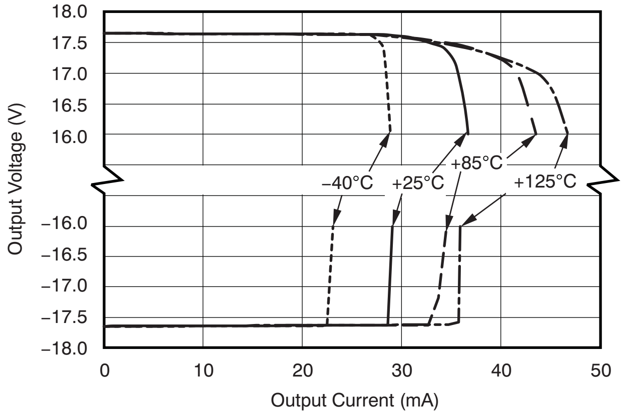


Figure 6.

CMRR AND PSRR vs FREQUENCY (Referred to Input)

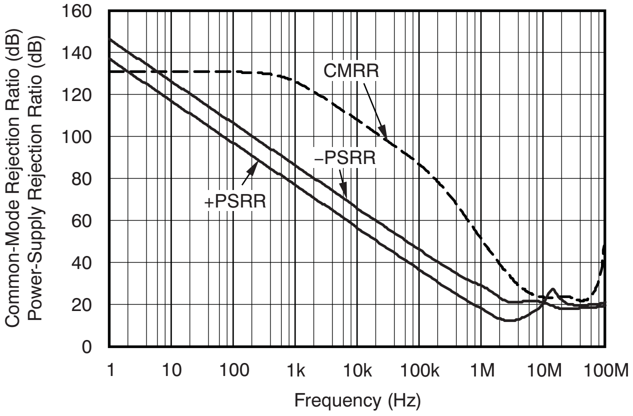


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, R_L = 2kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

COMMON-MODE REJECTION RATIO vs TEMPERATURE

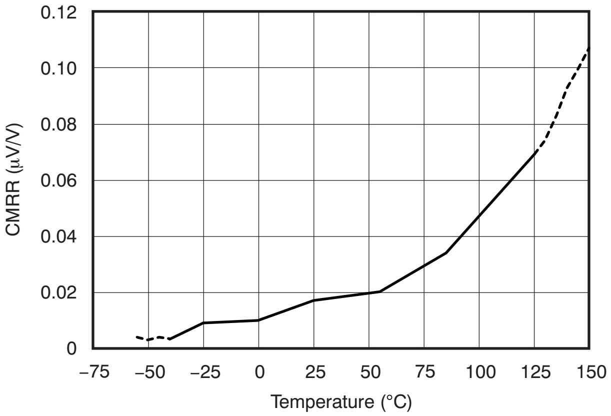


Figure 8.

0.1Hz to 10Hz NOISE

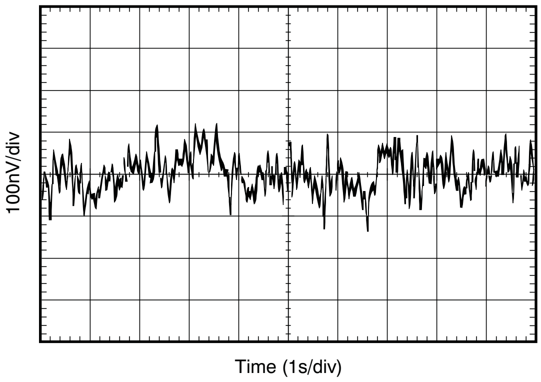


Figure 9.

INPUT VOLTAGE NOISE DENSITY vs FREQUENCY

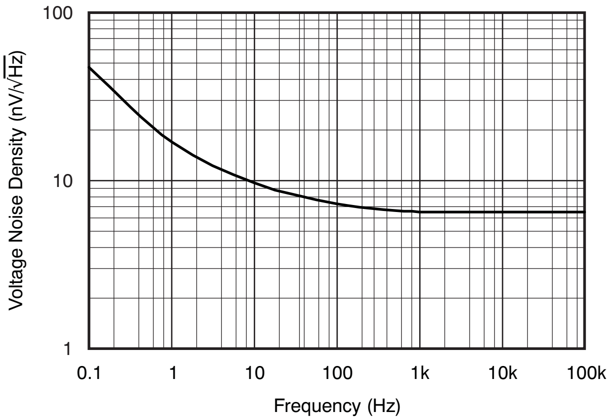


Figure 10.

THD+N RATIO vs FREQUENCY

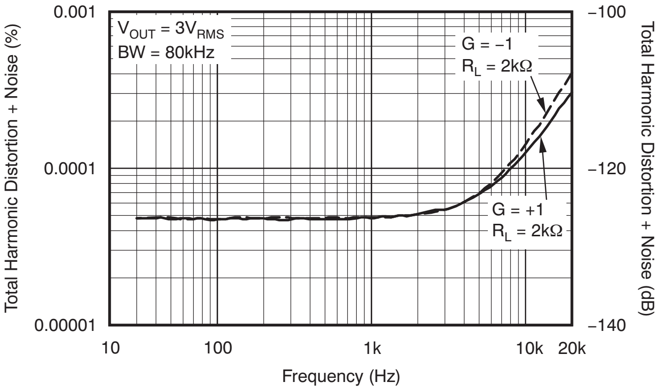


Figure 11.

THD+N RATIO vs OUTPUT AMPLITUDE

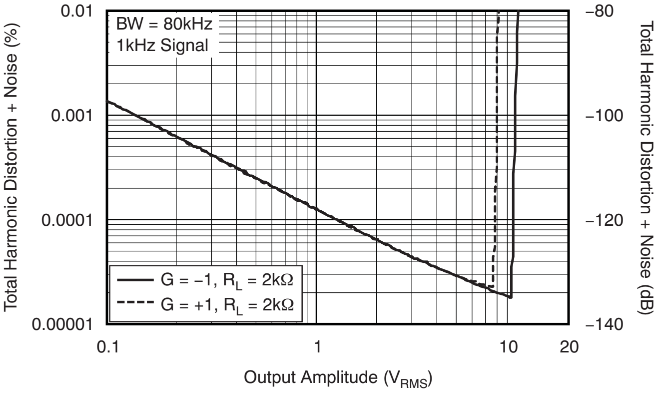


Figure 12.

QUIESCENT CURRENT vs TEMPERATURE

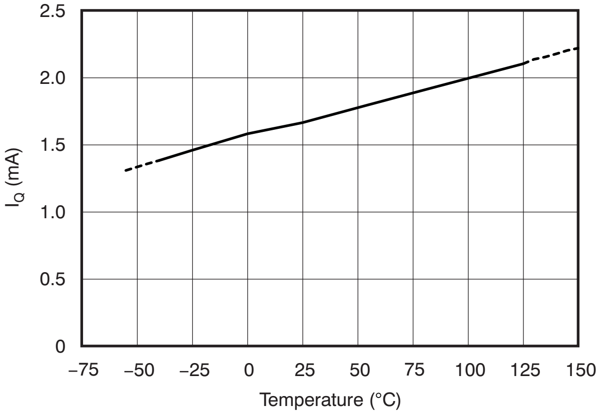


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, R_L = 2kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

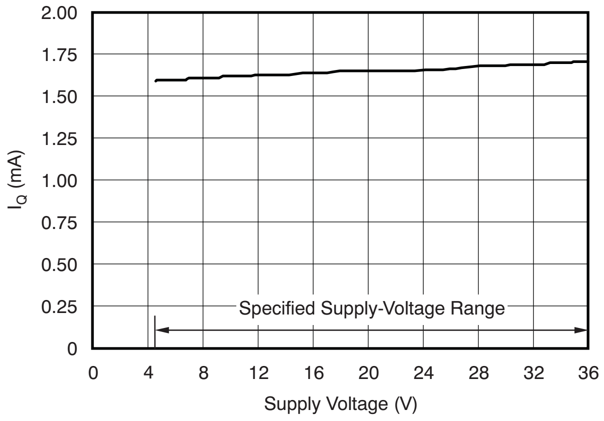


Figure 14.

GAIN AND PHASE vs FREQUENCY

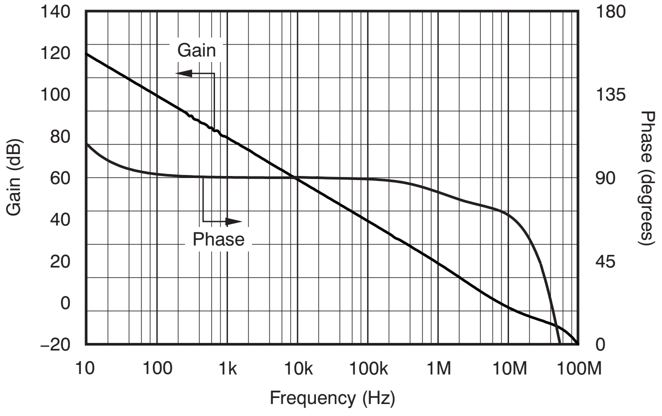


Figure 15.

CLOSED-LOOP GAIN vs FREQUENCY

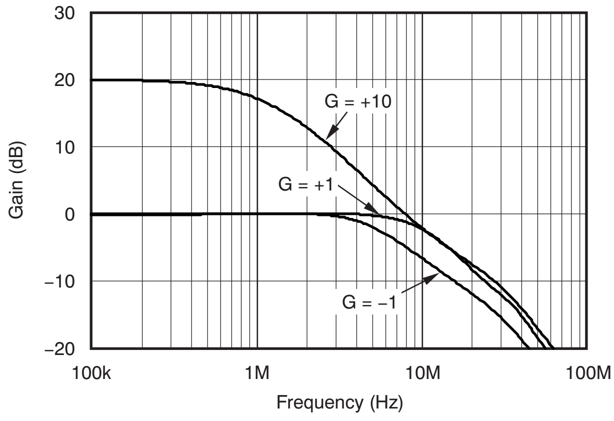


Figure 16.

OPEN-LOOP GAIN vs TEMPERATURE

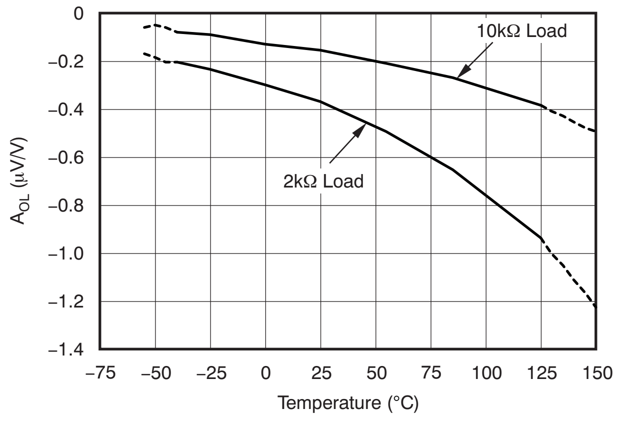


Figure 17.

OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

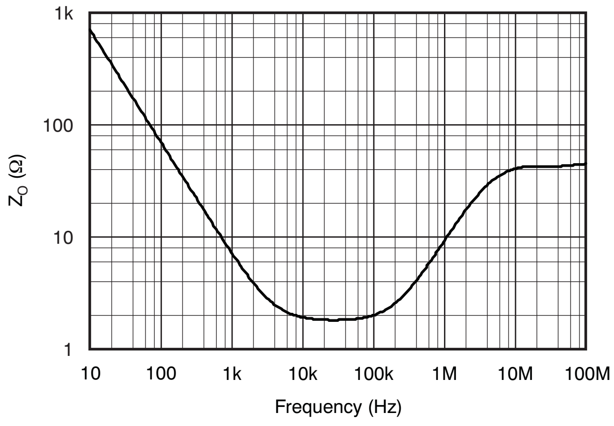


Figure 18.

SMALL-SIGNAL OVERSHOOT
vs CAPACITIVE LOAD (100mV Output Step)

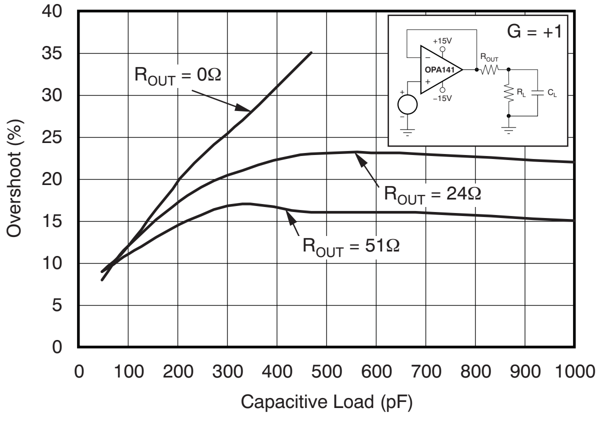


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, R_L = 2kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100mV Output Step)

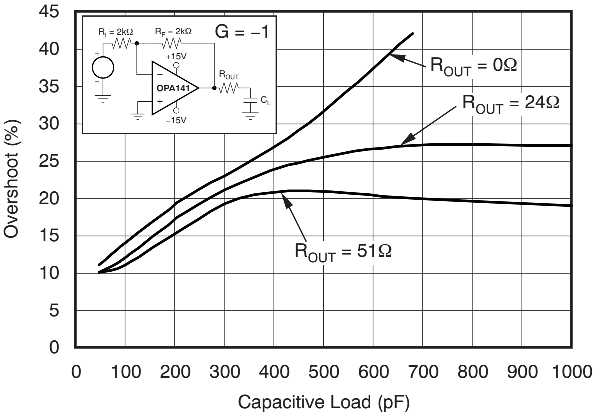


Figure 20.

NO PHASE REVERSAL

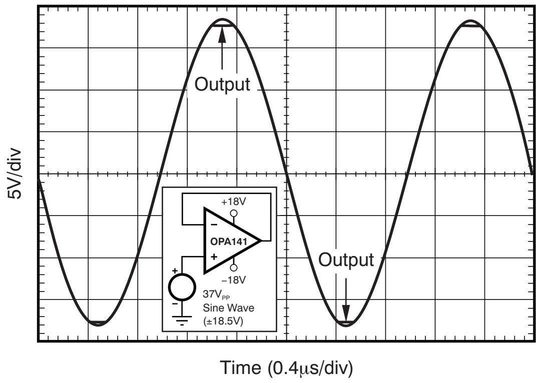


Figure 21.

POSITIVE OVERLOAD RECOVERY

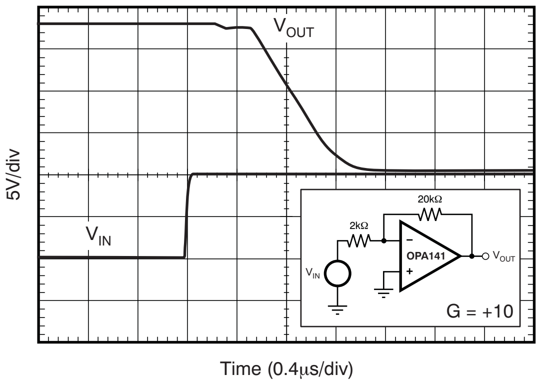


Figure 22.

NEGATIVE OVERLOAD RECOVERY

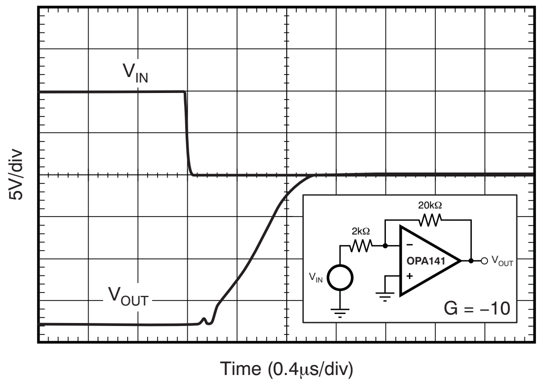


Figure 23.

SMALL-SIGNAL STEP RESPONSE (100mV)

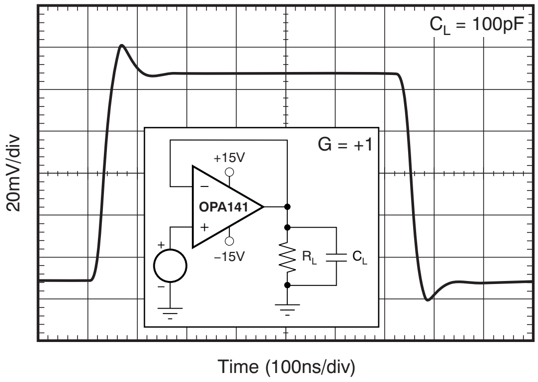


Figure 24.

SMALL-SIGNAL STEP RESPONSE (100mV)

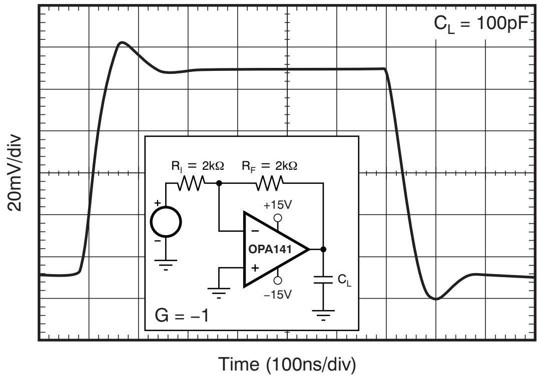


Figure 25.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, R_L = 2kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

LARGE-SIGNAL STEP RESPONSE

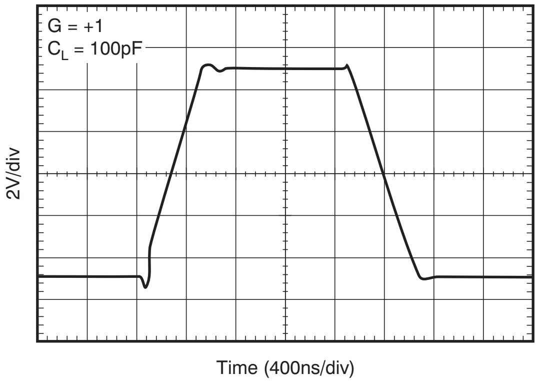


Figure 26.

LARGE-SIGNAL STEP RESPONSE

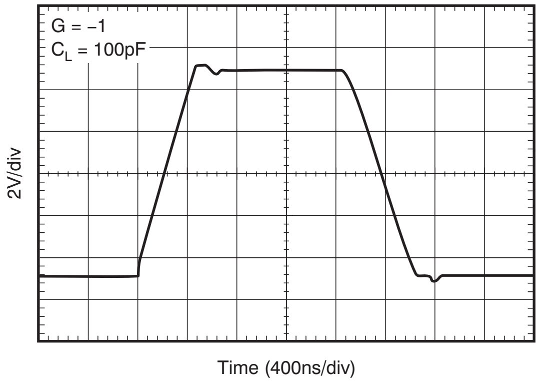


Figure 27.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

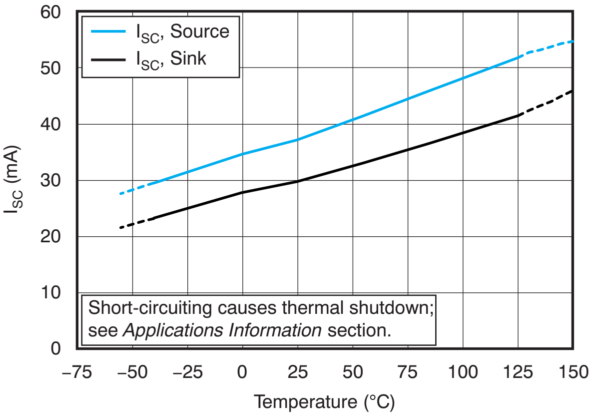


Figure 28.

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

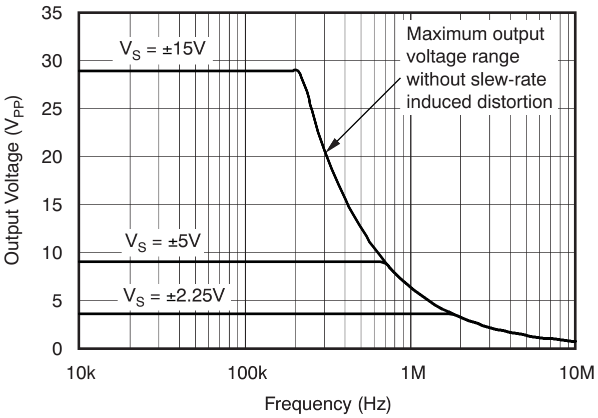


Figure 29.

CHANNEL SEPARATION vs FREQUENCY

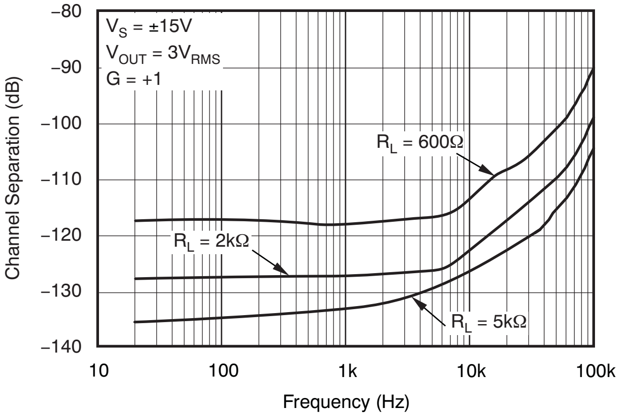


Figure 30.

APPLICATION INFORMATION

The OPA141, OPA2141, and OPA4141 are unity-gain stable, operational amplifiers with very low noise, input bias current, and input offset voltage. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1μF capacitors are adequate. Figure 1 shows a simplified schematic of the OPA141.

OPERATING VOLTAGE

The OPA141, OPA2141, and OPA4141 series of op amps can be used with single or dual supplies from an operating range of V_S = +4.5V (±2.25V) and up to V_S = +36V (±18V). These devices do not require symmetrical supplies; they only require a minimum supply voltage of +4.5V (±2.25V). For V_S less than ±3.5V, the common-mode input range does not include midsupply. Supply voltages higher than +40V can permanently damage the device; see the Absolute Maximum Ratings table. Key parameters are specified over the operating temperature range, T_A = –40°C to +125°C. Key parameters that vary over the supply voltage or temperature range are shown in the Typical Characteristics section of this data sheet.

CAPACITIVE LOAD AND STABILITY

The dynamic characteristics of the OPAx141 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_{OUT} equal to 50Ω, for example) in series with the output.

Figure 19 and Figure 20 illustrate graphs of *Small-Signal Overshoot vs Capacitive Load* for several values of R_{OUT}. Also, refer to Applications Bulletin AB-028 (literature number SBOA015, available for download from the TI web site) for details of analysis techniques and application circuits.

NOISE PERFORMANCE

Figure 31 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (with no feedback resistor network and therefore no additional noise contributions). The OPA141 and OPA211 are shown with total circuit noise calculated. The op amp itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The OPA141, OPA2141, and OPA4141 family has both low voltage noise and extremely low current noise because of the FET input of the op amp. As a result, the current noise contribution of the OPAx141 series is negligible for any practical source impedance, which makes it the better choice for applications with high source impedance.

The equation in Figure 31 shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise
- I_n = current noise
- R_S = source impedance
- k = Boltzmann's constant = 1.38 × 10^{-23} J/K
- T = temperature in degrees Kelvin (K)

For more details on calculating noise, see the section on Basic Noise Calculations.

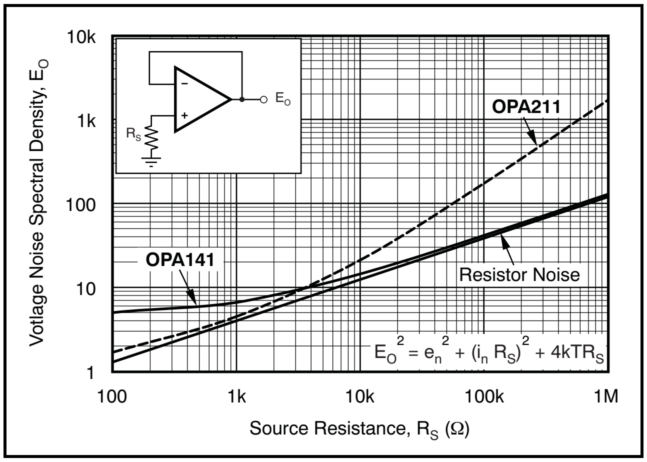


Figure 31. Noise Performance of the OPA141 and OPA211 in Unity-Gain Buffer Configuration

BASIC NOISE CALCULATIONS

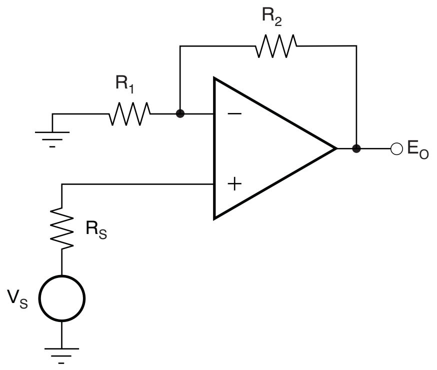
Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 31. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 32 illustrates both noninverting **(A)** and inverting **(B)** op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the extremely low current noise of the OPAx141 means that its current noise contribution can be neglected.

The feedback resistor values can generally be chosen to make these noise sources negligible. Note that low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

A) Noise in Noninverting Gain Configuration

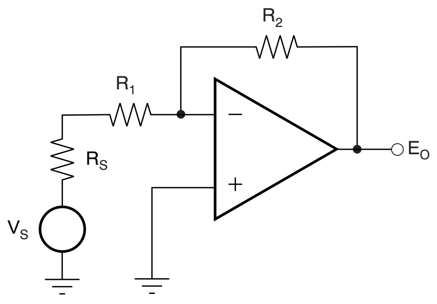


Noise at the output:

$$E_O^2 = \left[1 + \frac{R_2}{R_1}\right]^2 e_n^2 + \left[\frac{R_2}{R_1}\right]^2 e_1^2 + e_2^2 + \left[1 + \frac{R_2}{R_1}\right]^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S
$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1
$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

B) Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left[1 + \frac{R_2}{R_1 + R_S}\right]^2 e_n^2 + \left[\frac{R_2}{R_1 + R_S}\right]^2 e_1^2 + e_2^2 + \left[\frac{R_2}{R_1 + R_S}\right]^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S
$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1
$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPAx141 series of operational amplifiers at 1kHz, $e_n = 6.5\text{nV}/\sqrt{\text{Hz}}$.

Figure 32. Noise Calculation in Gain Configurations

PHASE-REVERSAL PROTECTION

The OPA141, OPA2141, and OPA4141 family has internal phase-reversal protection. Many FET- and bipolar-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input circuitry of the OPA141, OPA2141, and OPA4141 prevents phase reversal with excessive common-mode voltage; instead, the output limits into the appropriate rail (see Figure 21).

OUTPUT CURRENT LIMIT

The output current of the OPAx141 series is limited by internal circuitry to +36mA/–30mA (sourcing/sinking), to protect the device if the output is accidentally shorted. This short-circuit current depends on temperature, as shown in Figure 28.

POWER DISSIPATION AND THERMAL PROTECTION

The OPAx141 series of op amps are capable of driving 2kΩ loads with power-supply voltages of up to ±18V over the specified temperature range. In a single-supply configuration, where the load is connected to the negative supply voltage, the minimum load resistance is 2.8kΩ at a supply voltage of +36V. For lower supply voltages (either single-supply or symmetrical supplies), a lower load resistance may be used, as long as the output current does not exceed 13mA; otherwise, the device short-circuit current protection circuit may activate.

Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA141, OPA2141, and OPA4141 series devices improves heat dissipation compared to conventional materials. Printed circuit board (PCB) layout can also help reduce a possible increase in junction temperature. Wide copper traces help dissipate the heat by acting as an additional heatsink. Temperature rise can be further minimized by soldering the devices directly to the PCB rather than using a socket.

Although the output current is limited by internal protection circuitry, accidental shorting of one or more output channels of a device can result in excessive heating. For instance, when an output is shorted to mid-supply, the typical short-circuit current of 36mA leads to an internal power dissipation of over 600mW at a supply of ±18V.

In the case of a dual OPA2141 in an MSOP-8 package (thermal resistance θ_{JA} = 180°C/W), such power dissipation would lead the die temperature to be 220°C above ambient temperature, when both channels are shorted. This temperature increase significantly decreases the operating life of the device.

In order to prevent excessive heating, the OPAx141 series has an internal thermal shutdown circuit, which shuts down the device if the die temperature exceeds approximately +180°C. Once this thermal shutdown circuit activates, a built-in hysteresis of 15°C ensures that the die temperature must drop to approximately +165°C before the device switches on again.

Additional consideration should be given to the combination of maximum operating voltage, maximum operating temperature, load, and package type. Figure 33 and Figure 34 show several practical considerations when evaluating the OPA2141 (dual version) and the OPA4141 (quad version).

As an example, the OPA4141 has a maximum total quiescent current of 12.4mA (3.1mA/channel) over temperature. The TSSOP-14 package has a typical thermal resistance of 135°C/W. This parameter means that because the junction temperature should not exceed 150°C in order to ensure reliable operation, either the supply voltage must be reduced, or the ambient temperature should remain low enough so that the junction temperature does not exceed 150°C. This condition is illustrated in Figure 33 for various package types. Moreover, resistive loading of the output causes additional power dissipation and thus self-heating, which also must be considered when establishing the maximum supply voltage or operating temperature. To this end, Figure 34 shows the maximum supply voltage versus temperature for a worst-case dc load resistance of 2kΩ.

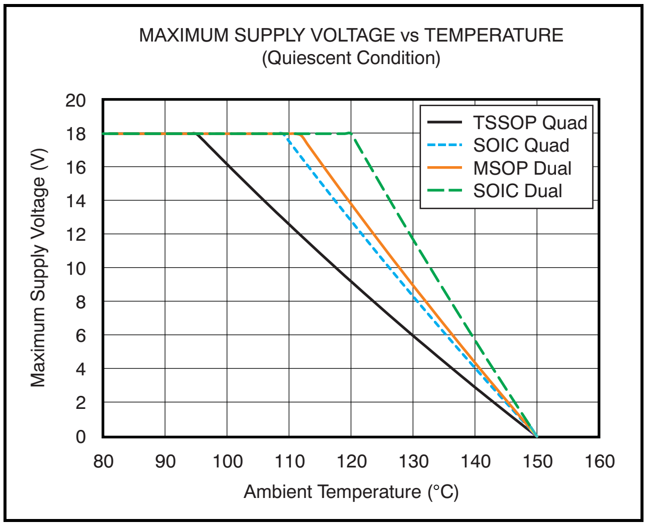


Figure 33. Maximum Supply Voltage vs Temperature (OPA2141 and OPA4141), Quiescent Condition

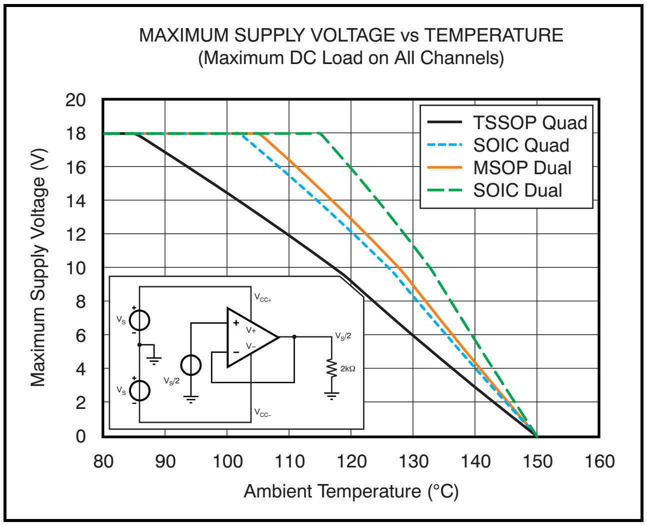


Figure 34. Maximum Supply Voltage vs Temperature (OPA2141 and OPA4141), Maximum DC Load

ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. See Figure 35 for an illustration of the ESD circuits contained in the OPAx141 series (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx141 but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as the one Figure 35 shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Figure 35 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the datasheet specifications recommend that applications limit the input current to 10mA.

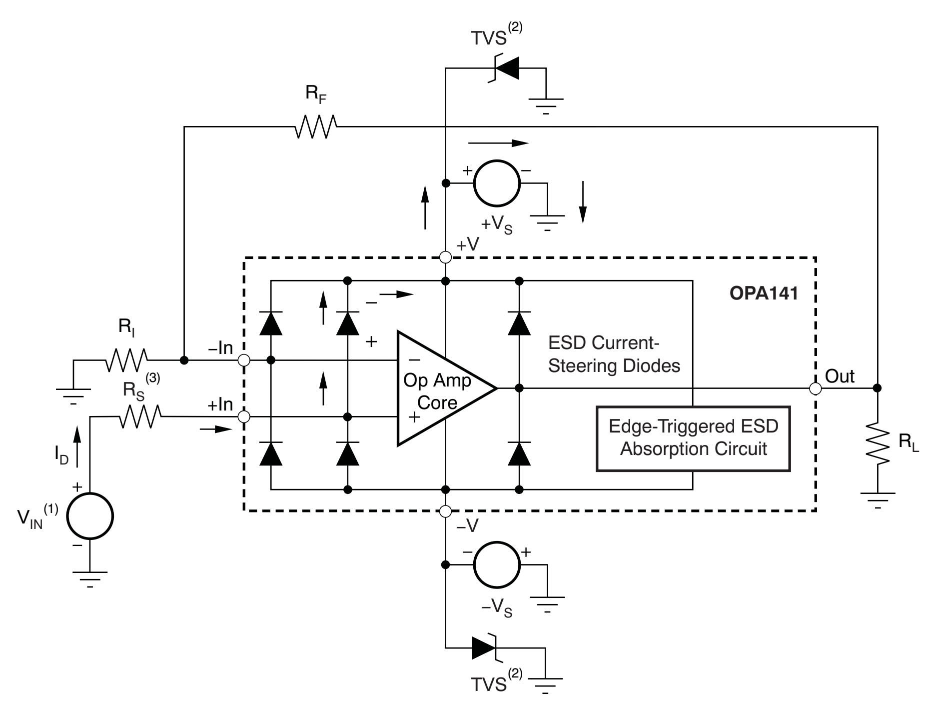
If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $–V_S$ are at 0V.

Again, it depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins as shown in Figure 35. The zener voltage must be selected such that the diode does not turn on during normal operation.

However, its zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



(1) $V_{IN} = +V_S + 500mV$.

(2) TVS: $+V_{S(max)} > V_{TVSBR\ (Min)} > +V_S$

(3) Suggested value approximately 1kΩ.

Figure 35. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
OPA141AID	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI
OPA141AIDGKR	PREVIEW	MSOP	DGK	8	2500	TBD	Call TI	Call TI
OPA141AIDGKT	PREVIEW	MSOP	DGK	8	250	TBD	Call TI	Call TI
OPA141AIDR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI
OPA2141AID	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI
OPA2141AIDGKR	PREVIEW	MSOP	DGK	8	2500	TBD	Call TI	Call TI
OPA2141AIDGKT	PREVIEW	MSOP	DGK	8	250	TBD	Call TI	Call TI
OPA2141AIDR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI
OPA4141AID	PREVIEW	SOIC	D	14	50	TBD	Call TI	Call TI
OPA4141AIDR	PREVIEW	SOIC	D	14	2500	TBD	Call TI	Call TI
OPA4141AIPW	PREVIEW	TSSOP	PW	14	90	TBD	Call TI	Call TI
OPA4141AIPWR	PREVIEW	TSSOP	PW	14	2000	TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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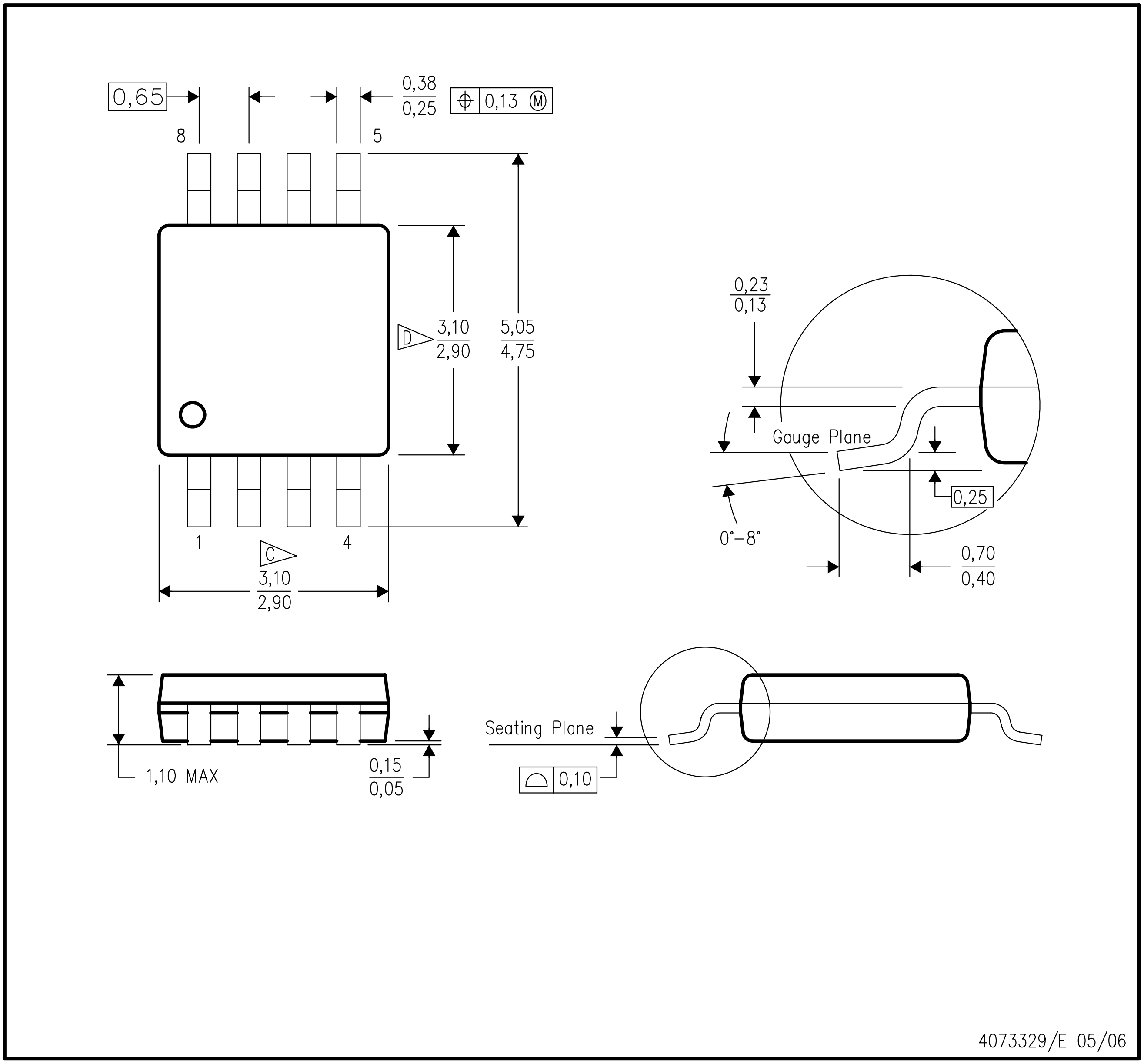
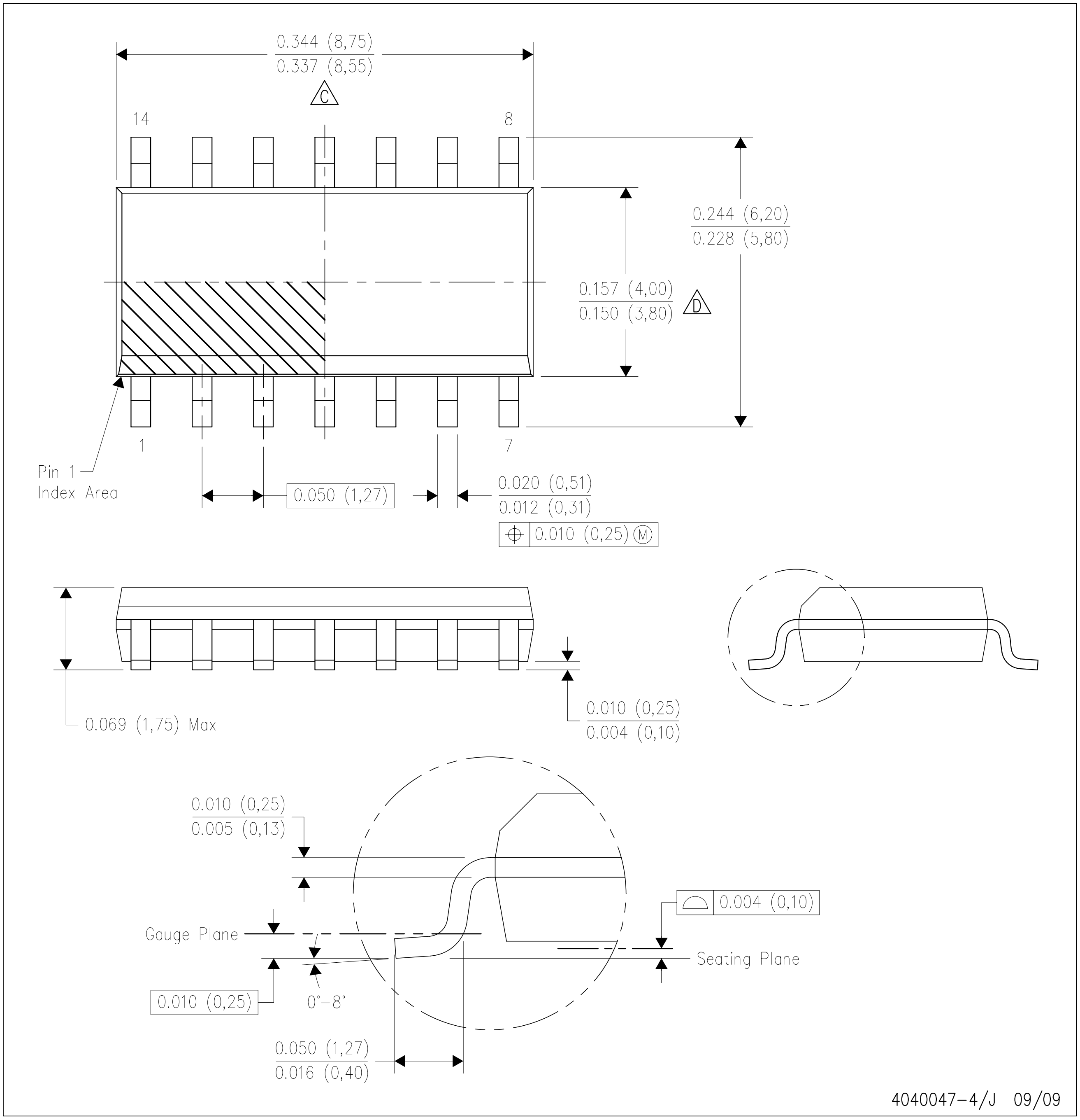
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R-PDSO-G14) PLASTIC SMALL-OUTLINE PACKAGE



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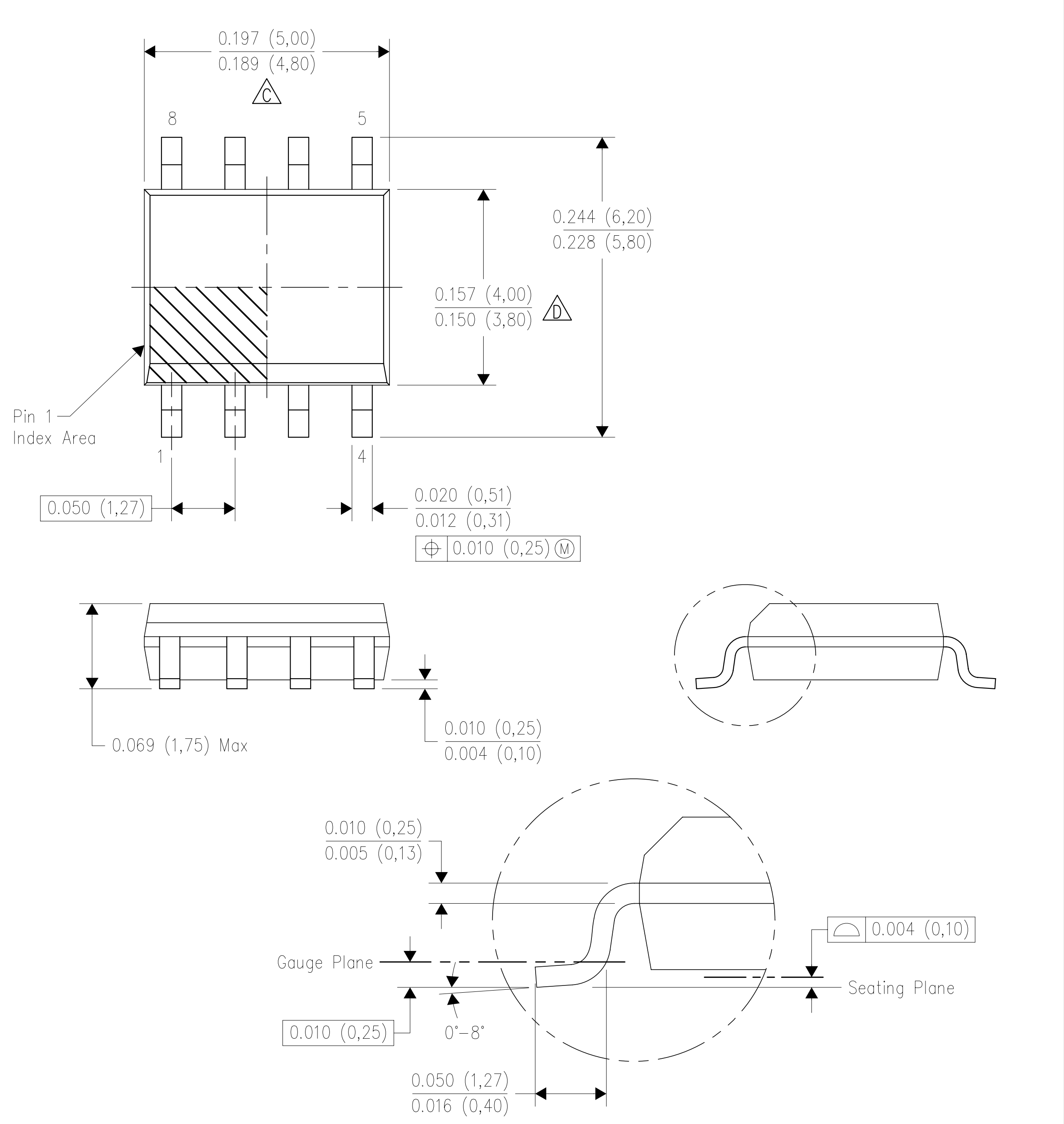
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AB.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE

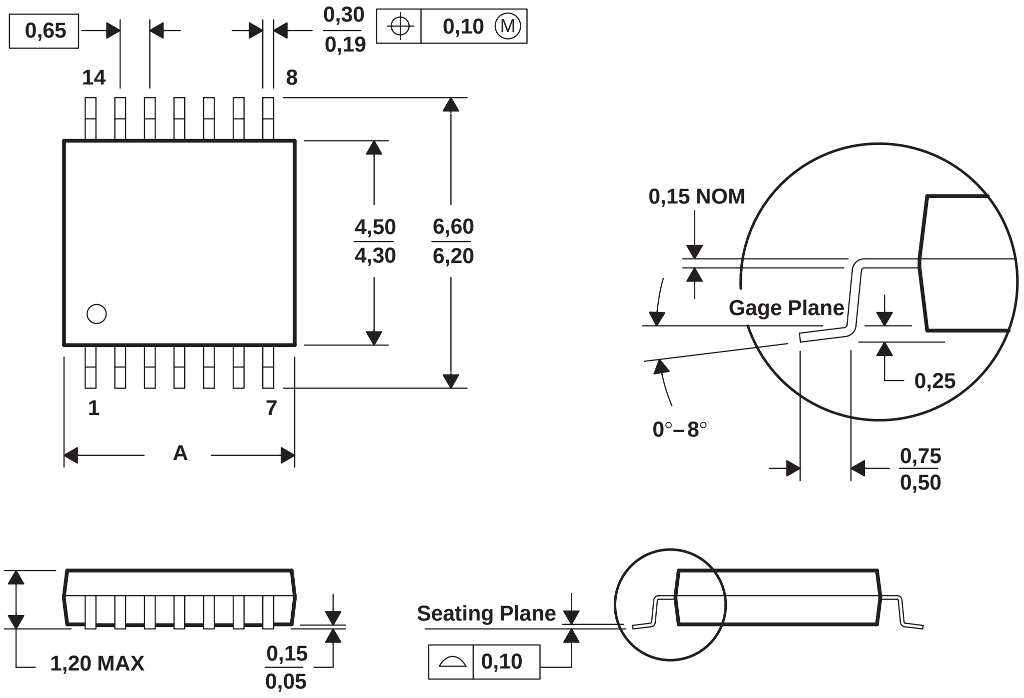


NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS–012 variation AA.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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