Intel® LXT914 Flexible Quad Ethernet Repeater

Datasheet

The Intel® LXT914 Flexible Quad Ethernet Repeater (called hereafter the LXT914 Repeater) is an integrated multi-port repeater designed for mixed-media networks. It provides all the active circuitry required for the repeater function in a single CMOS device. It includes one Attachment Unit Interface (AUI) port and four 10BASE-T transceivers. The AUI port is mode selectable: DTE mode allows connection of an external transceiver (10BASE2, 10BASE5, 10BASE-T or FOIRL) or a drop cable. MAU mode creates a MAU output allowing direct connection to another DTE interface. The 10BASE-T transceivers are entirely self-contained with internal filters which simplify the design work required for FCC-compliant EMI performance.

An inter-repeater backplane interface allows 128 or more 10BASE-T ports to be cascaded together. In addition, a serial port provides information for network management.

The LXT914 Repeater requires only a single 5-volt power supply due to an advanced CMOS fabrication process.

Product Features

- Four integrated 10BASE-T transceivers and one AUI transceiver on a single chip
- Programmable DTE/MAU interface on AUI port
- Seven integrated LED drivers with four unique operational modes
- On-chip transmit and receive filtering
- Automatic partitioning of faulty ports, enabled on an individual port basis
- Automatic polarity detection and correction
- Programmable squelch level allows extended range in low-noise environments
- Synchronous or asynchronous inter-repeater backplane supports “hot swapping”
- Inter-repeater backplane allows cascaded repeaters, linking 128 or more 10BASE-T ports
- Serial port for selecting programmable options
- 68-pin PLCC (Commercial or Extended temp range)
- 100-pin PQFP (Commercial temp range)

Applications

- LAN Repeaters
- Integrated Repeaters
- Switched Repeater Clusters

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Revision History

Date	Revision	Description
31-Oct-2005	003	• Added Section 5.1 and Figure 16 through Figure 19 (RoHS top labels). • Added Section 6.0, "Product Ordering Information" on page 44 with Table 29 "Product Ordering Information" on page 44 and Figure 20 "Ordering Information Matrix – Sample" on page 45.
Feb 2001	002	• Added Layout Requirements section under Application Information. • Modified I/O Electrical Characteristics table: Change Max value under Supply Current from 180 to 240; Add text under Test Conditions: "100 test load, no LEDs"; add table note 3.

1.0 LXT914 Pin Assignments and Signal Descriptions

Figure 1. Block Diagram

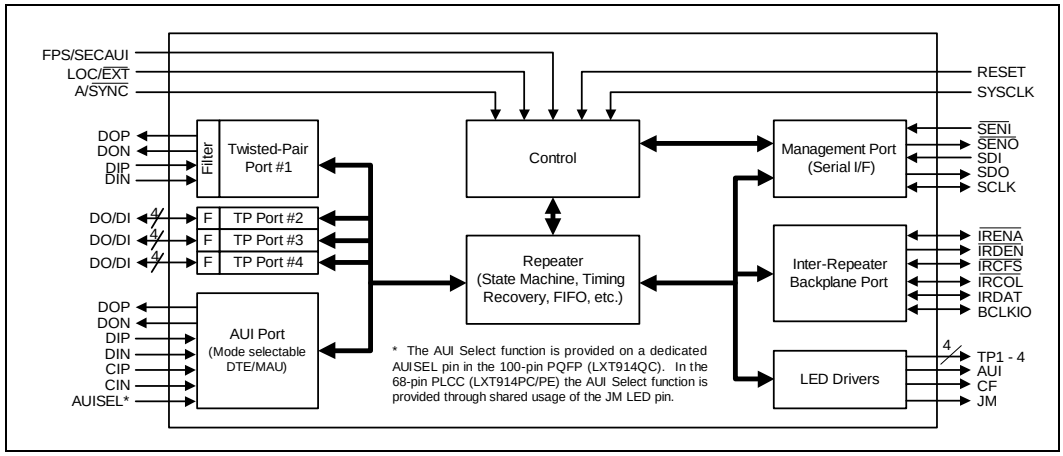


Figure 2. Pin Assignments

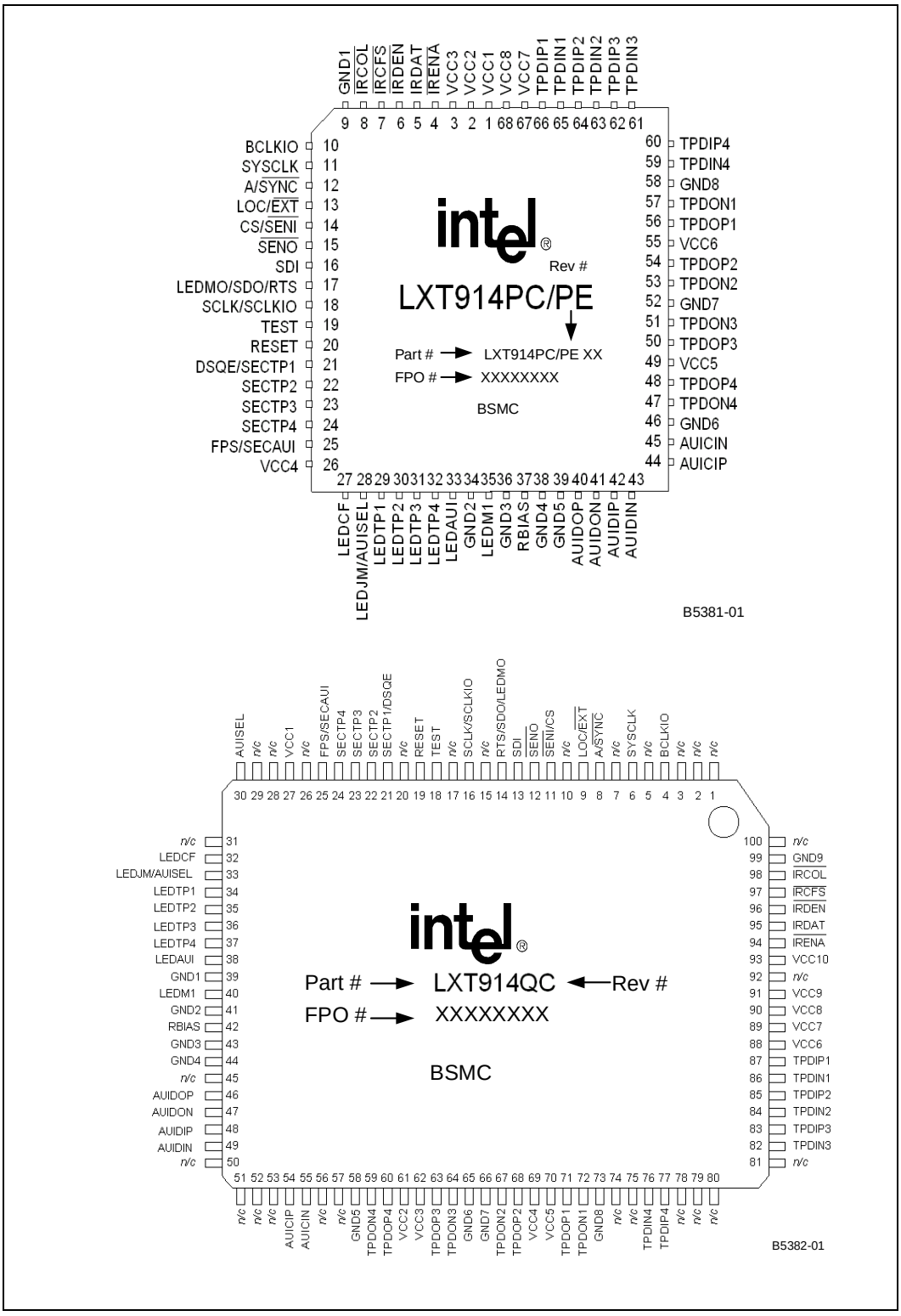


Table 1. Power, Ground, and Clock Signal Descriptions

Pin #		Symbol	I/O	Description
PLCC	PQFP			
1	27	VCC1	—	**Power Supply Inputs.** These pins each require a +5 VDC power supply. The various pins may be supplied from a single power source, but special de-coupling requirements may apply. Each VCC input must be within ±0.3 V of every other VCC input.
2	61	VCC2	—	
3	62	VCC3	—	
26	69	VCC4	—	
49	70	VCC5	—	
55	88	VCC6	—	
67	89	VCC7	—	
68	90	VCC8	—	
—	91	VCC9	—	
—	93	VCC10	—	
9	39	GND1	—	**Ground.** These pins provide ground return paths for the various power supply pins.
34	41	GND2	—	
36	43	GND3	—	
38	44	GND4	—	
39	58	GND5	—	
46	65	GND6	—	
52	66	GND7	—	
58	73	GND8	—	
—	99	GND9	—	
37	42	RBIAS	—	**Bias.** This pin provides bias current for the internal circuitry. The 100 µA bias current is provided through an external 12.4 kΩ resistor to ground.
10	4	BCLKIO	I/O	**Backplane Clock.** This 10 MHz clock synchronizes multiple repeaters on a common backplane. In the synchronous mode, BCLKIO must be supplied to all repeaters from a common external source. In the asynchronous mode, BCLKIO is supplied only when a repeater is outputting data to the bus. Each repeater outputs its internally recovered clock when it takes control of the bus. Other repeaters on the backplane then sync to BCLKIO for the duration of the transmission.
11	6	SYSCLK	I	**System Clock.** The required 20 MHz system clock is input at this pin. Clock must have a 40-60 duty cycle with < 10 ns rise time.

Table 2. Inter-Repeater Backplane Signal Descriptions

PLCC	PQFP	Symbol	I/O	Description
4	94	IRENA	I/O	**Inter-Repeater Backplane Enable.** This pin allows individual LXT914 repeaters to take control of the Inter-Repeater Backplane (IRB) data bus (IRDAT). The IRENA bus must be pulled up locally by a 330 Ω resistor.[1]
5	95	IRDAT	I/O	**IRB Data.** This pin is used to pass data between multiple repeaters on the IRB. The IRDAT bus must be pulled up locally by a 330 Ω resistor.[1]
6	96	IRDEN	O	**IRB Driver Enable.** The IRDEN pin is used to enable external bus drivers which may be required in synchronous systems with large backplanes. This is an active Low signal, maintained for the duration of the data transmission. IRDEN must be pulled up locally by a 330 Ω resistor.
7 8	97 98	IRCFS IRCOL	I/O I/O	**IRB Collision Flag Sense** (IRCFS) and **IRB Collision** (IRCOL). These two pins are used for collision signalling between multiple LXT914 devices on the Inter-Repeater Backplane (IRB). Both the IRCFS bus and the IRCOL bus must be pulled up globally with 330 Ω resistors. (IRCFS requires a precision resistor [±1%].)[2]

NOTES:
1. IRENA and IRDAT can be buffered between boards in multi-board configurations. Where buffering is used, a 330 Ω pull-up resistor can be used on each signal, on each board. Where no buffering is used, the total impedance should be no less than 330 Ω.
2. IRCFS and IRCOL cannot be buffered. In multi-board configurations, the total impedance on IRCOL should be no smaller than 330 Ω. IRCFS should be pulled up only once, by a single 330 Ω, 1% resistor.

Table 3. Mode Select and Control Signal Descriptions

PLCC	PQFP	Symbol	I/O	Description
12	8	A/SYNC	I	**Backplane Sync Mode Select.** This pin selects the backplane sync mode. When this pin is left floating an internal pull-up defaults to the Asynchronous mode (A/SYNC High). In the asynchronous mode 12 or more LXT914s can be connected on the backplane, and an external 10 MHz backplane clock source is not required. When the synchronous mode is selected (A/SYNC tied Low), 32 or more LXT914s can be connected to the backplane and an external 10 MHz backplane clock source is required.
13	9	LOC/EXT	I	**Management Mode Select.** This pin selects the management mode. When this pin is left floating, an internal pull-up defaults to the Local management mode (LOC/EXT High). In the Local mode, setup parameters are downloaded from an EEPROM during initialization. Once initialized with the setup parameters, the repeater functions independently.
28	33	LEDJM/ AUISEL	I/O	**LED Driver or DTE/MAU Select.** At reset, this pin selects the mode of the AUI port. If left floating, an internal pull-down device forces the AUI port to DTE mode. If pulled High with an external resistor, the port changes to a MAU, in which case the functions of the LEDJM pin are disabled and the default LED mode (Refer to Table 7) is not available.
—	30	AUISEL	I	**DTE/MAU Select.** This pin changes the mode of the AUI port independent of the condition at reset. This function is available only in the 100-pin PQFP package.
17 35	14 40	LEDM0 LEDM1	I/O I/O	**LED Mode 0 & 1 Select.** These two pins select one of four possible LED modes of operation. The Functional Description section describes the four modes.

Table 4. Serial Port Signal Descriptions (External Management Mode)

PLCC	PQFP	Symbol	I/O	Description
14	11	$\overline{\text{SENI}}$	I	**Serial Enable Input.** This active Low input is used to access the LXT914 serial interface. To write to the serial input (SDI), an External Management Device (EMD) must drive this pin from High to Low. The input must be asserted Low concurrent with the appearance of data on SDI and remain Low for the duration of the serial input transaction.
15	12	$\overline{\text{SENO}}$	O	**Serial Enable Output.** This active Low output is used to access the serial interface of an EMD. When the LXT914 sends a data stream to the EMD through the serial port (SDO), this output transitions from High to Low and remains Low for the duration of the serial transmission.
16	13	SDI	I	**Serial Data Input.** This pin is the input for the EMD serial interface. Setup and operating parameters are supplied to the LXT914 in a serial data stream through this port when operating in the External Management Mode.
17	14	SDO	I/O	**Serial Data Output.** After each packet transmission or interrupt event, the LXT914 reports status information to the EMD in a serial data stream through this port.
18	16	SCLK	I	**Serial Clock.** This 10 MHz clock synchronizes the serial interface between the LXT914 and the EMD. Both devices must be supplied from the same clock source. In synchronous mode, SCLK and BCLK may be tied together.

Table 5. Serial Port Signal Descriptions (Local Management Mode)

PLCC	PQFP	Symbol	I/O	Description
14	11	CS	O	**Chip Select.** The LXT914 is designed for use with an EEPROM or similar device which may be used to store setup parameters and serially download them to the LXT914 during initialization. In a single-device application or in the first device of a daisy chain application, this pin is an active High Chip Select output used to enable the EEPROM.
		$\overline{\text{SENI}}$	I	**Serial Enable Input.** In subsequent devices of a daisy-chain configuration, a High-to-Low transition on this pin enables the serial input port (SDI). The input must be asserted concurrent with the appearance of data on SDI and remain Low for the duration of the serial input transaction.
15	12	$\overline{\text{SENO}}$	O	**Serial Enable Output.** During initialization, the LXT914 accepts 48 bits of setup data through the SDI port. After the 48th bit, the LXT914 asserts this pin Low. When multiple LXT914 devices are connected in a daisy-chain, this output is tied to the $\overline{\text{SENI}}$ input of the next device in the chain. Thus each device in the chain is serially enabled by the previous device until all the devices have read in their 48 bits of setup data.
16	13	SDI	I	**Setup Data Input.** This pin is the serial input port for the setup parameters (48 bits).This pin should be tied Low if no EEPROM is present.
17	14	RTS	I/O	**Request To Send.** In a single-device application or in the first device of a daisy chain application, this pin outputs a 9-bit, active High sequence. This pin must be tied to the EEPROM DI input to trigger the EEPROM to download its stored data. In subsequent devices this pin is not used.
18	16	SCLKIO	I/O	**Serial Clock.** A 1 MHz clock provided by the first LXT914 in the chain to all subsequent repeaters and the EEPROM. In the Local mode all repeaters have their SCLKIO pins tied together.

Table 6. Miscellaneous Control Signal Descriptions

PLCC	PQFP	Symbol	I/O	Description
19	18	TEST	I	**Test Mode Select.** This pin must be tied Low for normal operation.
20	19	RESET	I	**RESET.** This pin resets the LXT914 circuitry when pulled High for ≥ 1 ms.
21	21	DSQE (Local)	I	**DSQE.** In Local Mode, this pin controls the SQE function. When High, the SQE function of the AUI port is disabled. When Low, SQE is enabled.
		SECTP1 (External)	I	**Security Mode Select (TP Port 1).** In External Mode, this pin enables the security mode for twisted-pair port 1. When pulled High, the LXT914 Jams the port. This pin must be tied Low if external security control is not required.
22 23 24	22 23 24	SECTP2 SECTP3 SECTP4 (External)	I I I	**Security Mode Select (TP Ports 2–4).** In External Mode, these pins enable the security mode for the respective twisted-pair ports (TP1 through TP4). When pulled High, the LXT914 jams the affected port. The SEC pins must be tied Low if external security control is not required.
25	25	FPS (Local)	I	**First Position Select.** In the Local mode this pin identifies the first device in a daisy chain configuration. When tied High (First position), the LXT914 controls the local EEPROM by providing clock and handshaking. When tied Low (Not First), the LXT914 will accept CLK and data in its turn from previous LXT914s in the data chain.
		SECAUI (External)	I	**Security Mode Select (AUI Port).** In the External mode this pin enables the security mode for the AUI port. When pulled High, the LXT914 jams the AUI port. The security feature is available only in External management mode.

Table 7. LED Driver Signal Descriptions

PLCC	PQFP	Symbol	I/O	Description
27	32	LEDCF	O	**Collision & FIFO Error LED Driver.** This tri-state LED driver pin reports collisions and FIFO errors. It pulses Low to report collisions, and pulses High to report FIFO errors. When this pin is connected to the anode of one LED and to the cathode of a second LED, the LXT914 will simultaneously monitor and report both conditions independently.
28	33	LEDJM	O	**Jabber/MJLP & Manchester Code Violation LED Driver.** This tri-state LED driver pin reports jabber and code violations. It pulses Low to report MAU Jabber Lockup Protection (MJLP), and pulses High to report Manchester code violations. When this pin is connected to the anode of one LED and to the cathode of a second LED, the LXT914 will simultaneously monitor and report both conditions independently.
29 30 31 32	34 35 36 37	LEDTP1 LEDTP2 LEDTP3 LEDTP4	O O O O	**Twisted-Pair Port LED Drivers.** These tri-state LED drivers use an alternating pulsed output to report TP port status. Each pin should be tied to a pair of LEDs (to the anode of one LED and the cathode of a second LED). When connected this way, each pin reports five separate conditions (receive, transmit, link integrity, reverse polarity and auto partition).
33	38	LEDAUI	O	**AUI Port LED Driver.** This tri-state LED driver uses an alternating pulsed output to report AUI port status. This pin should be tied to a pair of LEDs (to the anode of one LED and the cathode of a second LED). When connected this way, this pin reports five separate conditions (receive, transmit, receive jabber, receive collision and auto partition.

Table 8. Repeater Port Signal Descriptions

PLCC	PQFP	Symbol	I/O	Description
40 41	46 47	AUIDOP AUIDON	O O	**AUI Data Outputs (Positive and Negative).** These pins are the positive and negative data outputs for the AUI Port. In MAU Mode these pins are connected to the DI pins of the DTE.
42 43	48 49	AUIDIP AUIDIN	I I	**AUI Data Input (Positive and Negative).** These pins are the positive and negative data inputs for the AUI Port. In MAU Mode, these pins are connected to the DO pins of the DTE.
44 45	54 55	AUICIP AUICIN	I/O I/O	**AUI Collision (Positive and Negative).** These pins are the positive and negative Collision inputs for the AUI Port in DTE Mode. In MAU Mode, these pins output a collision indication to the DTE.
56 57 54 53 50 51 48 47	71 72 68 67 63 64 60 59	TPDOP1 TPDON1 TPDOP2 TPDON2 TPDOP3 TPDON3 TPDOP4 TPDON4	O O O O O O O O	**Twisted-Pair Data Outputs (Positive and Negative).** These pins are the positive (TPDOP1-4) and negative (TPDON1-4) outputs to the network from the respective twisted-pair ports.
66 65 64 63 62 61 60 59	87 86 85 84 83 82 77 76	TPDIP1 TPDIN1 TPDIP2 TPDIN2 TPDIP3 TPDIN3 TPDIP4 TPDIN4	I I I I I I I I	**Twisted-Pair Data Inputs (Positive and Negative).** These pins are the positive (TPDIP1-4) and negative (TPDIN1-4) inputs from the network to the respective twisted-pair ports.

2.0 Functional Description

2.1 Introduction

The LXT914 Repeater is an integrated hub repeater for 10BASE-T networks. The hub repeater is the central point for information transfer across the network. The LXT914 Repeater offers multiple operating modes to suit a broad range of applications ranging from simple 4-port stand-alone hubs or attachments for print and file servers, up to intelligent 128-port enterprise systems with microprocessor/gate arLXT914 Repeater ray management.

The main functions of the LXT914 Repeater hub repeater are data recovery and re-transmission and collision propagation. Data packets received at the AUI or 10BASE-T ports are detected and recovered by the port receivers before being passed to the repeater core circuitry for re-timing and re-transmission. Data packets received through the IRB port are essentially passed directly to the core for retransmission. After recovery of a valid data packet, the repeater broadcasts it to all enabled stations, except the originator station.

2.2 External Interfaces

The LXT914 Repeater includes four 10BASE-T ports with internal filters. The LXT914 Repeater also includes an Attachment Unit Interface (AUI) port, a serial port and an Inter-Repeater Backplane (IRB) port. The serial port allows an external device such as an EEPROM to download setup parameters to the repeater. In more complex designs the serial port can also be used to monitor repeater status. The IRB port enables multiple LXT914 Repeater devices to be cascaded, creating a large, multi-port repeater.

2.2.1 10BASE-T Ports

The four 10BASE-T transceiver ports are completely self-contained. Since the transmitters and receivers include the required filtering, only simple, inexpensive transformers are required to complete the 10BASE-T interface. Each individual Twisted-Pair (TP) port is implemented in accordance with the IEEE 802.3 10BASE-T standard.

2.2.2 AUI Port

The AUI port mode is selectable (DTE mode or MAU mode). With DTE mode selected, the AUI port allows connection of an external transceiver (10BASE2, 10BASE5, 10BASE-T or FOIRL) or a drop cable. With MAU mode selected, the AUI port establishes a MAU output allowing direct connection to another DTE interface.

2.2.3 Serial Port

The serial port provides the management interface to the LXT914 Repeater. Refer to Test Specifications for serial port timing. The serial port can be either unidirectional or bidirectional, depending on the management mode selected. In the Local management mode the serial port is

unidirectional (input only), and is used only to download setup parameters during initialization. The Local mode is intended for use with a simple EEPROM, but the serial port may be tied Low if an EEPROM is not required.

In the External management mode, the serial port is bi-directional (input for setup parameters, output for status reports). The External mode is intended for use with an External Management Device (EMD) and a Media Access Controller (MAC). The EMD (typically a gate array) communicates with a microprocessor (e.g., Intel 8051) and can control up to three LXT914 Repeaters. This simplifies design of a relatively standard 12-port repeater on a single printed circuit board.

2.2.4 Inter-Repeater Backplane

The Inter-Repeater Backplane (IRB) allows several LXT914 Repeaters to function as a single repeater. Refer to Test Specifications for IRB timing. The IRB also allows several multi-repeater boards to be integrated in a standard rack and to function as a single unit. The IRB supports “hot swapping” for easy maintenance and troubleshooting. Each individual repeater distributes recovered and re-timed data to other repeaters on the IRB for broadcast on all ports simultaneously. This simultaneous rebroadcast allows the multi-repeater system to act as a single large repeater unit. The maximum number of repeaters on the IRB is limited by bus loading factors such as parasitic capacitance. The IRB can be operated synchronously or asynchronously.

2.2.4.1 Synchronous IRB Operation

In the synchronous mode, a common external source provides the 10 MHz backplane clock (BCLKIO) and the 20 MHz system clock (SYSCLK) to all repeaters. BCLKIO must be synchronous to SYSCLK and may be derived from SYSCLK using a divide-by-two circuit. In the synchronous mode 32 or more LXT914 Repeaters may be connected on the IRB, providing 128 10BASE-T ports and 32 AUI ports.

2.2.4.2 Asynchronous IRB Operation

In the asynchronous mode an external BCLKIO source is not required. The repeaters run independently until one takes control of the IRB. The transmitting repeater then outputs its own 10 MHz clock onto the BCLKIO line. All other repeaters sync to that clock for the duration of the transmission. In the asynchronous mode 12 or more LXT914 Repeater may be connected to the IRB, providing 48 10BASE-T ports and 12 AUI ports.

The maximum number of repeaters which may be linked on the backplane is limited by board design factors. The numbers listed above are engineering estimates only. Stronger drivers and reduced capacitive loading in PCB layout may allow an increased device count.

2.3 Internal Repeater Circuitry

The basic repeater circuitry is shared among all the ports within the LXT914 Repeater. It consists of a global repeater state machine, several timers and counters and the timing recovery circuit. The timing recovery circuit includes a FIFO for re-timing and recovery of the clock which is used to clock the receive data out onto the IRB.

The shared functional blocks of the LXT914 Repeater are controlled by the global state machine (Figure 3). This diagram and all associated notations used are in strict accordance with section 9.6 of the IEEE 802.3 standard.

The LXT914 Repeater also implements the Partition State Diagram as defined by the IEEE 802.3 standard and shown in Figure 4. The value of CCLimit as implemented in the LXT914 Repeater is 64.

The CCLimit value sets the number of consecutive collisions that must occur before the port is subjected to automatic partitioning. Auto-partition/re-connection is also supported by the LXT914 Repeater with Tw5 conforming to the standard requirement of 450 to 560 bit times.

2.4 Initialization

The following description applies to the initial power-on reset and to any subsequent hardware reset. When a reset occurs (RESET pin pulled High for > 1 ms), the device senses the levels at the various control pins (see Figure 3) to determine the correct operating modes for Management, LEDs, and the AUI port functions.

2.4.1 Local Management Mode Initialization

An internal pull-up causes the LXT914 Repeater to default to the Local management mode unless the LOC/EXT pin is tied Low. In the Local mode the serial port is a unidirectional interface used only to download setup parameters from an external device.

In a Locally managed multiple-repeater (daisy chain) configuration, the first repeater in the chain performs special functions. The First Position Select (FPS) pin is used to establish position (FPS High = First, FPS Low = Not First). After establishing the Hardware mode, each LXT914 Repeater monitors the FPS pin to determine its position.

If FPS is High (First Position), the repeater performs the following functions:

Outputs a 1 MHz Serial Clock (SCLK). SCLK is derived from the 20 MHz SYSCLK input in ASYNC mode and from BCLKIO in SYNC mode; it is supplied to the SCLK inputs of all other repeaters on the bus and to the EEPROM.

Asserts Chip Select (CS) High to enable the EEPROM.

Outputs a serial 9-bit request-to-send (RTS) strobe. The programmable device responds to the RTS strobe with a serial data stream containing the setup parameters for all repeaters in the chain.

Clocks the first 48 serial data input (SDI) bits from the EEPROM into its setup register. Refer to Table 9 and Table 10 for Setup Register bit assignments.

Asserts Serial Enable Output (SENO) Low to enable the next repeater in line.

The second repeater has FPS tied Low and Serial Enable Input (SENI) connected to the Serial Enable Output (SENO) of the first repeater. When enabled by a Low on SENI, each repeater downloads its portion of the stream, then stops accepting data and asserts SENO Low. The SENO pin is linked to the SENI input of the next repeater. This enables the next repeater to clock in its 48-bit word and so on.

If FPS is Low (Not First Position), the repeater performs the following functions:

1. Syncs to the 1 MHz Serial Clock (SCLK) input. SCLK is supplied by the First Position repeater.
2. Responds to SENI Low by enabling the SDI port.
3. Clocks 48 bits from the EEPROM into its setup register through the SDI port.
4. Asserts SENO Low to enable the next repeater in line.

Figure 3. Global State Machine

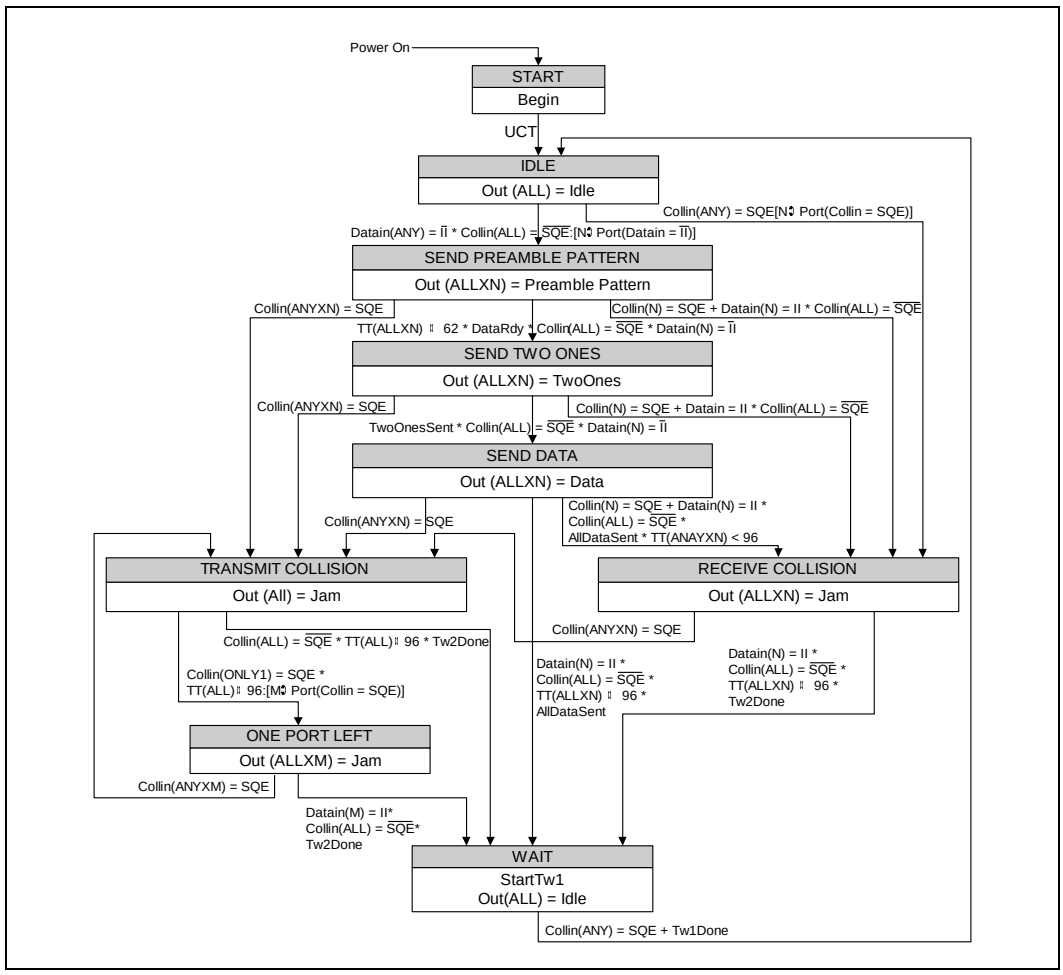


Figure 4. Partitioning State Machine

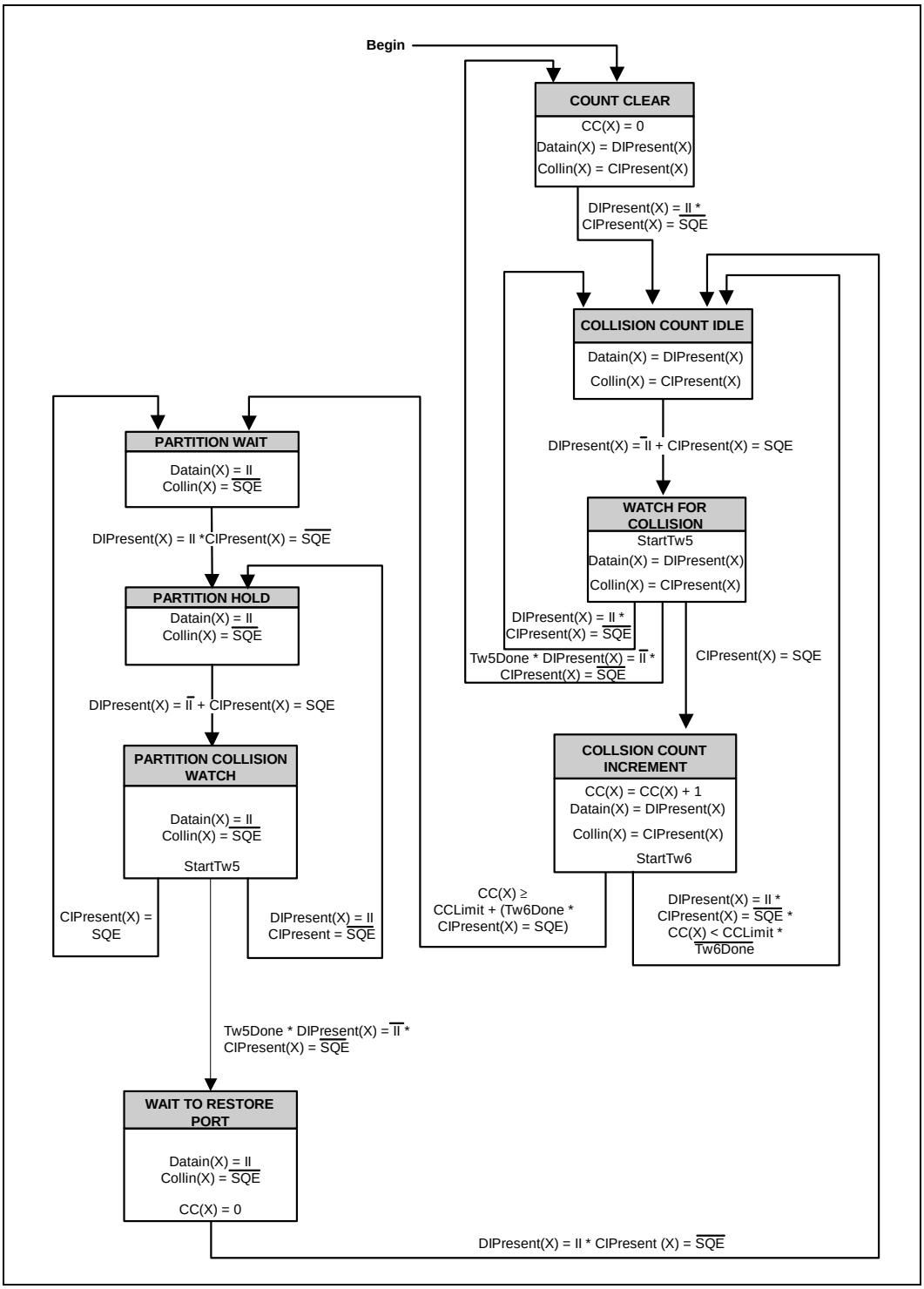


Table 9. Setup Register Bit Assignments

Register	D7	D6	D5	D4	D3	D2	D1	D0
SR(0)	DISLI3	DISLI2	DISLI1	DISAP4	DISAP3	DISAP2	DISAP1	DISAPA
SR(1)	DISTX2	DISTX1	DISTXA	DPRC4	DPRC3	DPRC2	DPRC1	DISLI4
SR(2)	ERSQ1	DISRX4	DISRX3	DISRX2	DISRX1	DISRXA	DISTX4	DISTX3
SR(3)	DFIFOE	DPFRM	DSQE	DMCV	ERXJAB	ERSQ4	ERSQ3	ERSQ2
SR(4)	RES	RES	RES	RES	RES	RES	RES	RES
SR(5)	RES	RES	RES	RES	RES	RES	RES	RES

Table 10. Setup Register Bit Definitions

Bit	Definition
DISAP*x*	1 = Disable Auto-Partitioning on Port *x*
DISLI*x*	1 = Disable Link Integrity on Port *x* (Twisted-pair ports only)
DPRC*x*	1 = Disable Polarity Reverse detection and Correction on Port *x* (Twisted-pair ports only)
DISTX*x*	1 = Disable Transmit on Port *x*
DISRX*x*	1 = Disable Receive on Port *x*
ERSQ*x*	1 = Enable Reduced Squelch on Port *x* (Twisted-pair ports only)
ERXJAB	1 = Enable Receive JAB (Long Packet) (Global)
DMCV	1 = Disable entering Tx Collision state on reception of Manchester Code Violation
DSQE	1 = Disable Signal Quality Error to provide heartbeat (AUI port only)
DPFRM	1 = Disable End-of-Frame checking for polarity correction (Global)
DFIFOE	1 = Disable entering Tx Collision state on FIFO over/underflow condition (Global)
DMJLP	1 = Disable MJLP counter (Global)
RES	*Reserved. Must be set to 0.*

2.4.2 External Management Mode Initialization

The LXT914 Repeater operates in the External management mode when the LOC/$\overline{\text{EXT}}$ pin is tied Low. In the External mode, the serial port is a bidirectional interface between the LXT914 Repeater and an external management device (EMD). The serial port is used to download initial setup parameters to the repeater and to monitor status reports from the repeater. The LXT914 Repeater setup parameters can be changed at any time by the EMD. The initialization process for each repeater in a managed mode configuration is the same, regardless of its position; each repeater is connected directly to the EMD. Each LXT914 Repeater initializes as follows:

1. Syncs to the 10 MHz Serial Clock (SCLK) input. SCLK must be supplied from an external source.
2. Responds to $\overline{\text{SENI}}$ Low by enabling the SDI port.
3. Clocks 48 bits from the EMD into its setup register through the SDI port.
4. Once initialized, the LXT914 Repeater reports its status in a 48-bit serial stream after every packet transmission or interrupt event. Refer to Table 11 and Table 12 for packet status register bit assignments and definitions.

Table 11. Packet Status Register Bit Assignments

Register	D7	D6	D5	D4	D3	D2	D1	D0
PSR(0)	COL2	COL1	COLA	RX4	RX3	RX2	RX1	RXA
PSR(1)	PR2	PR1	LLS4	LLS3	LLS2	LLS1	COL4	COL3
PSR(2)	SPA	AP4	AP3	AP2	AP1	APA	PR4	PR3
PSR(3)	LP3	LP2	LP1	LPA	SP4	SP3	SP2	SP1
PSR(4)	RXJABA	MJLP	LCOL4	LCOL3	LCOL2	LCOL1	LCOLA	LP4
PSR(5)	RES	RXCOL	MANCV	FIFOER	RXJAB4	RXJAB3	RXJAB2	RXJAB1

Table 12. Packet Status Register Bit Definitions

Bit[1]	Definition
RX*x*	Received Packet on Twisted-Pair Port 1-4 or on AUI Port
COL*x*	Transmit Collision of Twisted -Pair Port 1-4 or on AUI Port
LLSC*x*	Link Loss State on Twisted-Pair Port 1-4 or on AUI Port
PR*x*	Polarity reversed on Twisted-Pair Port 1-4 or on AUI Port
AP*x*	Auto-Partition circuit isolated Twisted-Pair Port 1-4 or the AUI Port
SP*x*	Short Packet (less than 74 bits) on Twisted-Pair Port 1-4 or on AUI Port
LP*x*	Long Packet (more than 1.3 ms) on Twisted-Pair Port 1-4 or on AUI Port
LCOL*x*	Late Collision on Twisted-Pair Port 1-4 or on AUI Port
MJLP	MAU Jabber Lockup Protection
RXJAB*x*	Receive Jabber Lockup Protection
FIFOER	FIFO overflow/underflow
MANCV	Manchester Code Violation
RXCOL	Receive Collision on the AUI Port
RES	*Reserved. Not used*

Note:
1. The notation ABCD*x* means bit ABCD associated with port *x*, which can be any of the four Twisted-Pair Ports or the AUI Port.

2.5 10BASE-T Port Operation

2.5.1 10BASE-T Reception

Each LXT914 Repeater 10BASE-T port receiver acquires data packets from its twisted-pair input (TPDIP/TPDIN). An internal RC filter and an intelligent squelch function discriminate noise from link test pulses and valid data streams. The receive function is activated only by valid data streams (above the squelch level and with proper timing). If the differential signal at the DI circuit inputs falls below 75% of the threshold level (unsquelched) for eight bit times (typical), the port receiver enters the idle state.

2.5.1.1 Programmable Internal Squelch Level

The 10BASE-T port receivers have two squelch levels: a normal level or default setting and a reduced level squelch (-4.5 dB) selected when the ERSQx is set in the Setup register. When used with Low noise media such as shielded twisted-pair cabling, the reduced squelch level allows longer loop lengths in the network.

2.5.1.2 Polarity Detection and Correction

The LXT914 Repeater 10BASE-T ports detect and correct for reversed polarity by monitoring link pulses and end-of-frame sequences. A reversed polarity condition is declared when the port receives sixteen or more incorrect link pulses consecutively, or four frames with reversed start-of-idle sequence. In these cases the receiver reverses the polarity of the signal and thereby corrects for this failure condition. If the port enters the link fail state and no valid data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. (If Link Integrity Testing is disabled, polarity detection is based only on received data.)

2.5.2 10BASE-T Transmission

Each LXT914 Repeater 10BASE-T port receives NRZ data from the repeater core and passes it through a Manchester encoder. The encoded data is then transmitted to the twisted-pair network (the DO circuit). The advanced integrated pulse shaping and filtering network produces the pre-distorted and pre-filtered output signal to meet the 10BASE-T jitter template. An internal continuous resistor-capacitor filter is used to remove any high-frequency clocking noise from the pulse shaping circuitry. Integrated filters simplify the design work required for FCC compliant EMI performance. During idle periods, the LXT914 Repeater 10BASE-T ports transmit link integrity test pulses in accordance with the 802.3 10BASE-T standard.

Data packets transmitted by the LXT914 Repeater contain a minimum of 56 preamble bits before the start of frame delimiter (SFD). In the Asynchronous mode, preamble regeneration takes place on the transmit side. In the Synchronous mode, the preamble is regenerated on the receive side and distributed via the IRB. If the total packet is less than 96 bits including the preamble, the LXT914 Repeater extends the packet length to 96 bits by appending a Jam signal (1010...) at the end.

2.5.3 10BASE-T Link Integrity Testing

The LXT914 Repeater fully supports the 10BASE-T Link Integrity test function. The link integrity test determines the status of the receive side twisted-pair cable. Link integrity testing is enabled unless disabled via the DISLIx bit in the Setup register. When enabled, the receiver recognizes link integrity pulses transmitted in the absence of data traffic. With no data packets or link integrity pulses within 100 (±50) ms, the port enters a link fail state and disables its transmitter. The port remains in the link fail state until it detects three or more data packets or link integrity pulses.

2.6 AUI Port Operation

2.6.1 AUI Reception

The LXT914 Repeater AUI port receiver acquires data packets from the network (AUIDIP/AUIDIN). Only valid data streams above the squelch level activate the receive function. If the differential signal at the DI circuit inputs falls below 75% of the threshold level (unsquelched) for 8 bit times (typical), the AUI receiver enters the idle state.

2.6.2 AUI Transmission

The LXT914 Repeater AUI port receives NRZ data from the repeater core, and passes it through a Manchester encoder. The encoded data then goes out on the network (AUIDOP/AUIDON).

2.6.3 AUI Mode Selection (DTE/MAU)

The LXT914 Repeater allows the user to change the mode of the AUI from a DTE to a MAU interface. This option is available on both 68- and 100-pin versions except as follows:

- When using the LEDJM/AUISEL pin to select the AUI interface mode the following is true: After reset the state of the LEDJM/AUISEL pin is sensed for the correct mode. The LEDJM/AUISEL pin when floated or pulled Low will select the DTE interface and the LEDJM/AUISEL output is still available. When the LEDJM/AUISEL pin is pulled High the MAU interface is selected and the LEDJM/AUISEL function is unavailable.
- The 100-pin PQFP has an additional pin, AUISEL (pin 30). When using this pin to select the AUI interface mode the LEDJM/AUISEL pin is still a functional LED driver. The AUISEL pin is not latched after reset and is actively polled to determine which AUI interface mode is to be used. Refer to Table 13.

Table 13. AUI Mode Selection (DTE/MAU)

App #	AUISEL (PQFP only)	LEDJM/ AUISEL (both pkgs)	AUI Mode	Available LED Modes
1	Low	Low	DTE	default, 0-3
2	Low	High	MAU	1-3
3	High	Low	MAU	default, 0-3
4	High	High	MAU	1-3
Note: Application 3 is valid only when using the 100-pin PQFP.				

2.7 Collision Handling

A collision occurs when two or more repeater ports receive simultaneously, or when the AUI CIP/CIN signal is active. The LXT914 Repeater fully complies with the IEEE 802.3 collision specifications, both in individual and multi-repeater applications. In multiple-repeater configurations, collision signaling on the IRB allows all repeaters to share collision parameters, acting as a single large repeater.

$\overline{\text{IRCOL}}$ is a digital open-drain pin. $\overline{\text{IRCFS}}$ is an analog/digital port. The $\overline{\text{IRCOL}}$ and $\overline{\text{IRCFS}}$ lines are pulled up globally (i.e., each signal requires one pull-up resistor for all boards). If there are eight 3-repeater boards in the system, all eight boards share a single pull-up resistor for $\overline{\text{IRCOL}}$ and a single pull-up resistor for $\overline{\text{IRCFS}}$. The global pull-up may be located on one of the boards, or on the backplane. The $\overline{\text{IRCFS}}$ line requires a precision (± 1%) resistor.

The $\overline{\text{IRENA}}$, IRDAT and $\overline{\text{IRDEN}}$ lines are each pulled up locally (one pull-up resistor per board) if external bus drivers are used. If no bus drivers are used then only one global pull-up per signal is used.

2.8 Security Mode

The LXT914 Repeater security mode is fully transparent to the user. In the External management mode, the security feature is available for all four TP ports and the AUI port. In the Local mode, security is available for the TP ports only (the SECAUI input is reassigned as FPS). The security inputs are normally held Low to disable the security feature. Any input can independently be pulled High to scramble the respective port for any given length of time. For applications which do not require security control, the SEC pins must be tied Low.

The security mode pins are real time response inputs. This allows the board designer to screen the destination address with an application specific device and (on match of the destination address) to assert the security input to jam the respective port for the given frame. This real time detection and jam assertion method provides the flexibility to implement customer specific solutions. The destination address decoding and security signal assertion functions can be integrated into the external management device.

2.9 LED Display

The LED display interface consists of seven integrated LED drivers, one for each of the five network ports and two for common functions. Each pin provides a three-state pulsed output (+5 V, high Z, and 0 V) which allows multiple conditions to be monitored and reported independently. Table 14 shows the LED Mode selected with each LEDM1 and LEDM0 combination. Figure 5 shows the LED Driver output conditions, and Table 15 through Table 18 list the repeater states associated with each of the five conditions.

Note: If LED mode 0 is selected and the LEDJM/AUISEL pin is High (which selects MAU Mode), the device defaults to LED Mode 1. LED Mode 0 is not available when LEDJM/AUISEL is pulled High.

Table 14. LED Mode Selection

	LEDM1	LEDM0	LED Mode Selected
PLCC pin	35	17	
PQFP pin	40	14	
	Low	Low	0 Note 1
	Low	High	1
	High	Low	2
	High	High	3

Note:
1. This mode is not available when using the LEDJM/AUISEL pin to select a MAU interface in the AUI port. In this case, the LED Mode defaults to LED Mode 1.

LED Mode 0 (Default) This mode is selected when LEDM1 and LEDM0 are floating or pulled Low. Refer to Table 15. This mode is not available when using the LEDJM/AUISEL pin to select a MAU interface in the AUI port. In this case, the LED Mode defaults to Mode 1.

LED Mode 1 This mode is selected when LEDM1 is floating or pulled Low and LEDM0 is pulled High by a pull-up resistor. Refer to Table 16.

LED Mode 2 This mode is selected when LEDM1 is pulled High by a pull-up resistor and LEDM0 is floating or pulled Low. Refer to Table 17.

LED Mode 3. This mode is selected when LEDM1 is pulled High by a pull-up resistor and LEDM0 is also pulled High by a pull-up resistor. Refer to Table 18.

Table 15. Mode 0 (Default) LED Truth Table

Condition	LEDTP 1–4	LEDAUI	LEDCF	LEDJM
1	Rx Link Pulse	N/A	FIFO Error	Manchester Code Violation
2	Tx Packet	Tx Packet	N/A	N/A
3	Reversed Polarity	N/A	Collision	MAU Jabber Lockup Protection (MJLP)
4	Rx Packet	Rx Packet	N/A	N/A
5	Partitioned Out	Partitioned Out	N/A	N/A

Table 16. Mode 1 LED Truth Table

Condition	LEDTP 1–4	LEDAUI	LEDCF	LEDJM
1	Rx Link Pulse	N/A	MAU Jabber Lockup Protection (MJLP)	N/A
2	N/A	N/A	N/A	N/A
3	N/A	N/A	Collision	N/A
4	Rx Packet	Rx Packet	N/A	N/A
5	N/A	N/A	N/A	N/A

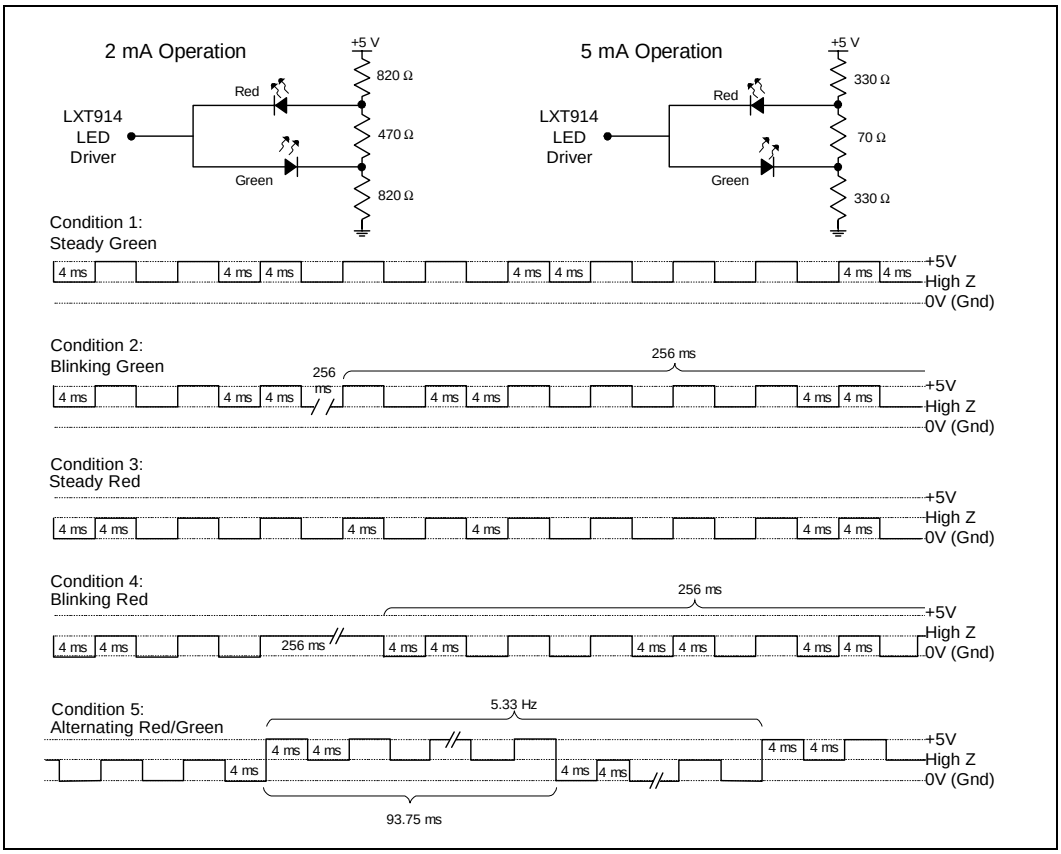
Table 17. Mode 2 LED Truth Table

Condition	LEDTP 1–4	LEDAUI	LEDCF	LEDJM
1	Rx Link Pulse	N/A	MAU Jabber Lockup Protection (MJLP)	N/A
2	Partitioned Out	Partitioned Out	N/A	N/A
3	N/A	N/A	Collision	N/A
4	Rx Packet	Rx Packet	N/A	N/A
5	N/A	N/A	N/A	N/A

Table 18. Mode 3 LED Truth Table

Condition	LEDTP 1–4	LEDAUI	LEDCF	LEDJM
1	Rx Link Pulse	N/A	MAU Jabber Lockup Protection (MJLP)	N/A
2	Rx Packet	Rx Packet	N/A	N/A
3	Partitioned Out	Partitioned Out	Collision	N/A
4	N/A	N/A	N/A	N/A
5	N/A	N/A	N/A	N/A

Figure 5. Integrated LED Driver Indications



3.0 Application Information

3.1 Layout Requirements

3.1.1 The Twisted Pair Interface

The four, twisted-pair output circuits are identical. Each TPDOP/TPDON signal has a 24.9 Ω, 1%, series resistor and a 120pF capacitor differentially across the positive and negative outputs. These signals go directly to a 1:$\sqrt{2}$ transformer creating the necessary 100 Ω termination for the cable. The TPDIP/TPDIN signals have a 100 Ω resistor across the positive and negative input signals to terminate the 100 Ω signal received from the line. To calculate the impedance on the output line interface, use:

$$(24.9\ \Omega + 24.9\ \Omega) * \sqrt{2}^2 \approx 100\ \Omega.$$

The layout of the twisted-pair ports is critical in complex designs. Run the signals directly from the device to the discrete termination components (located close to the transformers).

The signals running from the transformers to the connector should run in close pairs directly to the connector. Be careful not to cross the transmit and receive pairs. One way to avoid a problem is to run the receive pairs on the component side and the transmit pairs on the solder side. Careful planning during the schematic and layout stages can avoid these problems.

The PCB layout should have no ground or power planes from the transformers to the connectors. The data signals should be the only traces in this area. Place the chassis ground for the connectors near the edge of the PCB, away from the signals, connecting the connector shield with the chassis.

3.1.2 The RBIAS Pin

The RBIAS signal sets the levels for the output drivers of the LXT914 Repeater. Any emissions or common mode noise entering the device here could be measured on the twisted pair output signals. The LXT914 Repeater requires a 12.4 kΩ, 1% resistor directly connected to RBIAS. This connection should be as short as possible. The ground rails from the adjacent ground pins should come directly off of the device to enclose the resistor and pin forming a shielded area between the RBIAS connection and the switching signals on the PCB.

3.2 12-Port Hub Repeater

Figure 6 through Figure 9 (Sheets 1 through 4) show a simple 12-port hub repeater application with three LXT914 Repeaters. This application also provides two additional AUI ports—one DB-15 connector and one coaxial port. The application shown uses the asynchronous backplane mode so no external backplane clock source is required.

Figure 6 (Sheet 1) shows the XL93C46 EEPROM which downloads the setup parameters for all the LXT914 Repeater devices at initialization. (This EEPROM could be replaced with a simple pull down resistor on the SDI pin. This will select the default conditions of the set up register.) A single 20 MHz crystal provides the SYSCLK for all three LXT914 Repeater. The LXT914 Repeater hub repeater on Sheet 1 provides the AUI DB-15 connector as well as four twisted-pair ports. Table 19 lists transformers suggested for use with the LXT914 Repeater.

Figure 7 (Sheet 2) shows a second LXT914 Repeater hub repeater with four TP ports and a coaxial port. The MD-001 coax transceiver is used to implement the port. Figure 8 (Sheet 3) shows the third LXT914 Repeater device with its four TP ports and indicator LEDs. The AUI port of the third LXT914 Repeater is not used. Figure 9 (Sheet 4) of the schematic shows the LEDs for the remaining LXT914 Repeaters, along with the LED operation table.

3.3 8-Port Print or File Server

Figure 10 and Figure 11 (Sheets 1 and 2) show an eight-port repeater attachment for an existing single port AUI or 10BASE5 interface. This application can be added to a current design with an existing AUI or 10BASE5 interface. This circuit allows increased connectivity without the need for another external remote hub. The application shown is a 68-pin PLCC, an asynchronous backplane with both LXT914 Repeaters in the first position.

In Figure 10 (Sheet 1) the LXT914 Repeater is set up with the LEDs in Mode 1 with one LED per port and a single collision LED. The twisted pair port LEDs display link integrity only. (Refer to Table 16.) LED Mode 1 is selected by pulling LEDM0 High with a 1 kΩ resistor on pin 17 and pulling LEDM1 Low with pin 35 attached to ground.

Figure 11 (Sheet 2) has the same configuration, mode of operation and LED Mode as used in Sheet 1. However, the AUI port has been configured as a MAU interface. This is selected when LEDJM/AUISEL on pin 28 is pulled up through a 1 kΩ resistor. This mode disables the LEDJM pin as an LED driver. (See Table 13.) The MAU interface now configured on the LXT914 Repeater allows the AUI port to attach to a DTE interface. This application increases connectivity to any existing single-port Ethernet design. This unique application allows the designer to integrate an external hub, eliminating the need for additional external equipment.

Table 19. Manufacturers Magnetics List

Manufacturer	Quad Transmit	Quad Receive	Tx/Rx Pairs
Bell Fuse	S553-5999-02	S553-5999-03	–
Fil-Mag	23Z339	23Z338	–
HALO	TD54-1006L1 TG54-1006N2	TD01-1006L1 TG01-1006N2	TD42-2006Q; TD43-2006K; TG42-1406N1 TG43-1406N
(Octal)	–	–	TG44-S010NX
Kappa	TP4003P	TP497P101	–
Nanopulse	5976	5977	–
PCA	EPE6009	EPE6010	–
Pulse Eng.	PE68810	PE68820	PE65745; PE65994; PE65746; PE65998
VALOR	PT4116	PT4117	PT4069N1; PT4068N1; ST7011S2; ST7010S2

Figure 6. 12-Port Application Schematic, 68-Pin PLCC Package (Sheet 1 of 4)

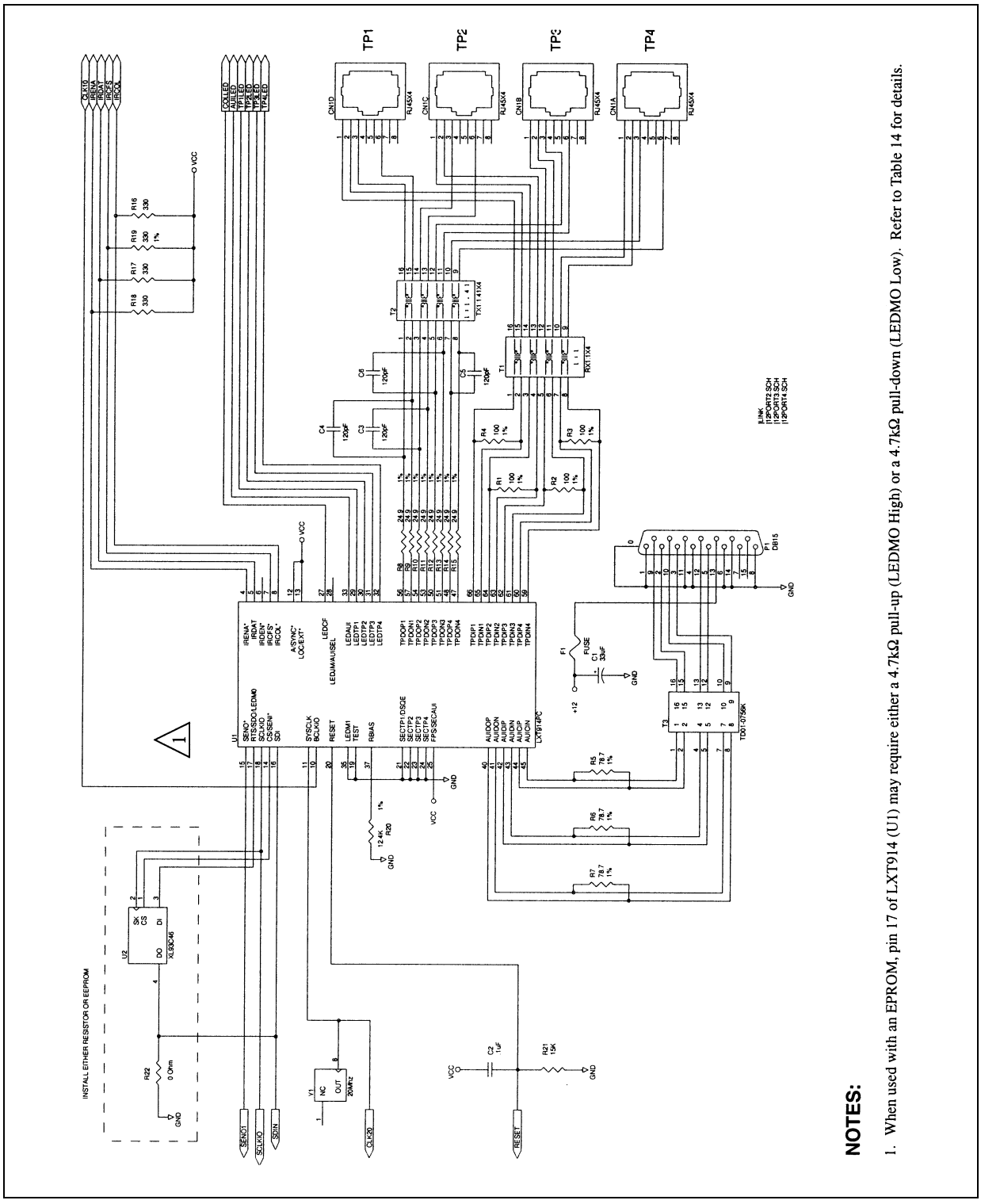


Figure 7. 12-Port Application Schematic, 68-Pin PLCC Package (Sheet 2 of 4)

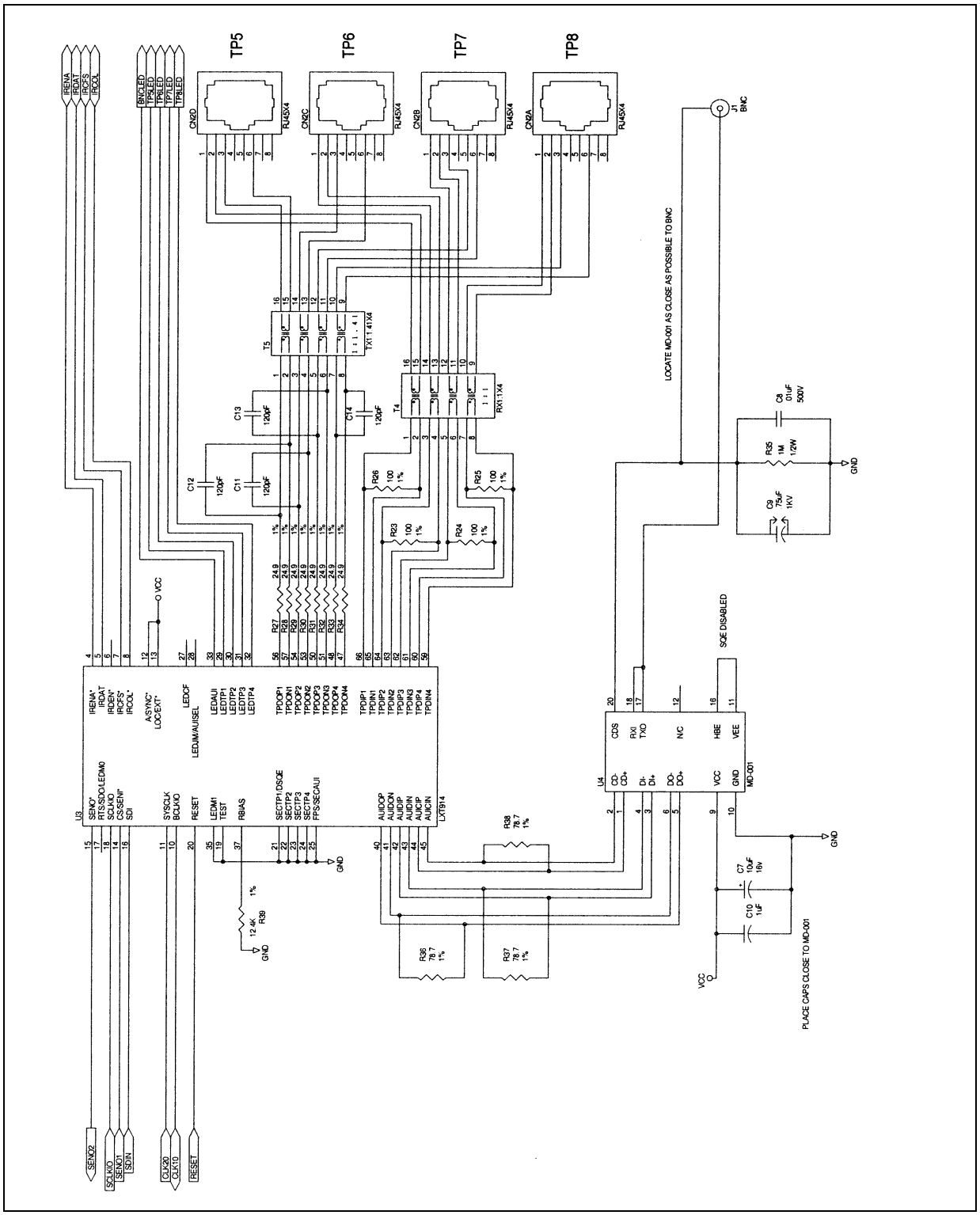


Figure 8. 12-Port Application Schematic, 68-Pin PLCC Package (Sheet 3 of 4)

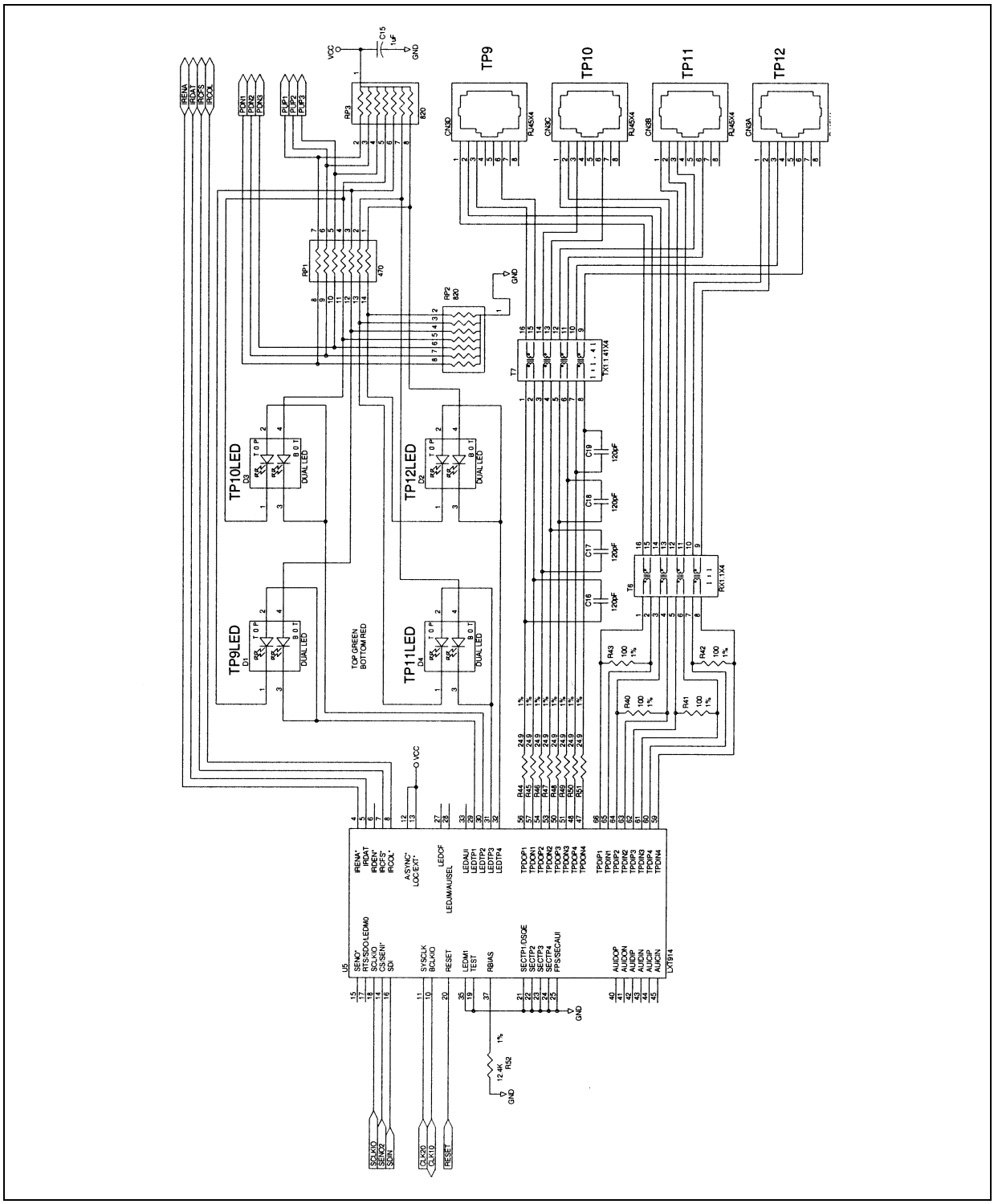


Figure 9. 12-Port Application Schematic, 68-Pin PLCC Package (Sheet 4 of 4)

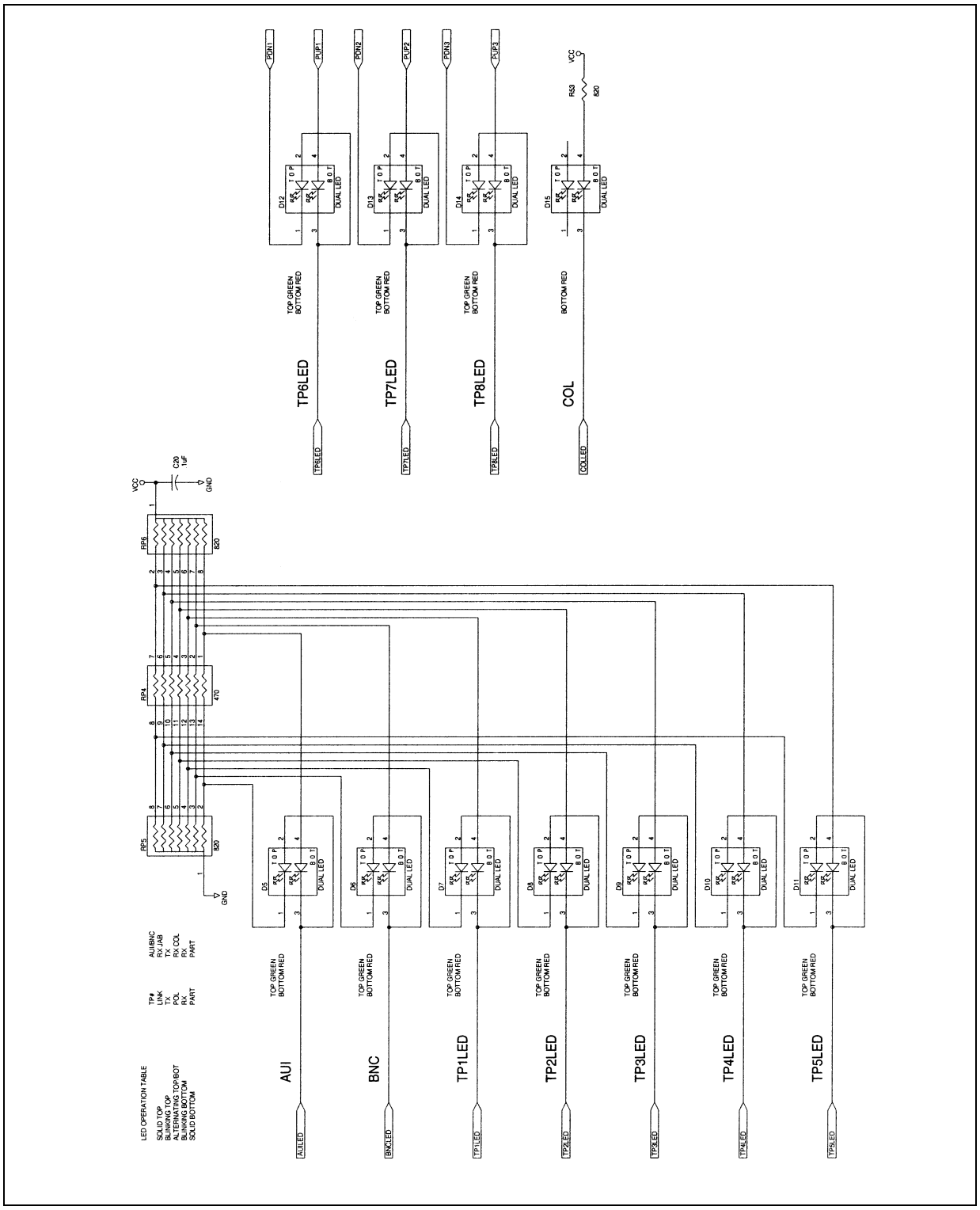


Figure 10. 8-Port Application Schematic, LED Mode 1 with AUISEL = MAU (Sheet 1 of 2)

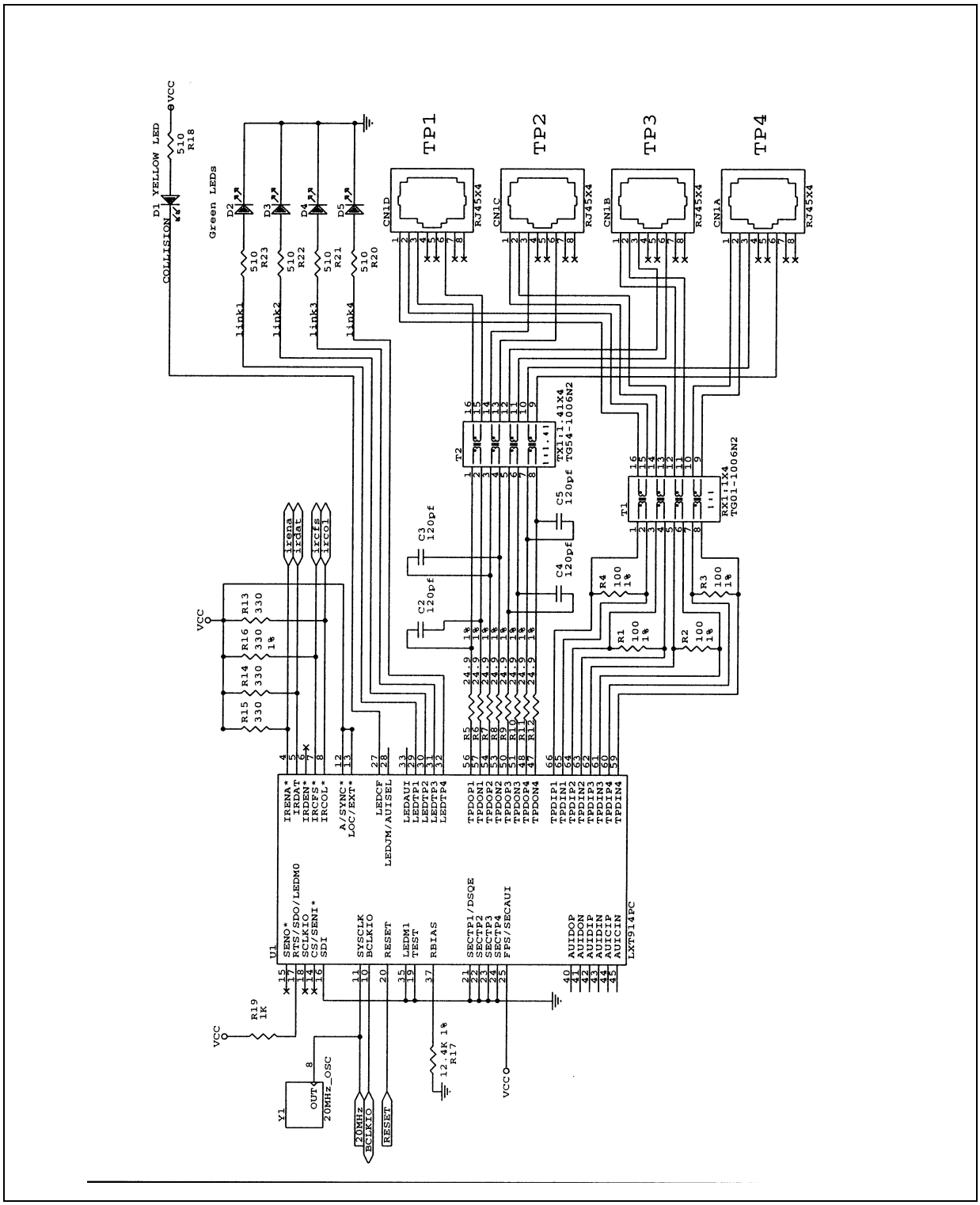
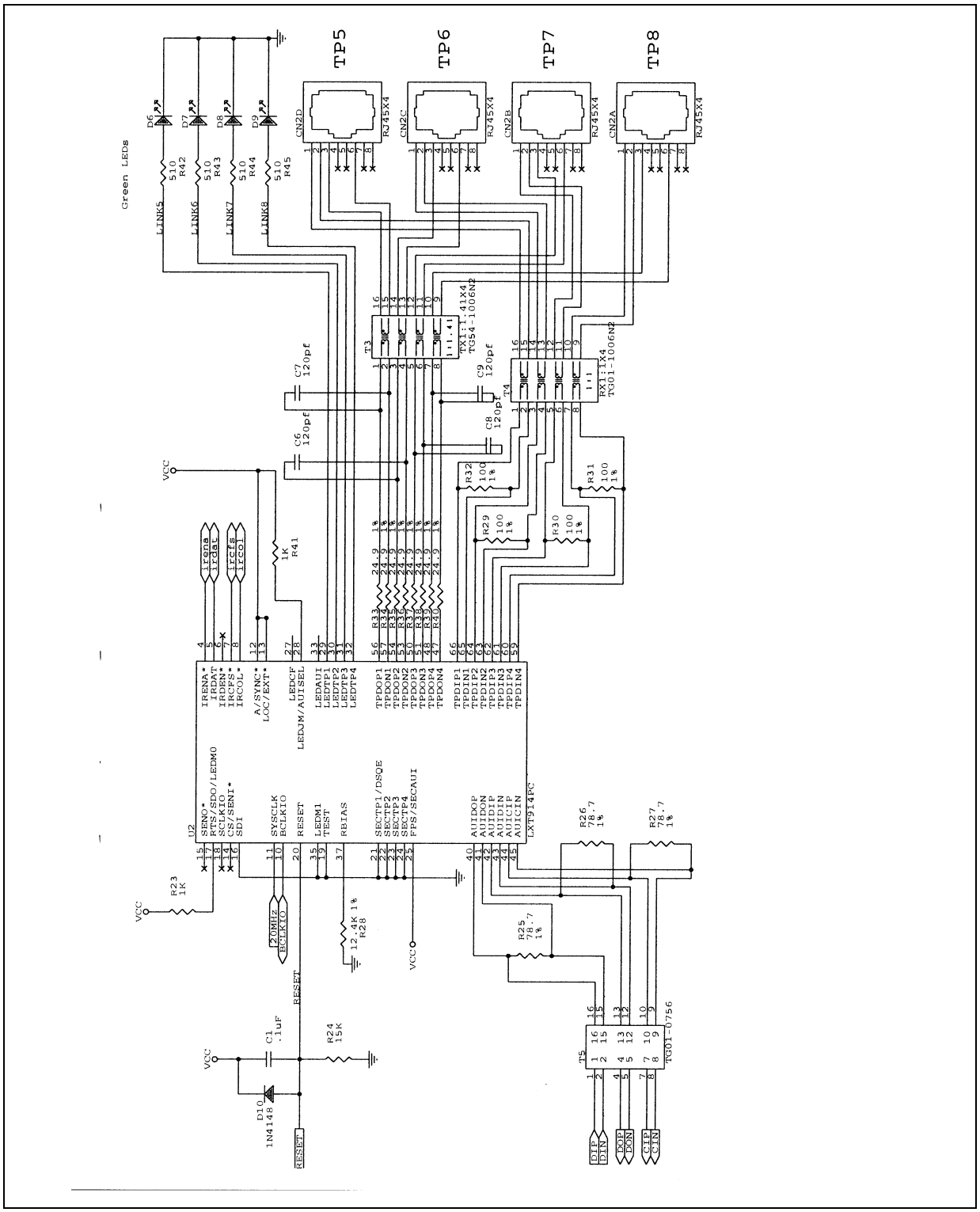


Figure 11. 8-Port Application Schematic, LED Mode 1 with AUISEL = MAU (Sheet 2 of 2)



4.0 Test Specifications

Note: Table 20 through Table 28 and Figure 12 and Figure 13 represent the performance specifications of the LXT914. These specifications are guaranteed by test except where noted "by design." Minimum and maximum values listed in Table 22 through Table 28 apply over the recommended operating conditions specified in Table 21.

Table 20. Absolute Maximum Ratings

Parameter		Symbol	Min	Typ	Max	Units
Supply voltage		VCC	-0.3	–	6	V
Operating temperature	LXT914PC/QC	TOP	0	–	+70	° C
	LXT914PE	TOP	-40	–	+85	° C
Storage temperature		TST	-65	–	+150	° C

Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 21. Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Units
Recommended supply voltage		VCC	4.75	5.0	5.25	V
Recommended operating temperature	LXT914PC/QC	TOP	0	–	+70	° C
	LXT914PE	TOP	-40	–	+85	° C

Table 22. I/O Electrical Characteristics[1] (Sheet 1 of 2)

Parameter	Symbol	Min	Typ[2]	Max	Units	Test Conditions
Supply current	ICC	–	–	240	mA	100Ω test load, no LEDs
Input Low voltage	VIL	–	–	0.8	V	–
Input Low voltage (RESET)	VILRESET	–	–	0.8	V	VCC = 5.25 V
Input High voltage	VIH	2.0	–	–	V	–
Input High voltage (RESET)	VIHRESET	4.0	–	–	V	VCC = 4.75 V
Output Low voltage	VOL	–	–	0.4	V	IOL = 1.6 mA
Output Low voltage	VOL	–	–	10	% V_{CC}	IOL < 10 µA
Output Low voltage (LED)	VOLL	–	–	1.0	V	IOLL = 5 mA
Output High voltage	VOH	2.4	–	–	V	IOH = 40 µA
Output High voltage	VOH	90	–	–	% V_{CC}	IOH < 10 µA
Output High voltage (LED)	VOHL	4	–	–	V	IOHL = -5 mA

NOTES:
1. Not applicable to IRB signals. IRB electrical characteristics are specified in Table 25.
2. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
3. Supply current may vary depending on the transformer, LED, and resistor selections.

Table 22. I/O Electrical Characteristics[1] (Sheet 2 of 2)

Parameter	Symbol	Min	Typ[2]	Max	Units	Test Conditions
Input Low current	I_{IL}	–	–	2	mA	V_{OL} = .4 V
Output rise / fall time	–	–	3	8	ns	C_{LOAD} = 20 pF
RESET pulse width	PW_{RESET}	1.0	–	–	ms	V_{CC} = 4.75 V
RESET fall time	TF_{RESET}	–	–	20.0	µs	$V_{IHRESET}$ to $V_{ILRESET}$

NOTES:
1. Not applicable to IRB signals. IRB electrical characteristics are specified in Table 25.
2. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
3. Supply current may vary depending on the transformer, LED, and resistor selections.

Table 23. AUI Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low current	I_{IL}	–	–	-700	µA	
Input High current	I_{IH}	–	–	500	µA	
Differential output voltage	V_{OD}	±550	–	±1200	mV	
Receive input impedance	Z_{IN}	–	20	–	kΩ	Between CIP/CIN & DIP/DIN
Differential squelch threshold	V_{DS}	–	220	–	mV	

Note:
1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 24. Twisted-Pair Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance	Z_{OUT}	–	5	–	Ω	
Peak differential output voltage	V_{OD}	3.3	3.5	3.7	V	Load = 100 Ω at TPOP and TPON
Transmit timing jitter addition	–	–	± 6.4	± 10	ns	0 line length
Transmit timing jitter added by the MAU and PLS sections[2]	–	–	± 3.5	± 5.5	ns	After line model specified by IEEE 802.3 for 10BASE-T
Receive input impedance	Z_{IN}	–	20	–	kΩ	Between TPIP/TPIN
Differential squelch threshold (Normal threshold: ERSQ*x* = 0)	V_{DS}	300	420	565	mV	5 MHz square wave input
Differential squelch threshold (Reduced threshold: ERSQ*x* = 1)	V_{DSL}	180	250	345	mV	5 MHz square wave input

NOTES:
1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. IEEE 802.3 specifies maximum jitter additions at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.

Table 25. IRB Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Output Low voltage	VOL	–	.3	.6	V	
Output rise or fall time	TF	–	4	12	ns	
Input Low voltage: $\overline{\text{IRENA}}$, IRCOL & IRDAT	VILIRB	–	–	0.8	V	RL = 330 Ω
Input High voltage: $\overline{\text{IRENA}}$, IRCOL & IRDAT	VIHIRB	3.0	–	–	V	RL = 330 Ω
Input Low voltage: BCLKIO	VILBCLK	–	–	0.4	V	RL = 330 Ω
Input High voltage: BCLKIO	VIHBCLK	4.0	–	–	V	RL = 330 Ω

Note:
1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 26. Switching Characteristics

Parameter		Min	Typ[1]	Max	Units
Jabber Timing	Maximum transmit time	5.0	–	5.5	ms
	Unjab time	–	9.6	–	µs
Link Integrity Timing	Time link loss	–	60	–	ms
	Time between Link Integrity Pulses	10	–	20	ms
	Interval for valid receive Link Integrity Pulses	4.1	–	30	ms

Note:
1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 27. Serial Port Timing—External Mode

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
SCLKIO High to $\overline{\text{SENI}}$ Low (active)	tS1	0	–	50	ns
SCLKIO High to SDIN data valid	tS2	0	–	50	ns
SCLKIO High to $\overline{\text{SENO}}$ Low (active)	tS3	5	–	15	ns
SCLKIO Low to SDOUT data valid	tS4	5	–	15	ns

Note:
1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 12. Serial Port Timing

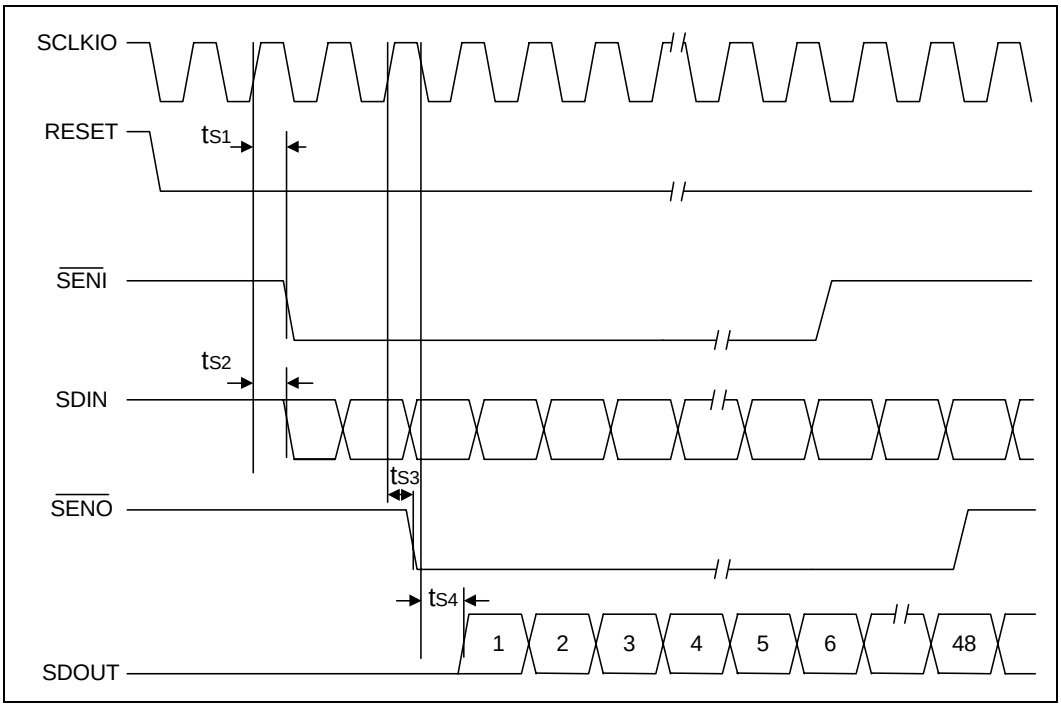
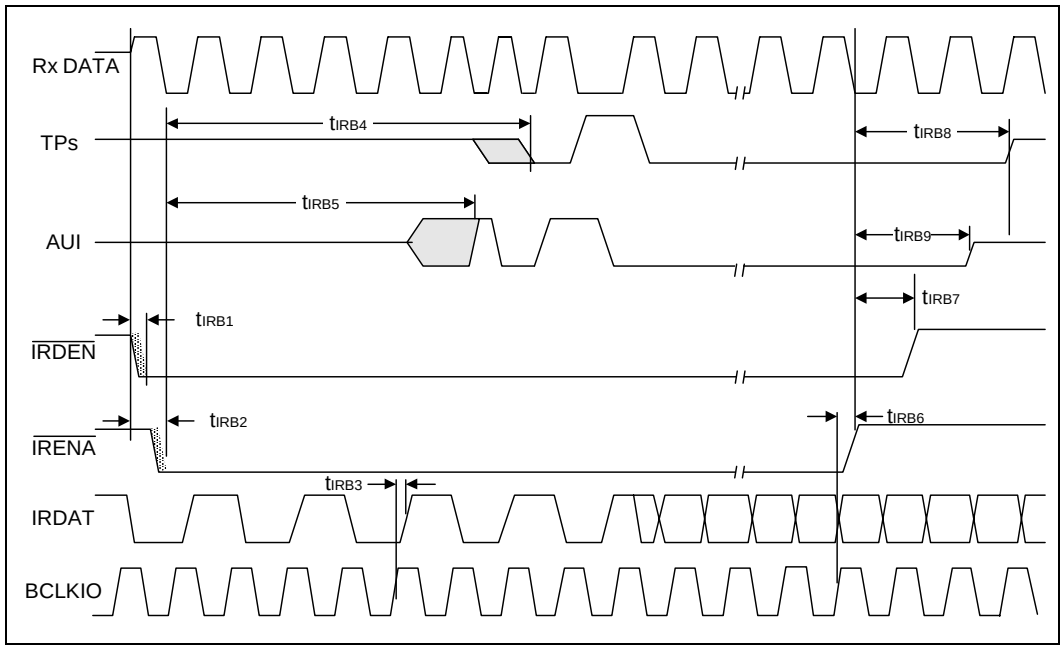


Table 28. Inter-Repeater Bus Timing

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
Start of Frame to $\overline{\text{IRDEN}}$ Low (active)	tIRB1	10	–	150	ns
Start of Frame to $\overline{\text{IRENA}}$ Low (active)	tIRB2	125	–	225	ns
BCLKIO to IRDAT valid (Synchronous mode)	tIRB3	5	–	30	ns
BCLKIO to IRDAT valid (Asynchronous mode)	tIRB3	–	50	–	ns
$\overline{\text{IRENA}}$ Low (active) to TP outputs active	tIRB4	525	–	600	ns
$\overline{\text{IRENA}}$ Low (active) to AUI output active	tIRB5	475	–	525	ns
End of Frame clock to $\overline{\text{IRENA}}$ High (inactive)	tIRB6	5	–	30	ns
$\overline{\text{IRENA}}$ High (inactive) to $\overline{\text{IRDEN}}$ High (inactive)	tIRB7	95	–	105	ns
$\overline{\text{IRENA}}$ High (inactive) to TP outputs inactive	tIRB8	575	–	600	ns
$\overline{\text{IRENA}}$ High (inactive) to AUI output inactive	tIRB9	425	–	450	ns

Note:
1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 13. Inter-Repeater Bus Timing



5.0 Package Specifications

Figure 14. LXT914PC/PE Package Specifications

68-Pin Plastic Leaded Chip Carrier

Part Number LXT914PC for Commercial Temperature Range (0°C to +70°C)
Part Number LXT914PE for Extended Temperature Range (-40°C to +85°C)

Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.165	0.180	4.191	4.572
A1	0.090	0.120	2.286	3.048
A2	0.062	0.083	1.575	2.108
B	0.050	–	1.270	–
C	0.026	0.032	0.660	0.813
D	0.985	0.995	25.019	25.273
D1	0.950	0.958	24.130	24.333
F	0.013	0.021	0.330	0.533

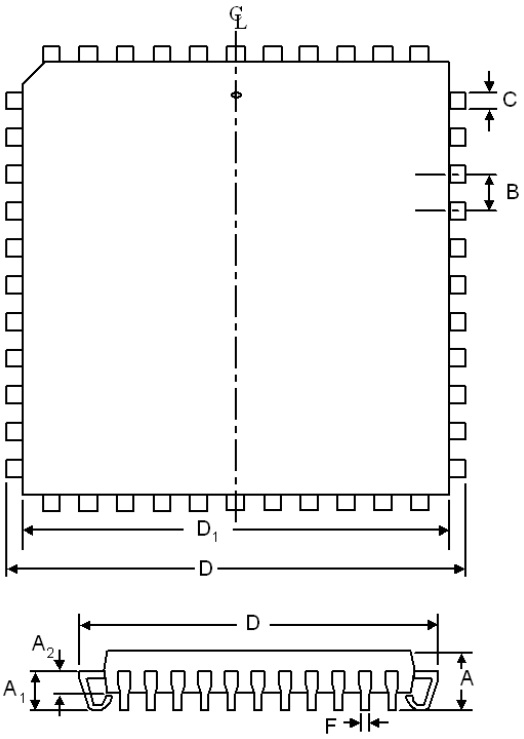


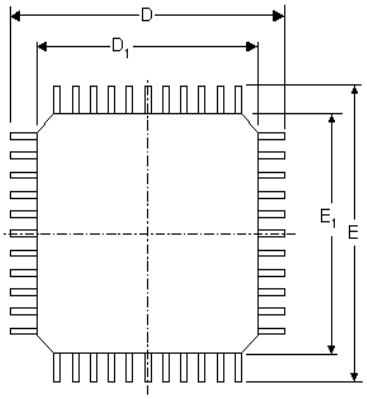
Figure 15. LXT914QC Package Specifications

100-Pin Quad Flat Package

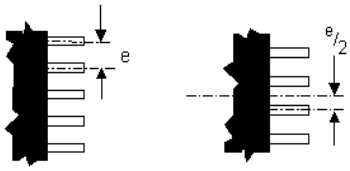
Part Number LXT914QC

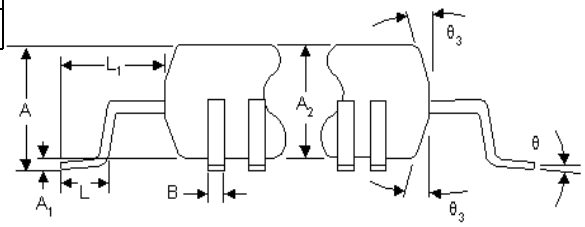
Commercial Temperature Range (0°C to +70°C)

Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	–	0.134	–	3.40
A1	0.010	–	0.25	–
A2	0.100	0.120	2.55	3.05
B	0.009	0.015	0.22	0.38
D	0.931	0.951	23.65	24.15
D1	0.783	0.791	19.90	20.10
D3	0.742 REF		18.85 REF	
E	0.695	0.715	17.65	18.15
E1	0.547	0.555	13.90	14.10
E3	0.486 REF		12.35 REF	
e	(nominal) 0.026 BSC[1]		(nominal) 0.65 BSC[1]	
L	0.026	0.037	0.65	0.95
L1	0.077 ref		1.95 ref	
q	0°	7°	0°	7°
q3	5°	16°	5°	16°
1.	BSC = Basic Spacing Between Centers			



D Side pin count = 30
E Side pin count = 20





5.1 Top-Label Marking

Figure 16 shows a sample PLCC package for the LXT914 Repeater.

Note: In contrast to the Pb-Free (RoHS-compliant) PLCC packages, the non-RoHS-compliant packages do not have the “e3” symbol in the last line of the package label.

Figure 16. Sample PLCC Package - Intel® LXT914 Repeater

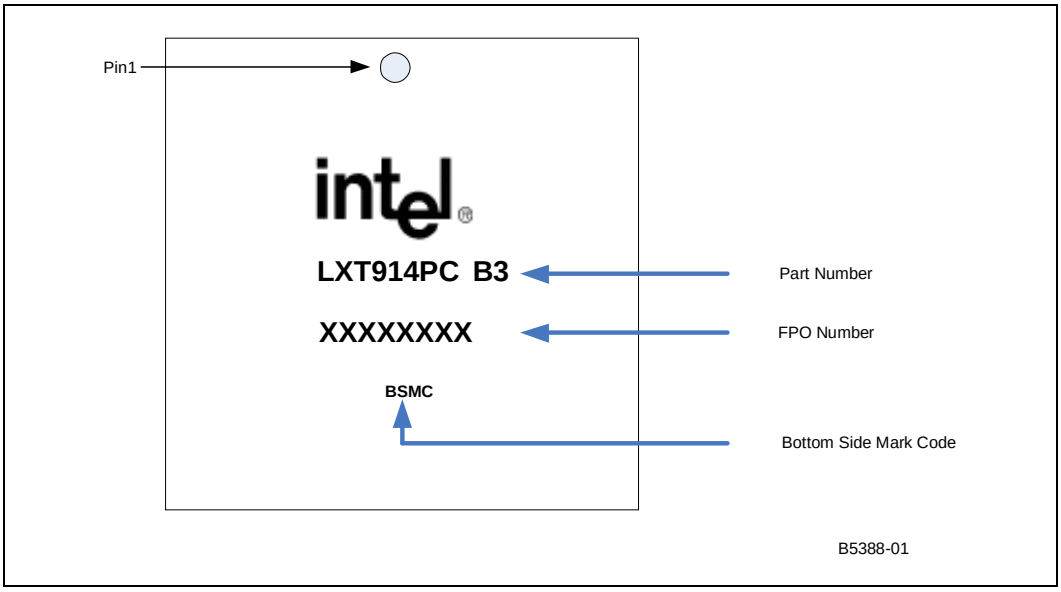


Figure 17 shows a sample Pb-Free (RoHS-compliant) PLCC package for the LXT914 Repeater.

Figure 17. Sample Pb-Free (RoHS-Compliant) PLCC Package - Intel® LXT914 Repeater

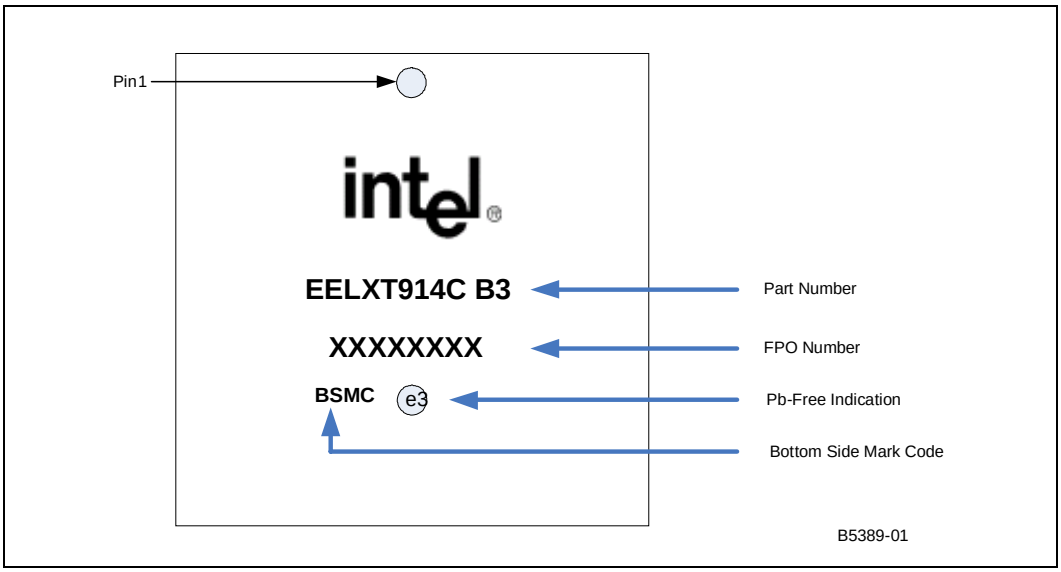


Figure 18 shows a sample PQFP package for the LXT914 Repeater.

Note: In contrast to the Pb-Free (RoHS-compliant) PQFP packages, the non-RoHS-compliant packages do not have the “e3” symbol in the last line of the package label.

Figure 18. Sample PQFP Package - Intel® LXT914 Repeater

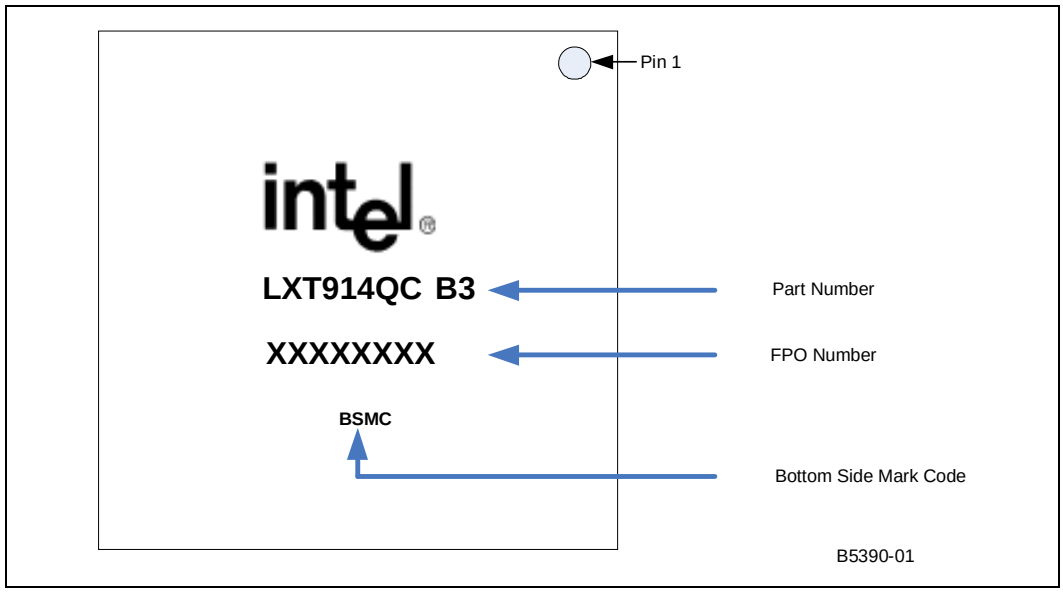
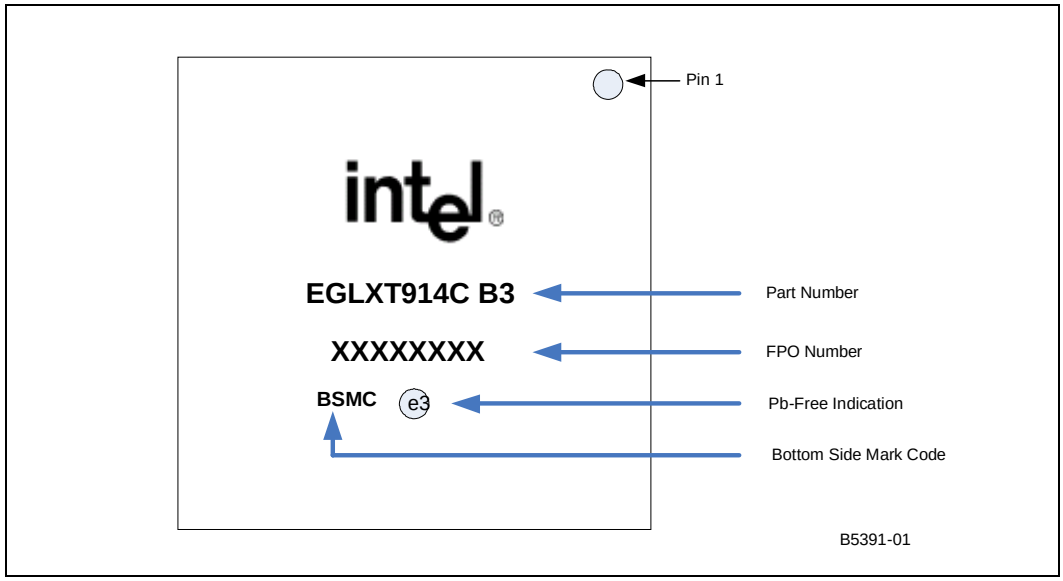


Figure 19 shows a sample Pb-Free (RoHS-compliant) PQFP package for the LXT914 Repeater.

Figure 19. Sample Pb-Free (RoHS-Compliant) PQFP Package - Intel® LXT914 Repeater



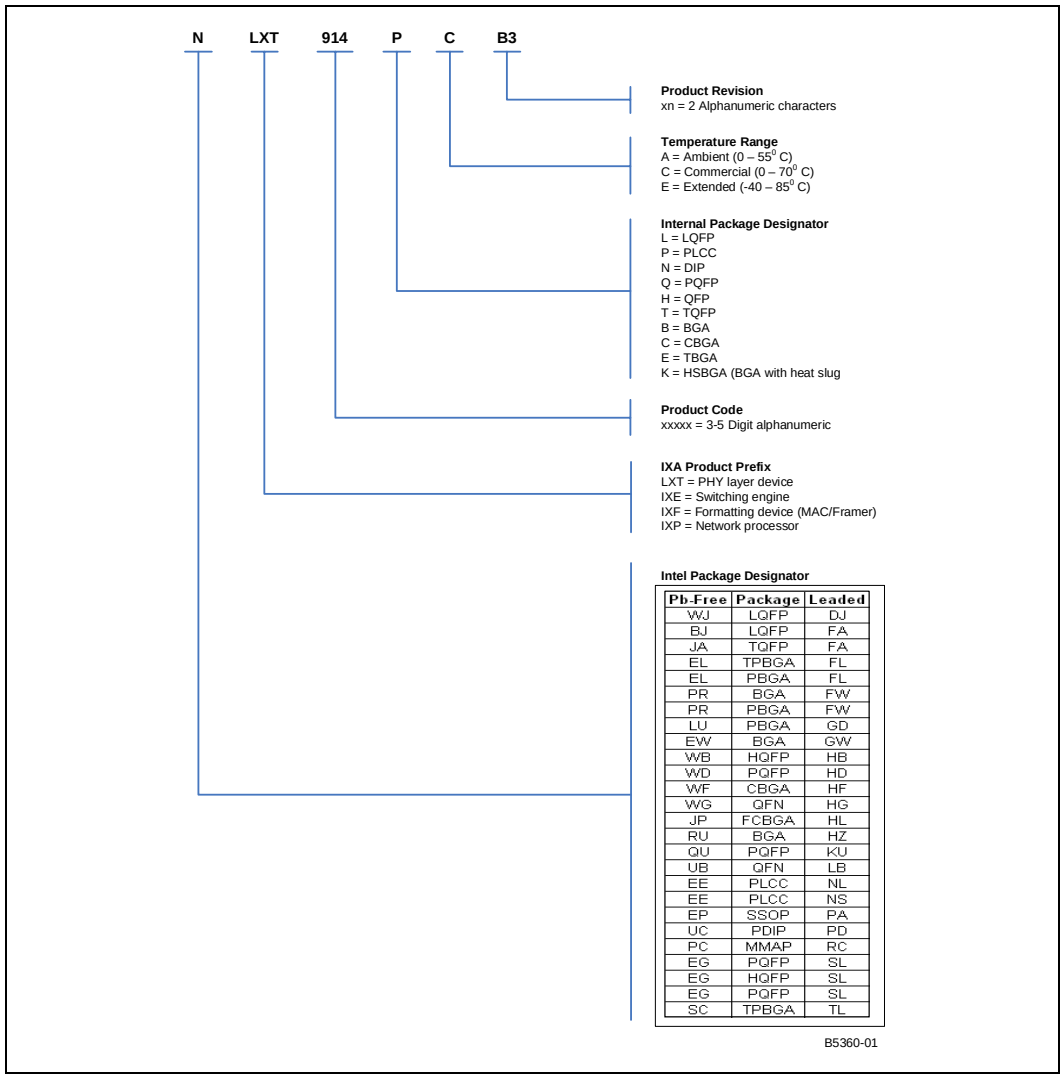
6.0 Product Ordering Information

Figure 29 and Figure 20 provide IXF1110 MAC product ordering information.

Table 29. Product Ordering Information

Number	Revision	Package Type	Pin Count	RoHS Compliant
NLXT914PC.B3	B3	PLCC	68	No
EELXT914PC.B3	B3	PLCC	68	Yes
NLXT914PE.B3	B3	PLCC	68	No
EELXT914PE.B3	B3	PLCC	68	Yes
SLXT914QC.B3	B3	PQFP	100	No
EGLXT914QC.B3	B3	PQFP	100	Yes

Figure 20. Ordering Information Matrix – Sample



Pb-Free	Package	Leaded
WJ	LQFP	DJ
BJ	LQFP	FA
JA	TQFP	FA
EL	TPBGA	FL
EL	PBGA	FL
PR	BGA	FW
PR	PBGA	FW
LU	PBGA	GD
EW	BGA	GW
WB	HQFP	HB
WD	PQFP	HD
WF	CBGA	HF
WG	QFN	HG
JP	FCBGA	HL
RU	BGA	HZ
QU	PQFP	KU
UB	QFN	LB
EE	PLCC	NL
EE	PLCC	NS
EP	SSOP	PA
UC	PDIP	PD
PC	MMAP	RC
EG	PQFP	SL
EG	HQFP	SL
EG	PQFP	SL
SC	TPBGA	TL

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