



STD5N52U STF5N52U, STI5N52U

N-channel 525 V, 1.28 Ω , 4.4 A, DPAK, TO-220FP, I²PAK
UltraFASTmesh™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on) max}	I _D	P _w
STD5N52U	525 V	< 1.5 Ω	4.4 A	70 W
STF5N52U				25 W
STI5N52U				70 W

- 100% avalanche tested
- Outstanding dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Very low R_{DS(on)}
- Extremely low t_{rr}

Applications

- Switching applications
 - High voltage inverters specific fo LCD TV
 - Lighting full bridge topology
 - Motor control

Description

These devices are N-channel Power MOSFETs developed using UltraFASTmesh™ technology, which combines the advantages of reduced on-resistance, Zener gate protection and very high dv/dt capability with an enhanced fast body-drain recovery diode.

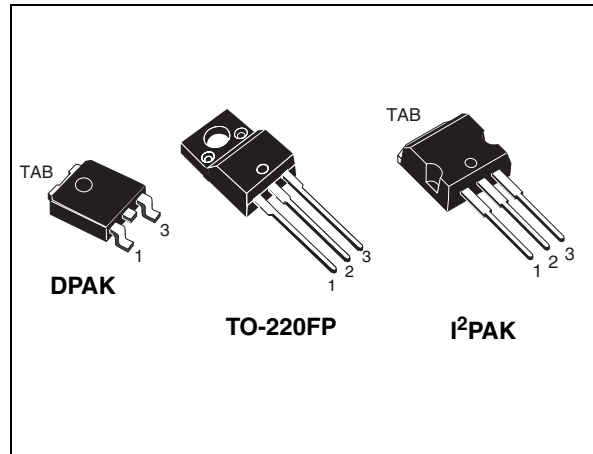


Figure 1. Internal schematic diagram

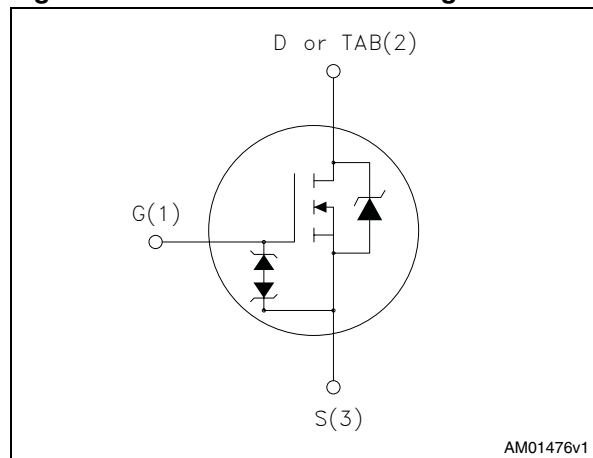


Table 1. Device summary

Order code	Marking	Package	Packaging
STD5N52U	5N52U	DPAK	Tape and reel
STF5N52U	5N52U	TO-220FP	Tube
STI5N52U	5N52U	I ² PAK	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
2.1	Electrical characteristics (curves)	6
3	Test circuits	9
4	Package mechanical data	10
5	Packaging mechanical data	15
6	Revision history	17

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		DPAK	TO-220FP	I ² PAK	
V _{GS}	Gate- source voltage	± 30			V
I _D	Drain current (continuous) at T _C = 25 °C	4.4			A
I _D	Drain current (continuous) at T _C = 100 °C	2.8			A
I _{DM} ⁽¹⁾	Drain current (pulsed)	17.6			A
P _{TOT}	Total dissipation at T _C = 25 °C	70	25	70	W
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _J max)	4.4			A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	170			mJ
dv/dt ⁽²⁾	Peak diode recovery voltage slope	20			V/ns
V _{ESD(G-S)}	G-S ESD (HBM C=100 pF; R=1.5 kΩ)	2800			V
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T _C =25 °C)		2500		V
T _J T _{stg}	Operating junction temperature Storage temperature	-55 to 150			°C

1. Pulse width limited by safe operating area.
2. I_{SD} ≤ 4.4 A, di/dt ≤ 400 A/μs, peak V_{DS} ≤ V_{(BR)DSS}

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		DPAK	TO-220FP	I ² PAK	
R _{thj-case}	Thermal resistance junction-case max	1.78	5	1.78	°C/W
R _{thj-amb}	Thermal resistance junction-ambient max		62.5	100	°C/W
R _{thj-pcb}	Thermal resistance junction-pcb	50			°C/W

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage (V _{GS} = 0)	I _D = 1 mA	525			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 525 V V _{DS} = 525 V, T _C = 125 °C			10 500	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 20 V			10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 50 μA	3	3.75	4.5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 2.2 A		1.28	1.5	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0	-	529	-	pF
C _{oss}	Output capacitance			71		pF
C _{rss}	Reverse transfer capacitance			13.4		pF
C _{o(tr)} ⁽¹⁾	Equivalent capacitance time related	V _{DS} = 0 to 420 V, V _{GS} = 0	-	11	-	pF
R _g	Gate input resistance	f = 1 MHz open drain	-	6	-	Ω
Q _g	Total gate charge	V _{DD} = 416 V, I _D = 4.4 A,	-	16.9	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 10 V		4.2		nC
Q _{gd}	Gate-drain charge	(see Figure 17)		8.4		nC

1. C_{oss,eq} time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 260 V, I _D = 2.2 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 16)	-	11.4	-	ns
t _r	Rise time			13.6		ns
t _{d(off)}	Turn-off-delay time			23.1		ns
t _f	Fall time			15		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4.4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		17.6	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4.4 \text{ A}, V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 4.4 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	-	55		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}$	-	95		μC
I_{RRM}	Reverse recovery current	(see Figure 18)	-	3.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 4.4 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	-	120		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V } T_J = 150 \text{ }^\circ\text{C}$	-	266		μC
I_{RRM}	Reverse recovery current	(see Figure 18)	-	4.5		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$ (open drain)	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device’s ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device’s integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK and i²PAK

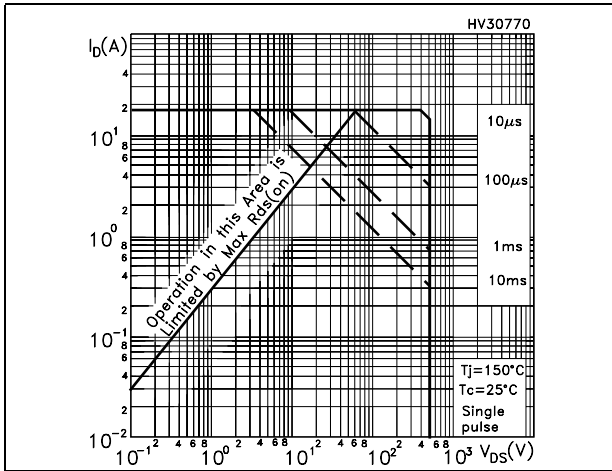


Figure 3. Thermal impedance for DPAK and i²PAK

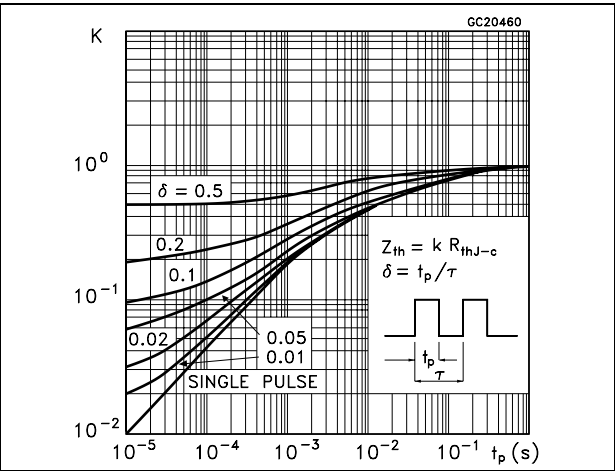


Figure 4. Safe operating area for TO-220FP

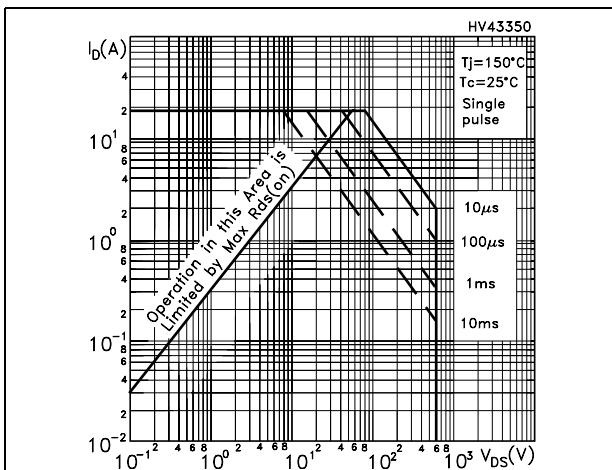


Figure 5. Thermal impedance for TO-220FP

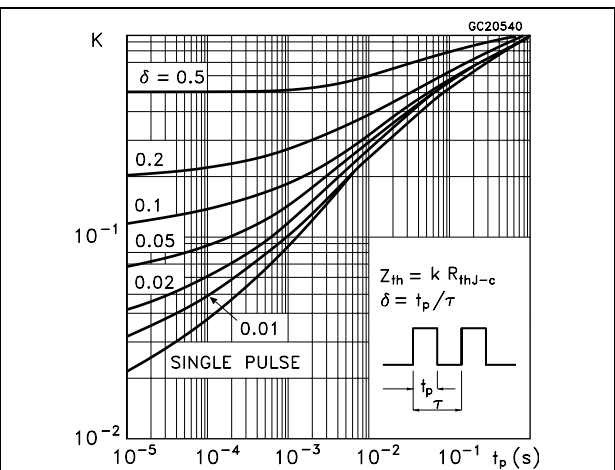


Figure 6. Output characteristics

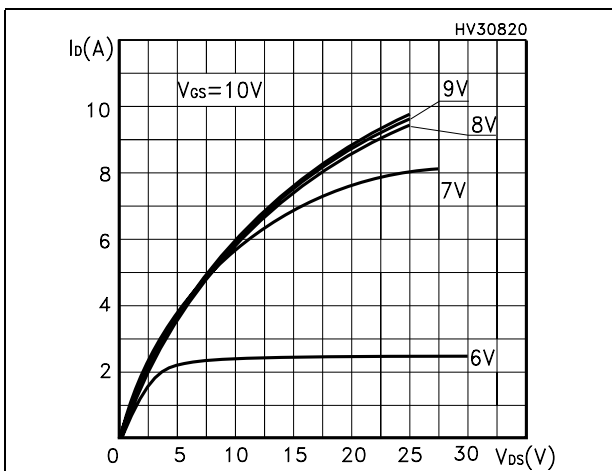


Figure 7. Transfer characteristics

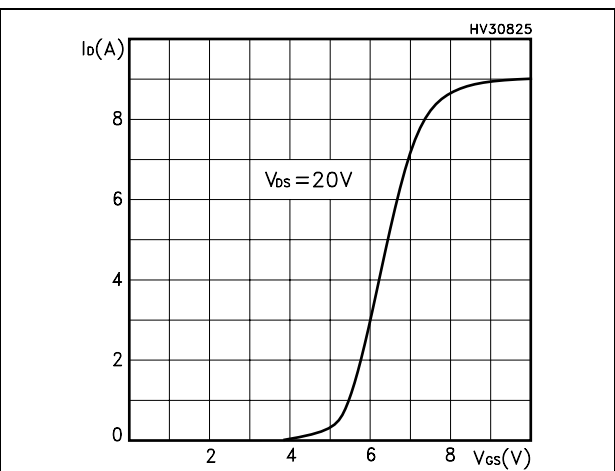


Figure 8. Normalized BV_{DSS} vs temperature Figure 9. Static drain-source on resistance

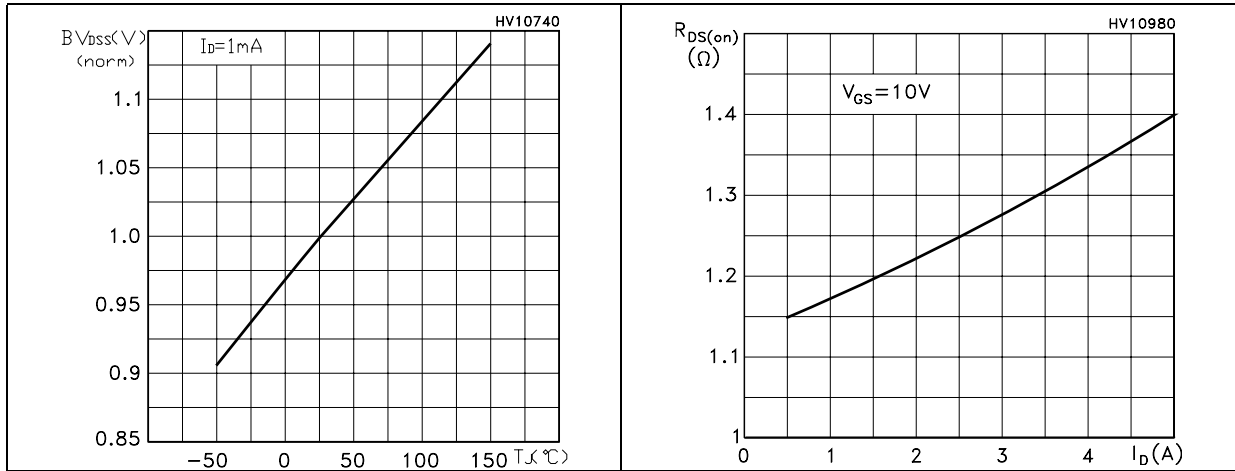


Figure 10. Gate charge vs gate-source voltage Figure 11. Capacitance variations

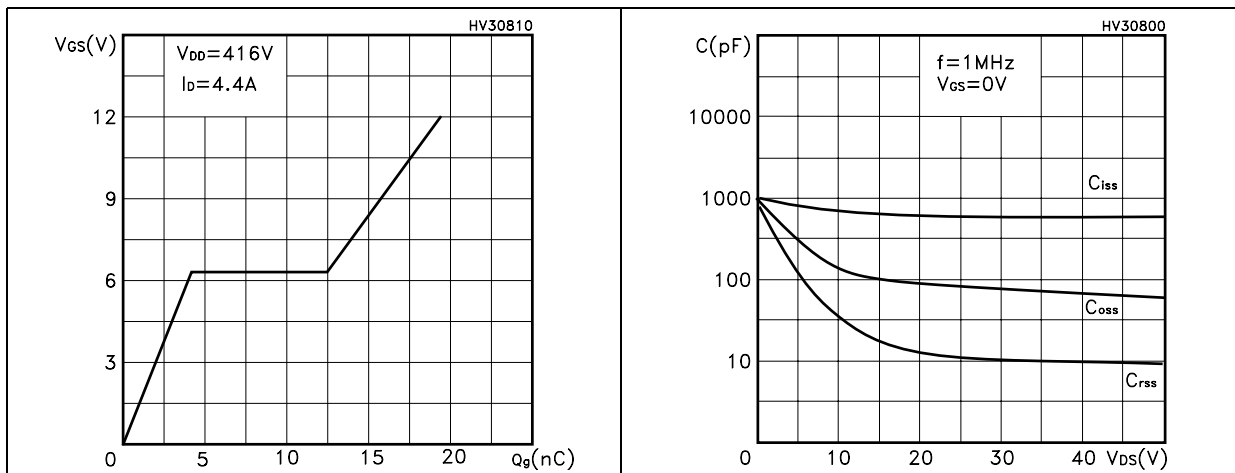


Figure 12. Normalized gate threshold voltage vs temperature Figure 13. Normalized on resistance vs temperature

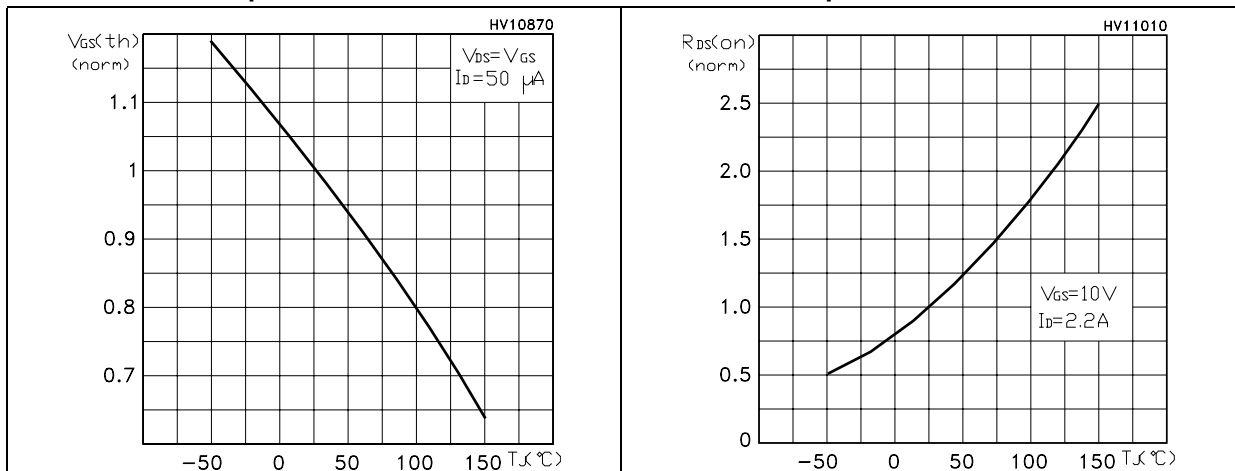


Figure 14. Source-drain diode forward characteristics

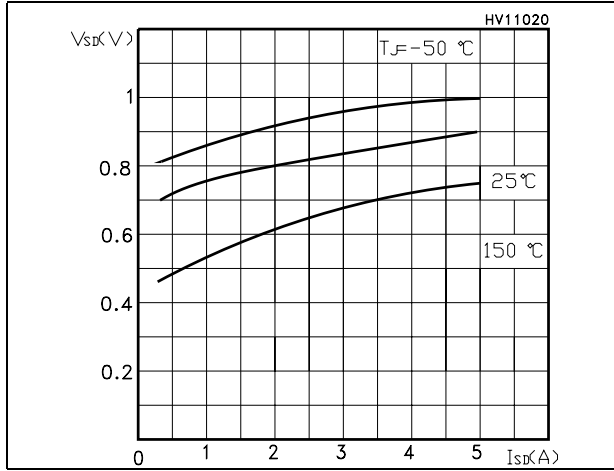
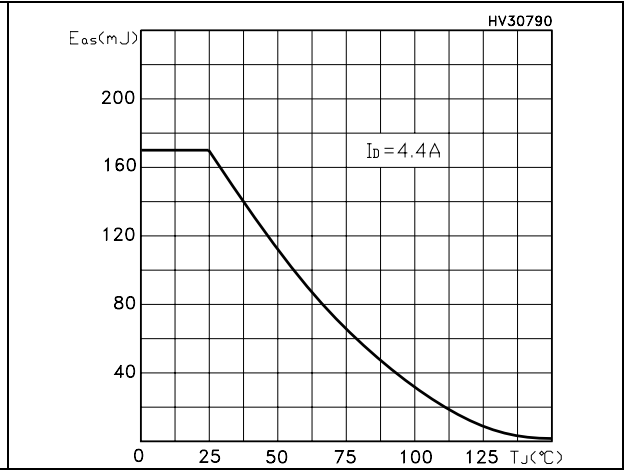
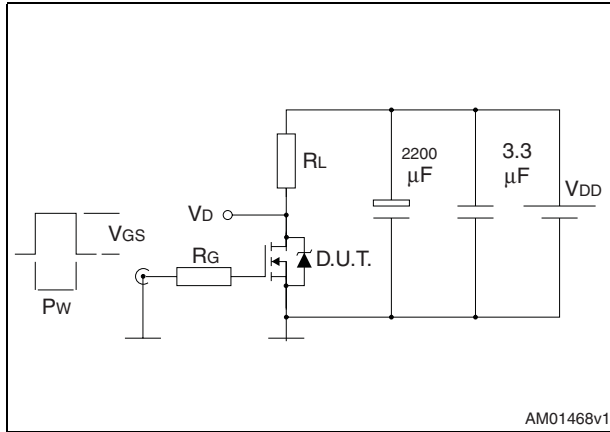


Figure 15. Maximum avalanche energy vs temperature



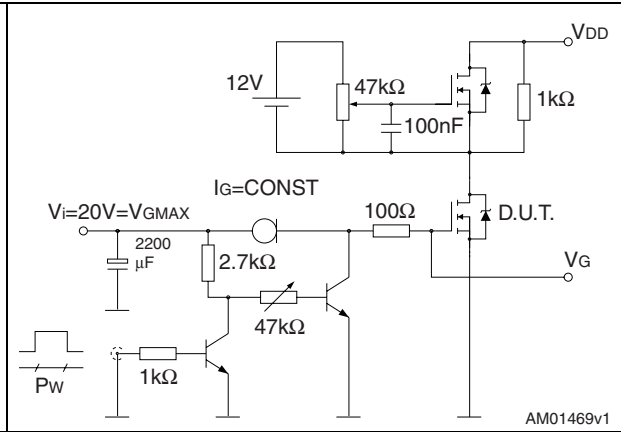
3 Test circuits

Figure 16. Switching times test circuit for resistive load



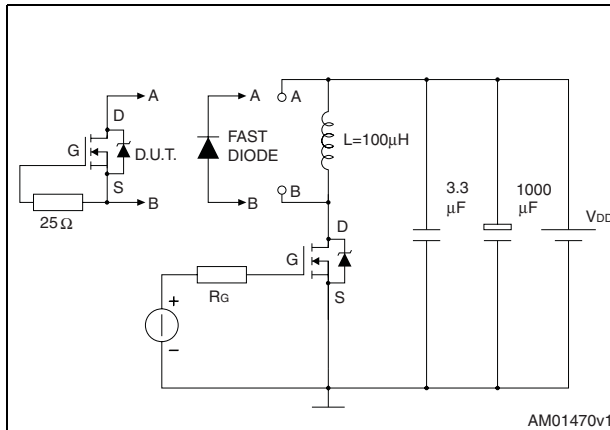
AM01468v1

Figure 17. Gate charge test circuit



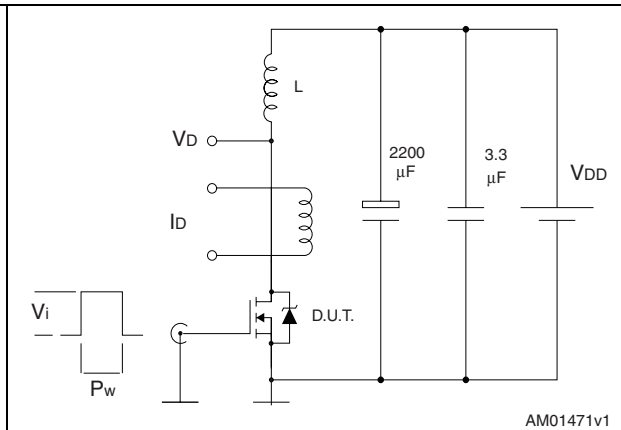
AM01469v1

Figure 18. Test circuit for inductive load switching and diode recovery times



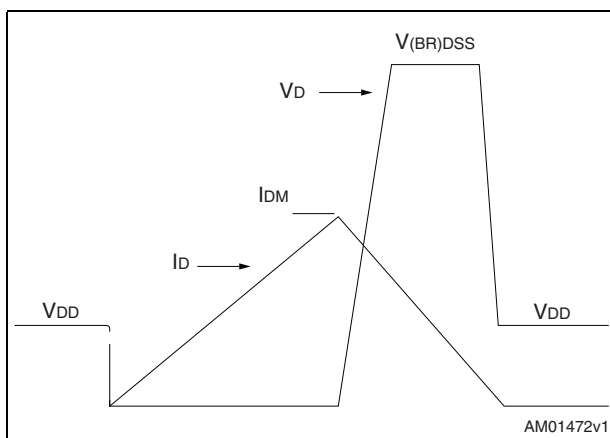
AM01470v1

Figure 19. Unclamped inductive load test circuit



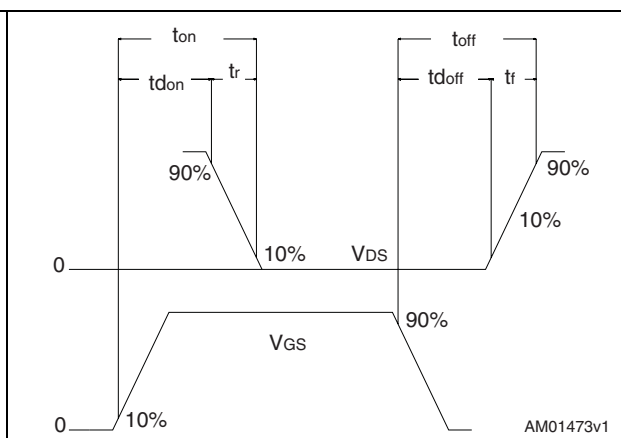
AM01471v1

Figure 20. Unclamped inductive waveform



AM01472v1

Figure 21. Switching time waveform



AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		1.50
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 22. DPAK (TO-252) drawing

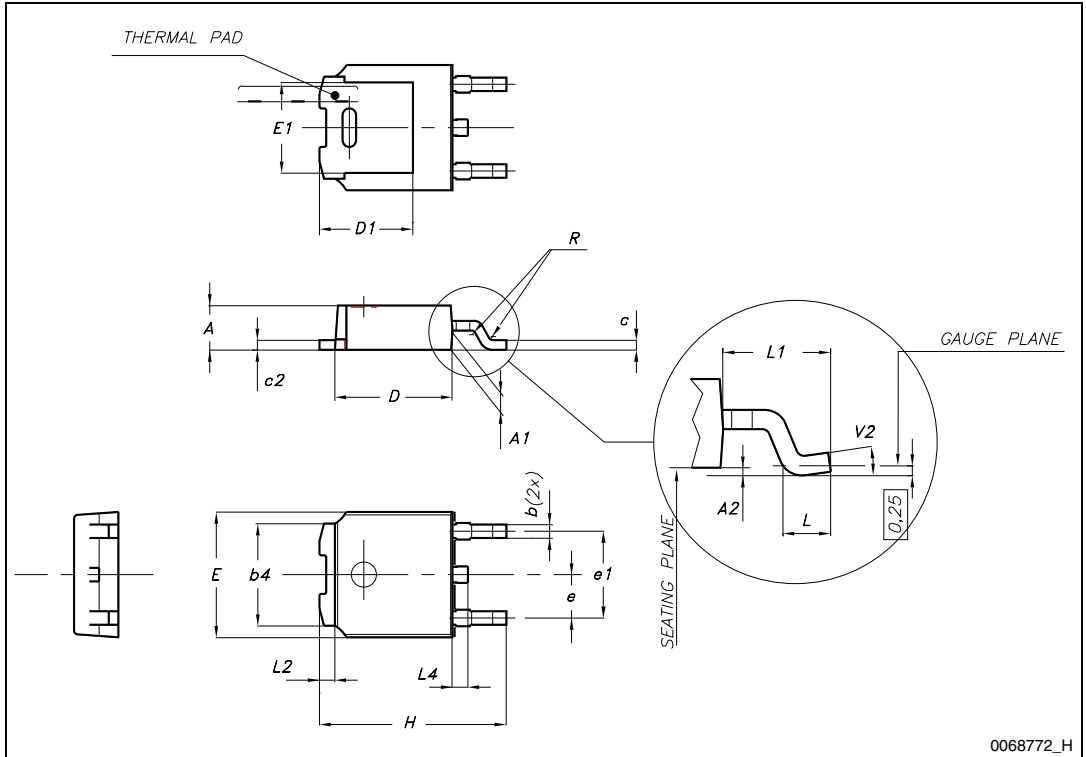
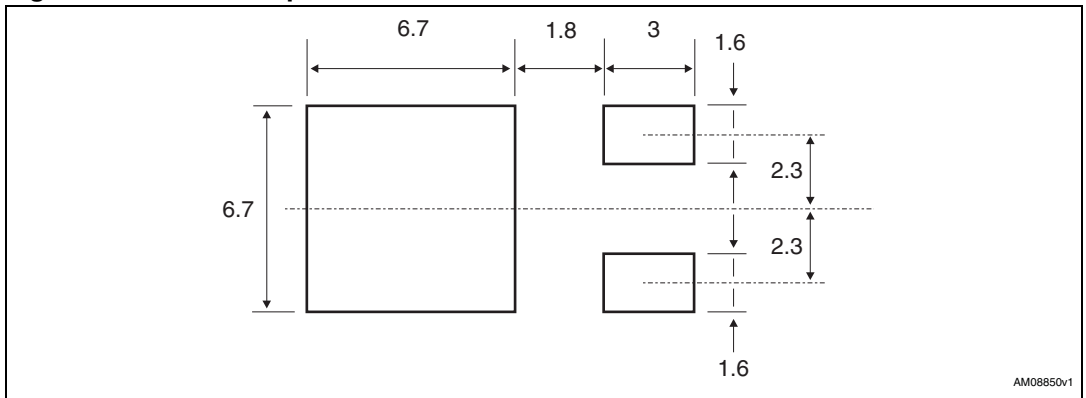


Figure 23. DPAK footprint^(a)

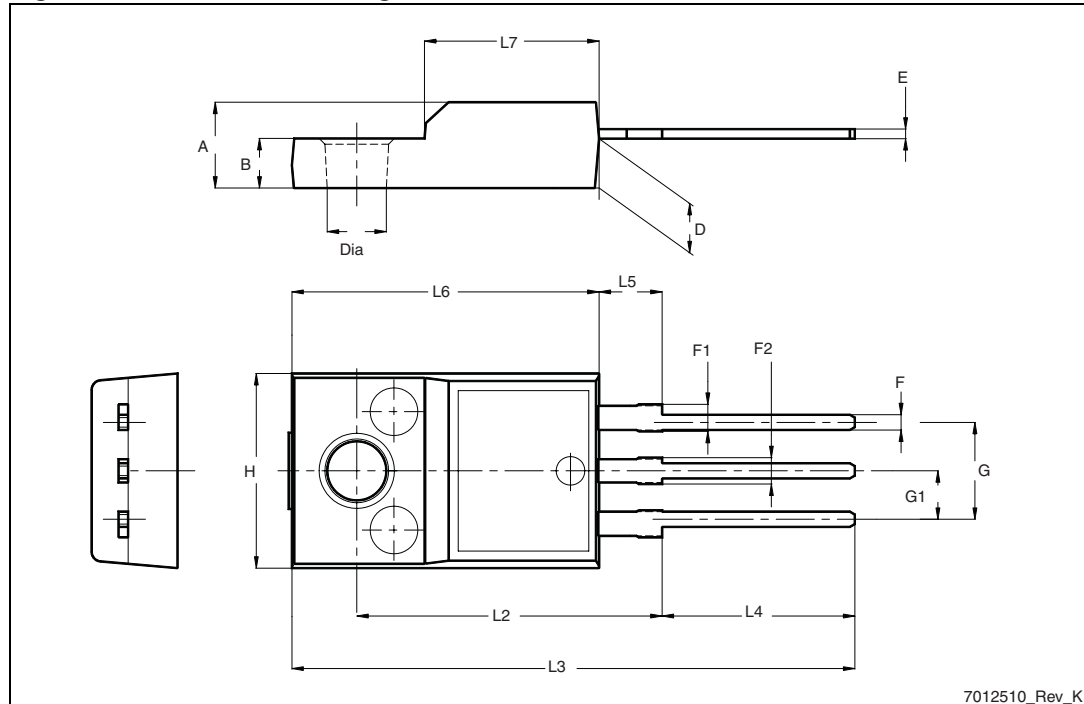


a. All dimension are in millimeters

Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 24. TO-220FP drawing

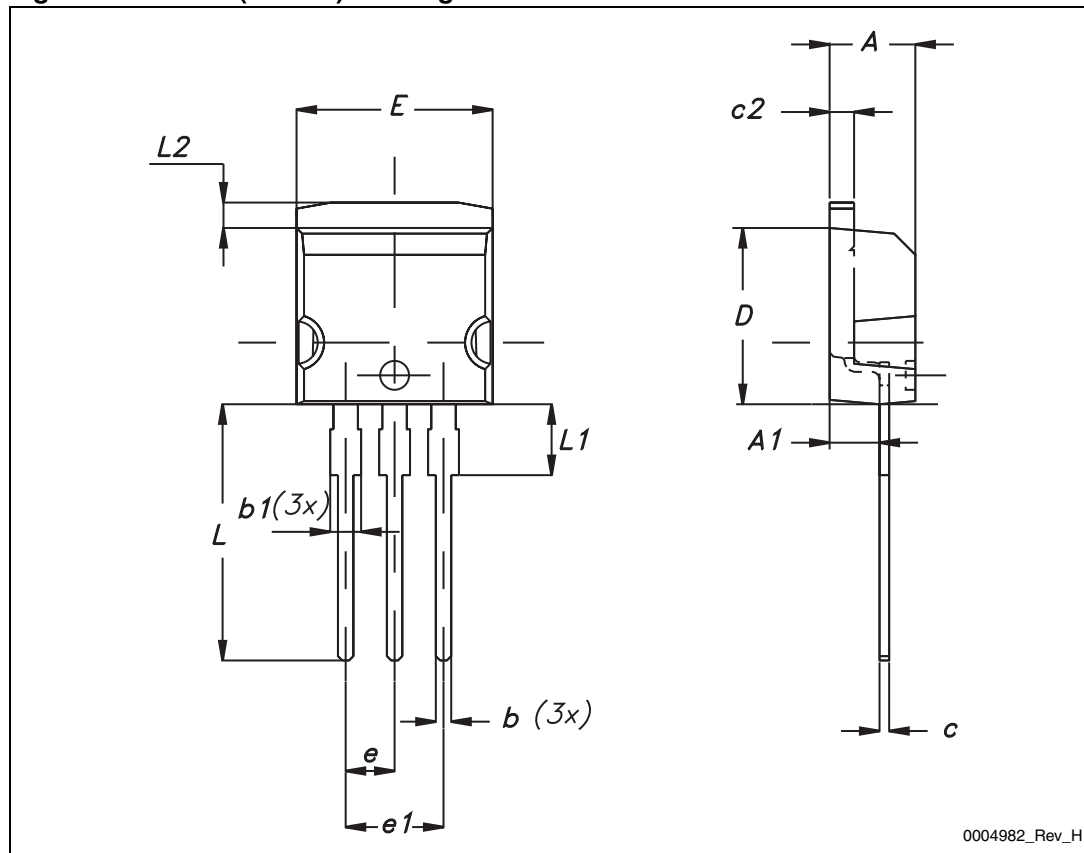


7012510_Rev_K

Table 11. I²PAK (TO-262) mechanical data

DIM.	mm.		
	min.	typ	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

Figure 25. I²PAK (TO-262) drawing



0004982_Rev_H

5 Packaging mechanical data

Table 12. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 26. Tape for DPAK (TO-252)

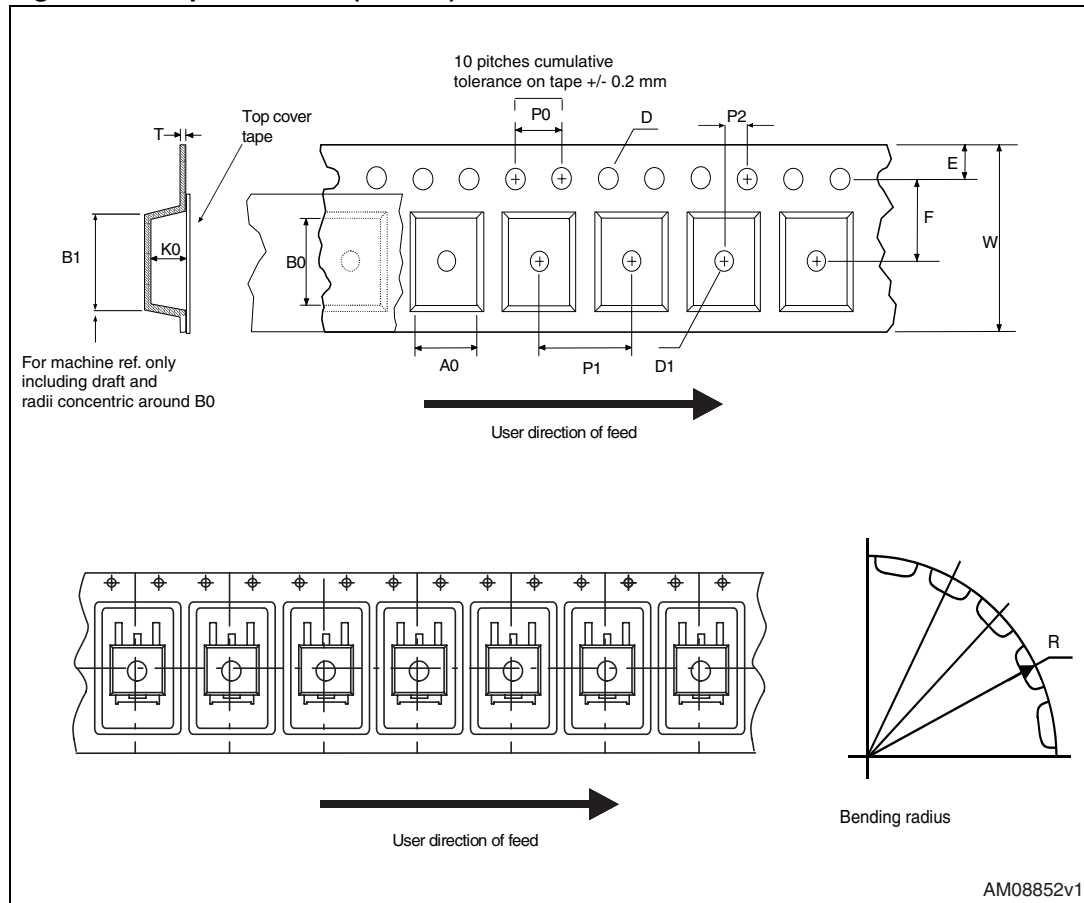
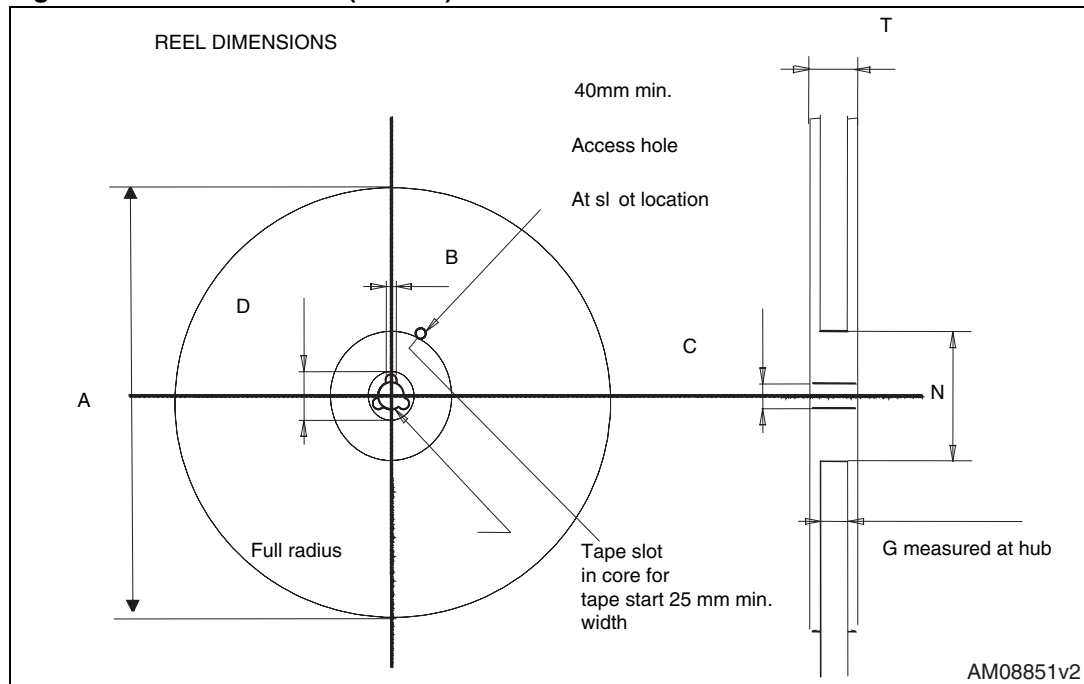


Figure 27. Reel for DPAK (TO-252)



6 Revision history

Table 13. Document revision history

Date	Revision	Changes
06-May-2009	1	First release.
28-Sep-2011	2	Inserted new device in I ² PAK. Updated tables 1 , 2 and 3 with the new package. Updated Section 4: Package mechanical data with the new package and Section 5: Packaging mechanical data . Minor text changes.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2011 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com