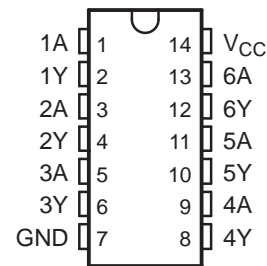


## FEATURES

- Inputs Are TTL-Voltage Compatible
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

CD54ACT05 . . . F PACKAGE  
CD74ACT05 . . . E OR M PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The 'ACT05 devices contain six independent inverters. These devices perform the Boolean function  $Y = \bar{A}$ . The open-drain outputs require pullup resistors to perform correctly, and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

### ORDERING INFORMATION

| T <sub>A</sub> | PACKAGE <sup>(1)</sup> |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|--------------|-----------------------|------------------|
| -55°C to 125°C | PDIP – E               | Tube of 25   | CD74ACT05E            | CD74ACT05E       |
|                | SOIC – M               | Tube of 50   | CD74ACT05M            | ACT05M           |
|                |                        | Reel of 2500 | CD74ACT05M96          |                  |
|                | CDIP – F               | Reel of 1000 | CD54ACT05F3A          | CD54ACT05F3A     |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### FUNCTION TABLE (EACH INVERTER)

| INPUT<br>A | OUTPUT<br>Y |
|------------|-------------|
| H          | L           |
| L          | Z           |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# CD54ACT05, CD74ACT05 HEX INVERTERS WITH OPEN-DRAIN OUTPUTS

SCHS311C—JANUARY 2001—REVISED JANUARY 2007

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|               |  | MIN                         | MAX | UNIT    |
|---------------|--|-----------------------------|-----|---------|
| $V_{CC}$      | Supply voltage range                     | -0.5                        | 6   | V       |
| $I_{IK}$      | Input clamp current <sup>(2)</sup>       | $V_I < 0$ or $V_I > V_{CC}$ |     | ±20 mA  |
| $I_{OK}$      | Output clamp current <sup>(2)</sup>      | $V_O < 0$                   |     | -50 mA  |
| $I_O$         | Continuous current                       |                             |     | ±50 mA  |
| $\theta_{JA}$ | Package thermal impedance <sup>(3)</sup> | E package                   |     | 80 °C/W |
|               |  | M package                   |     | 86      |
| $T_{stg}$     | Storage temperature range                | -65                         | 150 | °C      |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions<sup>(1)</sup>

|                     |                                    | $T_A = 25^\circ\text{C}$ |          | $-40^\circ\text{C TO } 85^\circ\text{C}$ |          | $-55^\circ\text{C TO } 125^\circ\text{C}$ |          | UNIT |
|---------------------|------------------------------------|--------------------------|----------|--|----------|---|----------|------|
|                     |                                    | MIN                      | MAX      | MIN                                      | MAX      | MIN                                       | MAX      |      |
| $V_{CC}$            | Supply voltage                     | 4.5                      | 5.5      | 4.5                                      | 5.5      | 4.5                                       | 5.5      | V    |
| $V_{IH}$            | High-level input voltage           | 2                        |          | 2  |          | 2   |          | V    |
| $V_{IL}$            | Low-level input voltage            | 0.8                      |          | 0.8                                      |          | 0.8                                       |          | V    |
| $V_I$               | Input voltage                      | 0                        | $V_{CC}$ | 0  | $V_{CC}$ | 0   | $V_{CC}$ | V    |
| $V_O$               | Output voltage                     | 0                        | 5.5      | 0  | 5.5      | 0   | 5.5      | V    |
| $I_{OL}$            | Low-level output current           | 24                       |          | 24                                       |          | 24  |          | mA   |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 10                       |          | 10                                       |          | 10  |          | ns/V |

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER       | TEST CONDITIONS                  | $V_{CC}$                        | $T_A = 25^\circ\text{C}$ |     | $-40^\circ\text{C TO } 85^\circ\text{C}$ |     | $-55^\circ\text{C TO } 125^\circ\text{C}$ |     | UNIT |
|-----------------|----------------------------------|---------------------------------|--------------------------|-----|--|-----|---|-----|------|
|                 |                                  |                                 | MIN                      | MAX | MIN                                      | MAX | MIN                                       | MAX |      |
| $V_{OL}$        | $V_I = V_{IH}$ or $V_{IL}$       | $I_{OL} = 50$ mA                | 4.5 V                    |     | 0.1                                      |     | 0.1                                       |     | V    |
|                 |                                  | $I_{OL} = 24$ mA                | 4.5 V                    |     | 0.36                                     |     | 0.44                                      |     |      |
|                 |                                  | $I_{OL} = 50$ mA <sup>(1)</sup> | 5.5 V                    |     |  |     | 1.65                                      |     |      |
|                 |                                  | $I_{OL} = 75$ mA <sup>(1)</sup> | 5.5 V                    |     |  |     | 1.65                                      |     |      |
| $I_I$           | $V_I = V_{CC}$ or GND            | 5.5 V                           | ±0.1                     |     | ±1                                       |     | ±1  |     | µA   |
| $I_{CC}$        | $V_I = V_{CC}$ or GND, $I_O = 0$ | 5.5 V                           | 4                        |     | 40                                       |     | 80  |     | µA   |
| $\Delta I_{CC}$ | $V_I = V_{CC} - 2.1$ V           | 4.5 V to 5.5 V                  | 2.4                      |     | 2.8                                      |     | 3   |     | mA   |
| $C_i$           |                                  |                                 | 10                       |     | 10                                       |     | 10  |     | pF   |

- (1) Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

**ACT INPUT LOAD TABLE<sup>(1)</sup>**

| Input | Unit Load |
|-------|-----------|
| A     | 0.18      |

(1) Unit load is  $\Delta I_{CC}$  limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

**Switching Characteristics**

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ ,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

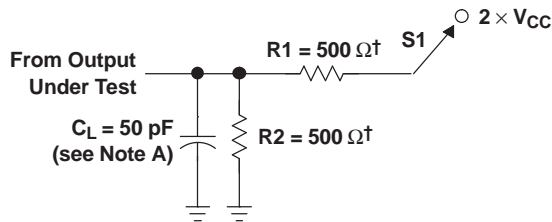
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -40°C TO 85°C |     | -55°C TO 125°C |      | UNIT |
|-----------|--------------|-------------|---------------|-----|----------------|------|------|
|           |              |             | MIN           | MAX | MIN            | MAX  |      |
| $t_{PZL}$ | A or B       | Y           | 2.4           | 8.5 | 2.3            | 9.3  | ns   |
| $t_{PLZ}$ |              |             | 2.8           | 9.8 | 2.7            | 10.8 |      |

**Operating Characteristics**

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

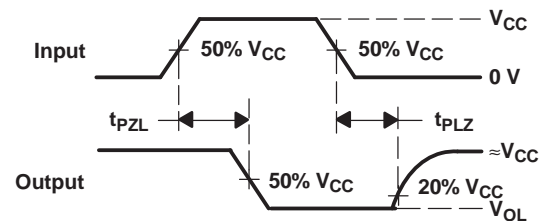
| PARAMETER                              | TYP | UNIT |
|--|-----|------|
| $C_{pd}$ Power dissipation capacitance | 105 | pF   |

**PARAMETER MEASUREMENT INFORMATION**



<sup>†</sup> When  $V_{CC} = 1.5\text{ V}$ ,  $R_1 = R_2 = 1\text{ k}\Omega$

**LOAD CIRCUIT**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .  
 C. The outputs are measured one at a time, with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-9068601QCA  | ACTIVE                | CDIP         | J               | 14   | 1           | TBD                     | A42 SNPB         | N / A for Pkg Type           |
| CD54ACT05F3A     | ACTIVE                | CDIP         | J               | 14   | 1           | TBD                     | A42 SNPB         | N / A for Pkg Type           |
| CD74ACT05E       | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| CD74ACT05EE4     | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| CD74ACT05M       | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74ACT05M96     | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74ACT05M96E4   | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74ACT05ME4     | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AB.

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