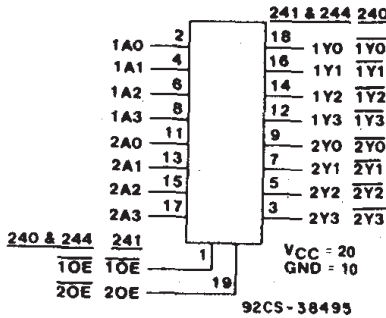


# CD54/74AC240/241/244 CD54/74ACT240/241/244



Data sheet acquired from Harris Semiconductor  
SCHS287B – Revised January 2004



### FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

The RCA CD54/74AC240, CD54/74AC241, and CD54/74AC244 and the CD54/74ACT240, CD54/74ACT241, and CD54/74ACT244 3-state octal buffer/line drivers use the RCA ADVANCED CMOS technology. The CD54/74AC/ACT240 and CD54/74AC/ACT244 have active-LOW output enables ( $\overline{1OE}$ ,  $\overline{2OE}$ ). The CD54/74AC/ACT241 has one active-LOW ( $\overline{1OE}$ ) and one active-HIGH (2OE) output enable.

The CD74AC240 and CD74ACT240 are supplied in 20-lead dual-in-line plastic packages (E suffix) and 20-lead small-outline packages (M and M96 suffixes). The CD74AC241 is supplied in 20-lead dual-in-line plastic packages (E suffix) and the CD74ACT241 is supplied in 20-lead dual-in-line plastic packages (E suffix) and 20-lead small-outline packages (M96 suffix). The CD74AC244 and CD74ACT244 are supplied in 20-lead dual-in-line plastic packages (E suffix), 20-lead small-outline packages (M and M96 suffixes), and 20-lead shrink small-outline packages (SM96 suffix). These package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC240 and CD54AC244 and the CD54ACT240, CD54ACT241, and CD54ACT244 are supplied in 20-lead hermetic dual-in-line ceramic packages (F3A suffix) and are operable over the -55 to +125°C temperature range.

## Octal Buffer/Line Drivers, 3-State

- CD54/74AC/ACT240 - Inverting
- CD54/74AC/ACT241 - Non-Inverting
- CD54/74AC/ACT244 - Non-Inverting

### Type Features:

- Buffered inputs
- Typical propagation delay:  
3.6 ns @  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 50 pF$

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latch-up-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24$ -mA output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

### TRUTH TABLES

INPUTS		OUTPUT	
$\overline{1OE}$ , $\overline{2OE}$	A	Y	
L	L	H	
L	H	L	
H	X	Z	

(AC/ACT240)

INPUTS		OUTPUT	
$\overline{1OE}$ , $\overline{2OE}$	A	Y	
L	L	L	
L	H	H	
H	X	Z	

(AC/ACT244)

INPUTS		OUTPUT		INPUTS		OUTPUT	
$\overline{1OE}$	1A	1Y	2OE	2A	2Y		
L	L	L	L	X	Z		
L	H	H	H	L	L		
H	X	Z	H	H	H		

(AC/ACT241)

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = HIGH Impedance

This data sheet is applicable to the CD54/74AC240, CD54ACT240, and CD54/74ACT241. The CD54/74AC241 were not acquired from Harris Semiconductor. See SCHS244 for information on the CD74ACT240, CD74AC244, and CD74ACT244.

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# CD54/74AC240/241/244 CD54/74ACT240/241/244

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*
<b>POWER DISSIPATION PER PACKAGE (<math>P_D</math>):</b>	
For $T_A = -40$ to $+85^\circ\text{C}$ (Package Type E)	500 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (Package Type M)	400 mW
For $T_A = +70$ to $+85^\circ\text{C}$ (Package Type M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 310 mW
<b>OPERATING-TEMPERATURE RANGE (<math>T_A</math>):</b>	
CD54	-55 to $+125^\circ\text{C}$
CD74	-40 to $+85^\circ\text{C}$
<b>STORAGE TEMPERATURE (<math>T_{Stg}</math>)</b>	
	-65 to $+150^\circ\text{C}$
<b>LEAD TEMPERATURE (DURING SOLDERING):</b>	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum.	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only.	$+300^\circ\text{C}$

\* For up to 4 outputs per device: add  $\pm 25$  mA for each additional output.

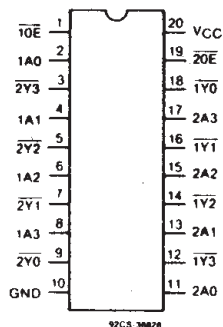
**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

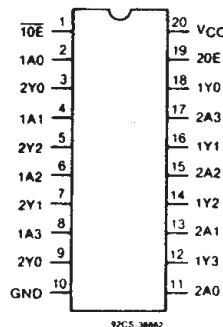
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A =$ Full Package-Temperature Range) AC Types ACT Types	1.5	5.5	V
	4.5	5.5	V
DC Input or Output Voltage, $V_I, V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$	CD54	$+125$	$^\circ\text{C}$
	CD74	$+85$	
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0	50	ns/V
	0	20	ns/V
	0	10	ns/V

\* Unless otherwise specified, all voltages are referenced to ground.

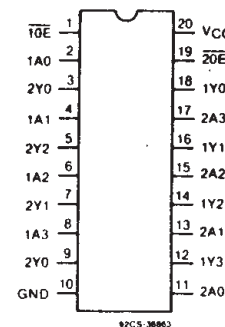
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**CD54/74AC, ACT240 TYPES  
TERMINAL ASSIGNMENT**



**CD54/74AC, ACT241 TYPES  
TERMINAL ASSIGNMENT**



**CD54/74AC, ACT244 TYPES  
TERMINAL ASSIGNMENT**

# CD54/74AC240/241/244 CD54/74ACT240/241/244

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
		-75	5.5	—	—	3.85	—	—	—	
Low-Level Output Voltage V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
		75	5.5	—	—	—	1.65	—	—	
Input Leakage Current I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

# CD54/74AC240/241/244

## CD54/74ACT240/241/244

### STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS	
				+25		-40 to +85		-55 to +125			
	V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V <sub>IH</sub>		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	V <sub>IL</sub>		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	V <sub>OH</sub>	$\left. \begin{array}{l} V_{IH} \text{ or } V_{IL} \\ \# , * \end{array} \right\}$	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	$\left. \begin{array}{l} V_{IH} \text{ or } V_{IL} \\ \# , * \end{array} \right\}$	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

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#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

### ACT INPUT LOADING TABLES

CD54/74ACT240	
INPUT	UNIT LOADS*
nA0 - A3	1.42
10E	0.83
20E	0.83

CD54/74ACT241	
INPUT	UNIT LOADS*
nA0 - A3	0.5
10E	0.83
20E	1.67

CD54/74ACT244	
INPUT	UNIT LOADS*
nA0 - A3	0.5
10E	0.83
20E	0.83

\*Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC240/241/244

## CD54/74ACT240/241/244

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Outputs AC240	$t_{PLH}$	1.5	—	82	—	90	ns
	$t_{PHL}$	3.3*	2.6	9.2	2.5	10.1	
AC241, 244	$t_{PLH}$	1.5	—	93	—	103	ns
	$t_{PHL}$	3.3	3	10.5	2.9	11.5	
Output Enable Times	$t_{PZL}$	1.5	—	136	—	150	ns
	$t_{PZH}$	3.3	4.6	16.4	4.5	18	
Output Disable Times	$t_{PLZ}$	1.5	—	136	—	150	ns
	$t_{PHZ}$	3.3	3.9	13.6	3.8	15	
Power Dissipation Capacitance AC240 AC241, 244	$C_{PD}\ddagger$	—	65 Typ.		65 Typ.		pF
		—	71 Typ.		71 Typ.		
Min. (Valley) $V_{OH}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OHV}$ See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) $V_{OL}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OLP}$ See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	$C_i$	—	—	10	—	10	pF
3-State Output Capacitance	$C_o$	—	—	15	—	15	pF

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Outputs ACT240	$t_{PLH}$	5†	2.3	7.8	2.2	8.6	ns
	$t_{PHL}$	5	2.5	8.7	2.4	9.6	
ACT241, 244	$t_{PLH}$	5	2.5	8.7	2.4	9.6	ns
	$t_{PHL}$	5	2.5	8.7	2.4	9.6	
Output Enable Times	$t_{PZL}$	5	3.5	12.2	3.4	13.4	ns
	$t_{PZH}$	5	3.5	12.2	3.4	13.4	
Output Disable Times	$t_{PLZ}$	5	3.5	12.2	3.4	13.4	ns
	$t_{PHZ}$	5	3.5	12.2	3.4	13.4	
Power Dissipation Capacitance ACT240 ACT241, 244	$C_{PD}\ddagger$	—	65 Typ.		65 Typ.		pF
		—	71 Typ.		71 Typ.		
Min. (Valley) $V_{OH}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OHV}$ See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) $V_{OL}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OLP}$ See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	$C_i$	—	—	10	—	10	pF
3-State Output Capacitance	$C_o$	—	—	15	—	15	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

‡ $C_{PD}$  is used to determine the dynamic power consumption, per package.

For AC series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

For ACT series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency

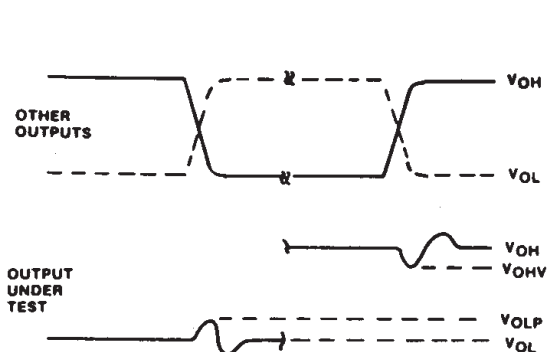
$C_L$  = output load capacitance

$V_{CC}$  = supply voltage.

# Technical Data

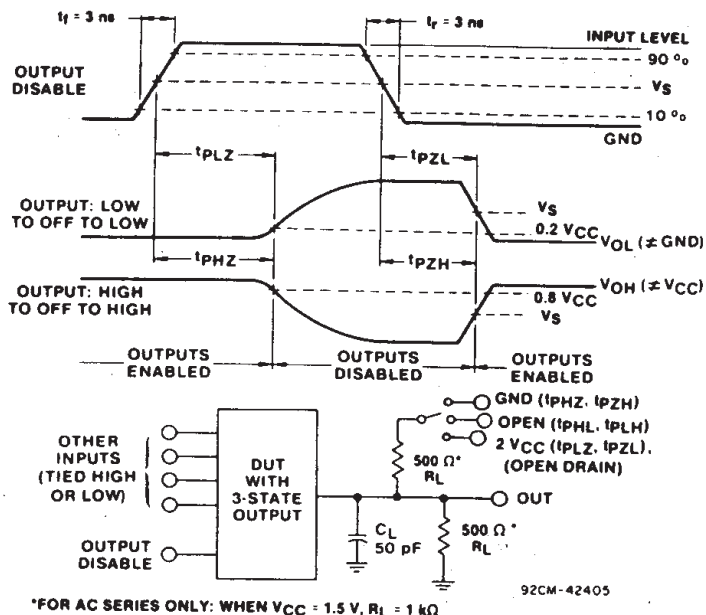
## CD54/74AC240/241/244 CD54/74ACT240/241/244

### PARAMETER MEASUREMENT INFORMATION



- NOTES:**
1.  $V_{OHV}$  and  $V_{OLP}$  ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
  2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:  
PRR  $\leq$  1 MHz,  $t_r = 3$  ns,  $t_f = 3$  ns, SKEW 1 ns.
  3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH  $0.1 \mu\text{F}$  CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406

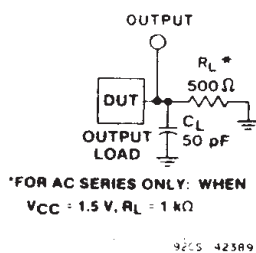


92CM-42405

\*FOR AC SERIES ONLY: WHEN  $V_{CC} = 1.5$  V,  $R_L = 1$  k $\Omega$

Fig. 1 - Simultaneous switching transient waveforms.

Fig. 2 - Three-state propagation delay times and test circuit.



\*FOR AC SERIES ONLY: WHEN  $V_{CC} = 1.5$  V,  $R_L = 1$  k $\Omega$

92CS-42389

92CS-42407

Fig. 3 - Propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	$0.5 V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	$0.5 V_{CC}$	$0.5 V_{CC}$

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**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD54AC240F3A	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
CD54AC244F3A	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
CD54ACT240F3A	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
CD54ACT241F3A	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
CD54ACT244F3A	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
CD74AC240E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74AC240M	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CD74AC240M96	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CD74AC244E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74AC244M	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CD74AC244M96	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CD74AC244SM	OBSOLETE	SSOP	DB	20		Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD74AC244SM96	ACTIVE	SSOP	DB	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD74ACT240E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74ACT240M	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CD74ACT240M96	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CD74ACT241E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74ACT241M96	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CD74ACT244E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74ACT244M	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CD74ACT244M96	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CD74ACT244SM	OBSOLETE	SSOP	DB	20		Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD74ACT244SM96	ACTIVE	SSOP	DB	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



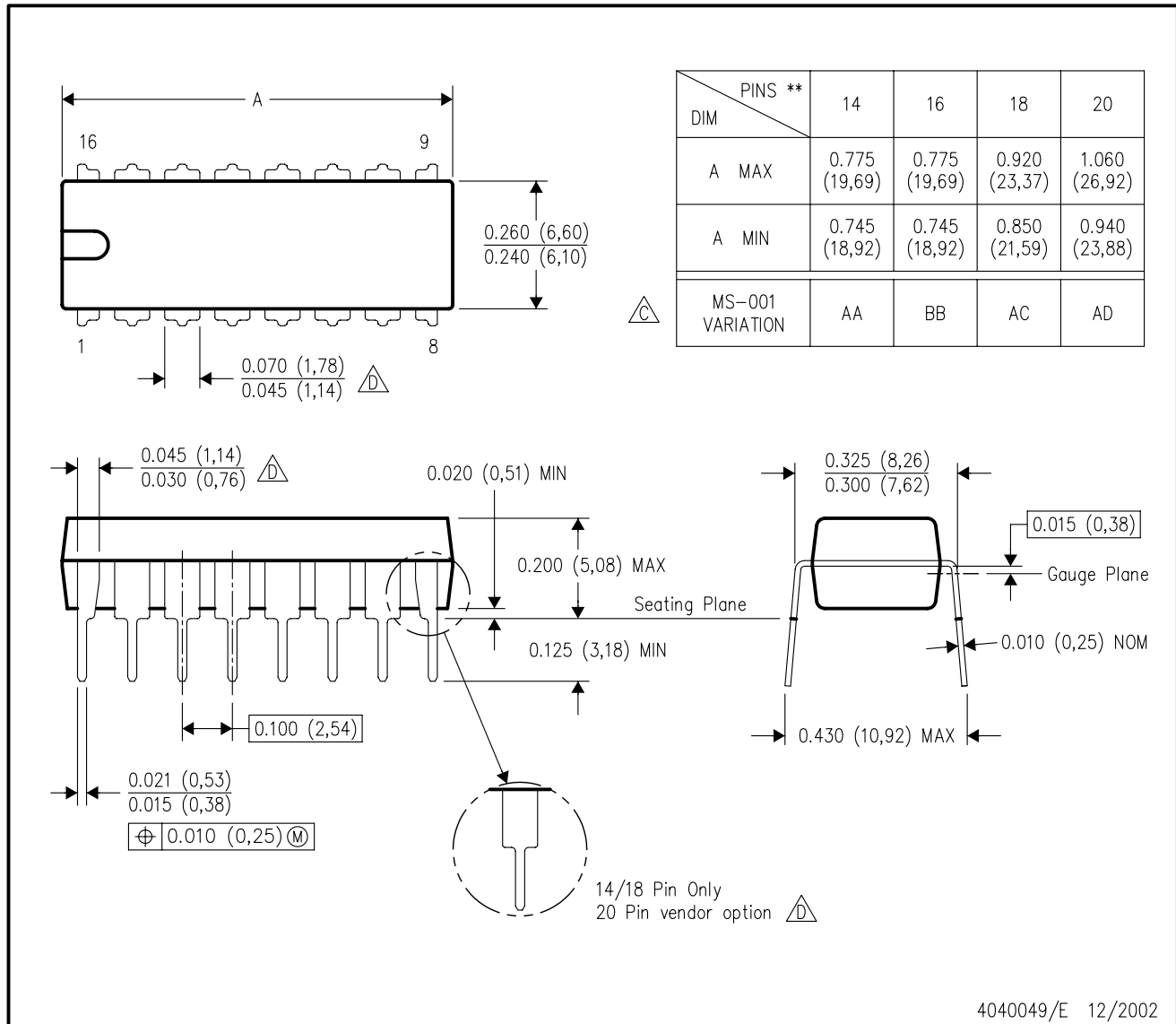
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

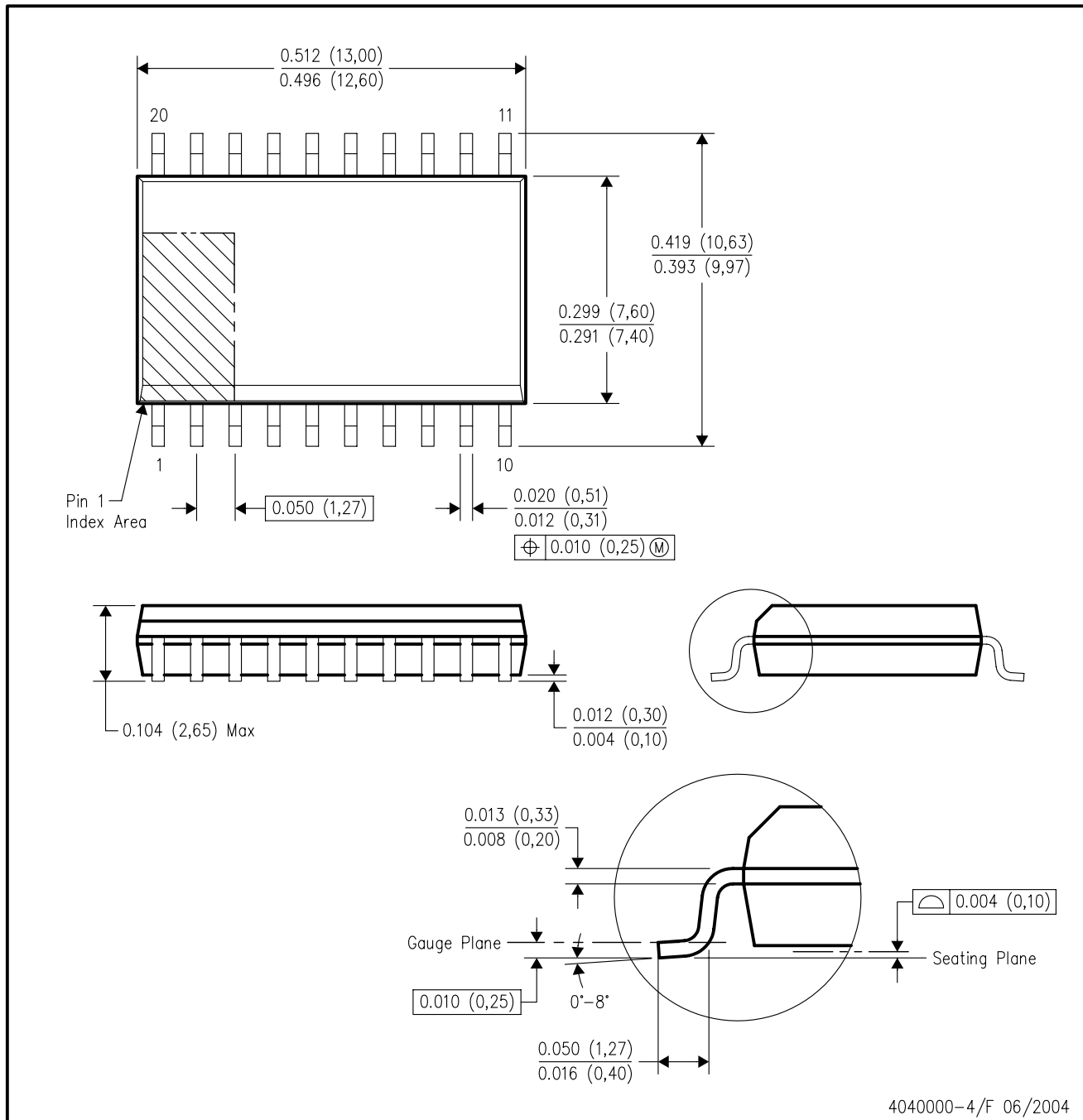


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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