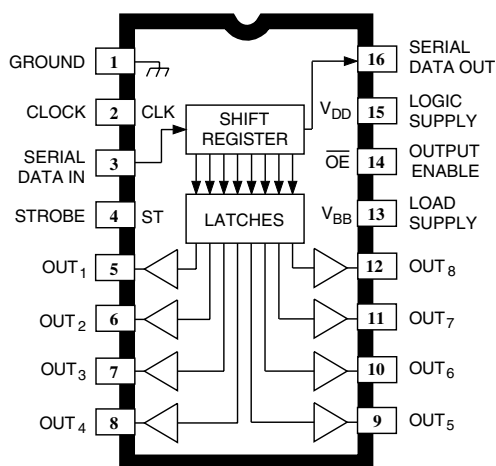


# 5890 AND 5891

## BIMOS II 8-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS



Dwg. PP-026-2A

Note the suffix 'A' devices (DIP) and the suffix 'LW' devices (SOIC) are electrically identical and share a common terminal number assignment.

### ABSOLUTE MAXIMUM RATINGS at $T_A = +25^\circ\text{C}$

Output Voltage, $V_{OUT}$	
(UCN5890A & UCN5890LW) .....	80 V
(UCN5891A & UCN5891LW) .....	50 V
Logic Supply Voltage Range,	
$V_{DD}$ .....	4.5 V to 15 V
Driver Supply Voltage Range, $V_{BB}$	
(UCN5890A/LW) .....	20 V to 80 V
(UCN5891A/LW) .....	5.0 V to 50 V
Input Voltage Range,	
$V_{IN}$ .....	-0.3 V to $V_{DD} + 0.3$ V
Continuous Output Current,	
$I_{OUT}$ .....	-500 mA
Allowable Package Power Dissipation,	
$P_D$ .....	See Graph
Operating Temperature Range,	
$T_A$ .....	-20°C to +85°C
Storage Temperature Range,	
$T_S$ .....	-55°C to +150°C

Caution: CMOS devices have input static protection, but are susceptible to damage when exposed to extremely high static electrical charges.

Frequently applied in non-impact printer systems, the UCN5890A, UCN5890LW, UCN5891A, and UCN5891LW are BiMOS II serial-input, latched source (high-side) drivers. The octal, high-current smart-power ICs merge an 8-bit CMOS shift register, associated CMOS latches, and CMOS control logic (strobe and output enable) with sourcing power Darlington outputs. Typical applications include multiplexed LED and incandescent displays, relays, solenoids, and similar peripheral loads to a maximum of -500 mA per output.

Except for output voltage ratings, these smart high-side driver ICs are equivalent. The UCN5890A/LW are rated for operation with load supply voltages of 20 V to 80 V and a minimum output sustaining voltage of 50 V. The UCN5891A/LW are optimized for operation with supply voltages of 5 V to 50 V (35 V sustaining).

BiMOS II devices have higher data-input rates than the original BiMOS circuits. With a 5 V supply, they will operate to at least 3.3 MHz. At 12 V, higher speeds are possible. The CMOS inputs are compatible with standard CMOS and NMOS logic levels. TTL circuits may require the use of appropriate pull-up resistors to ensure a proper input-logic high. A CMOS serial data output, allows cascading these devices in multiple drive-line applications required by many dot matrix, alphanumeric, and bar graph displays.

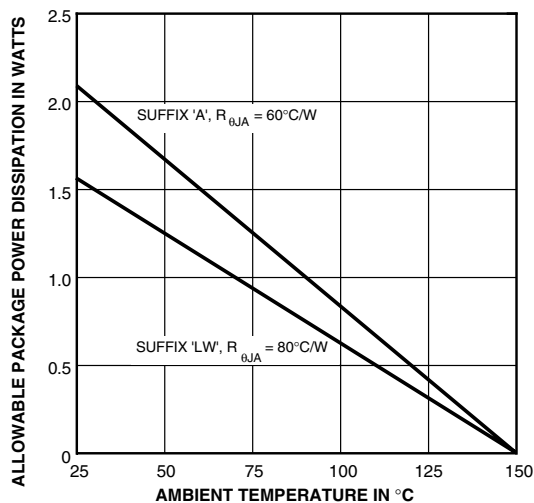
Suffix 'A' devices are supplied in a standard dual in-line plastic package with copper lead frame for enhanced package power dissipation characteristics. Suffix 'LW' devices are supplied in a standard wide-body SOIC package for surface-mount applications. Similar driver, featuring reduced output saturation voltage, are the UCN5895A and A5895SLW. Complementary, 8-bit serial-input, latched sink drivers are the Series UCN5820A.

### FEATURES

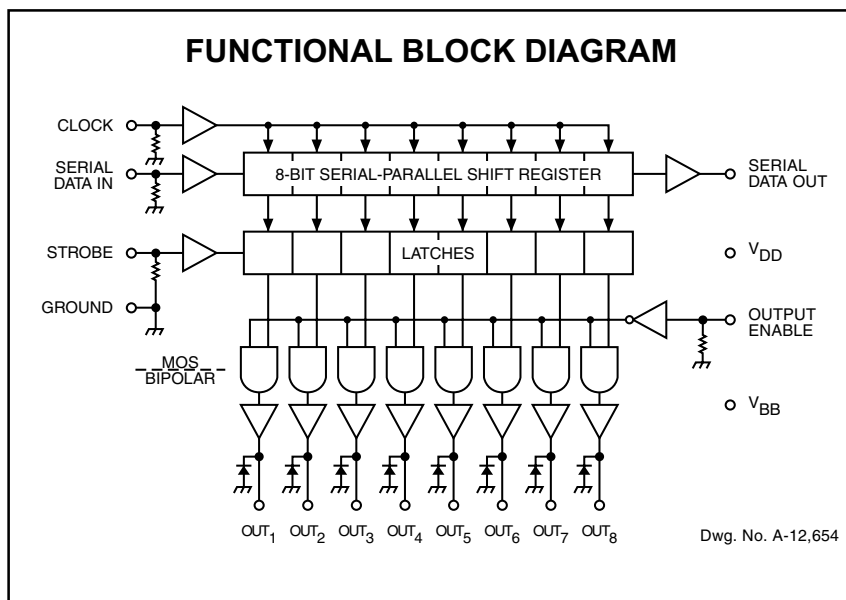
- 50 V or 80 V Source Outputs
- Output Current to -500 mA
- Output Transient-Suppression Diodes
- To 3.3 MHz Data-Input Rate
- Low-Power CMOS Logic and Latches

Always order by complete part number, e.g., UCN5891LW.

# 5890 AND 5891 8-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS

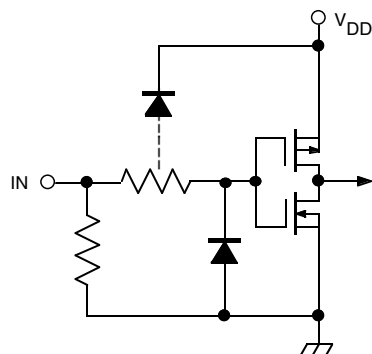


Dwg. GP-018B



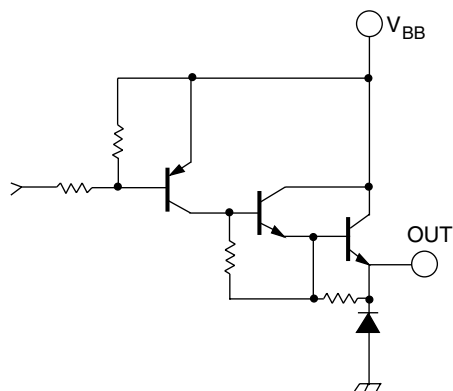
Dwg. No. A-12,654

## TYPICAL INPUT CIRCUIT



Dwg. EP-010-4A

## TYPICAL OUTPUT DRIVER



Dwg. No. A-12,648

Number of Outputs On at $I_{OUT} = -200\text{ mA}$	UCN5890/91A Max. Allowable Duty Cycle at $T_A$ of		
	50°C	60°C	70°C
8	53%	47%	41%
7	60%	54%	48%
6	70%	64%	56%
5	83%	75%	67%
4	100%	94%	84%
3	100%	100%	100%
2	100%	100%	100%
1	100%	100%	100%

Number of Outputs On at $I_{OUT} = -200\text{ mA}$	UCN5890/91LW Max. Allowable Duty Cycle at $T_A$ of		
	50°C	60°C	70°C
8	40%	35%	31%
7	45%	41%	36%
6	53%	48%	42%
5	62%	56%	50%
4	80%	71%	62%
3	100%	96%	84%
2	100%	100%	100%
1	100%	100%	100%

# 5890 AND 5891 8-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS

**ELECTRICAL CHARACTERISTICS at  $T_A = +25^\circ\text{C}$ ,  $V_{BB} = 80\text{ V}$  (UCN5890A/LW) or  $50\text{ V}$  (UCN5891A/LW),  $V_{DD} = 5\text{ V}$  and  $12\text{ V}$  (unless otherwise noted).**

Characteristic	Symbol	$V_{BB}$	Test Conditions	Limits		
				Min.	Max.	Units
Output Leakage Current	$I_{CEX}$	Max.	$T_A = +25^\circ\text{C}$	—	-50	$\mu\text{A}$
			$T_A = +70^\circ\text{C}$	—	-100	$\mu\text{A}$
Output Saturation Voltage	$V_{CE(SAT)}$	50 V	$I_{OUT} = -100\text{ mA}$	—	1.8	V
			$I_{OUT} = -225\text{ mA}$	—	1.9	V
			$I_{OUT} = -350\text{ mA}$	—	2.0	V
Output Sustaining Voltage	$V_{CE(sus)}$	Max.	$I_{OUT} = -350\text{ mA}$ , $L = 2\text{ mH}$ , UCN5891A/LW	35	—	V
			$I_{OUT} = -350\text{ mA}$ , $L = 2\text{ mH}$ , UCN5890A/LW	50	—	V
Input Voltage	$V_{IN(1)}$	50 V	$V_{DD} = 5.0\text{ V}$	3.5	5.3	V
			$V_{DD} = 12\text{ V}$	10.5	12.3	V
	$V_{IN(0)}$	50 V	$V_{DD} = 5\text{ V to }12\text{ V}$	-0.3	+0.8	V
Input Current	$I_{IN(1)}$	50 V	$V_{DD} = V_{IN} = 5.0\text{ V}$	—	50	$\mu\text{A}$
			$V_{DD} = V_{IN} = 12\text{ V}$	—	240	$\mu\text{A}$
Input Impedance	$Z_{IN}$	50 V	$V_{DD} = 5.0\text{ V}$	100	—	$\text{k}\Omega$
			$V_{DD} = 12\text{ V}$	50	—	$\text{k}\Omega$
Max. Clock Frequency	$f_C$	50 V		3.3*	—	MHz
Serial Data Output Resistance	$R_{OUT}$	50 V	$V_{DD} = 5.0\text{ V}$	—	20	$\text{k}\Omega$
			$V_{DD} = 12\text{ V}$	—	6.0	$\text{k}\Omega$
Turn-On Delay	$t_{PLH}$	50 V	Output Enable to Output, $I_{OUT} = -350\text{ mA}$	—	2.0	$\mu\text{s}$
Turn-Off Delay	$t_{PHL}$	50 V	Output Enable to Output, $I_{OUT} = -350\text{ mA}$	—	10	$\mu\text{s}$
Supply Current	$I_{BB}$	50 V	All outputs on, All outputs open	—	10	$\text{mA}$
			All outputs off	—	200	$\mu\text{A}$
	$I_{DD}$	50 V	$V_{DD} = 5\text{ V}$ , All outputs off, Inputs = 0 V	—	100	$\mu\text{A}$
			$V_{DD} = 12\text{ V}$ , All outputs off, Inputs = 0 V	—	200	$\mu\text{A}$
			$V_{DD} = 5\text{ V}$ , One output on, All Inputs = 0 V	—	1.0	$\text{mA}$
$V_{DD} = 12\text{ V}$ , One output on, All Inputs = 0 V	—	3.0	$\text{mA}$			
Diode Leakage Current	$I_R$	Max.	$T_A = +25^\circ\text{C}$	—	50	$\mu\text{A}$
			$T_A = +70^\circ\text{C}$	—	100	$\mu\text{A}$
Diode Forward Voltage	$V_F$	Open	$I_F = 350\text{ mA}$	—	2.0	V

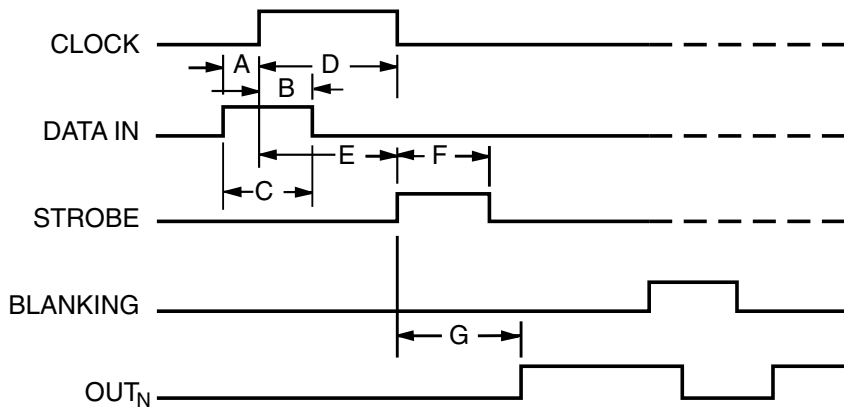
NOTES: Turn-off delay is influenced by load conditions. Systems applications well below the specified output loading may require timing considerations for some designs, i.e., multiplexed displays or when used in combination with sink drivers in a totem pole configuration.

Positive (negative) current is defined as going into (coming out of) the specified device pin.

\* Operation at a clock frequency greater than the specified minimum value is possible but not warranted.

# 5890 AND 5891

## 8-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS



Dwg. No. A-12,649A

### TIMING REQUIREMENTS

( $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5\text{ V}$ , Logic Levels are  $V_{DD}$  and Ground)

- A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) ..... **75 ns**
- B. Minimum Data Active Time After Clock Pulse (Data Hold Time) ..... **75 ns**
- C. Minimum Data Pulse Width ..... **150 ns**
- D. Minimum Clock Pulse Width ..... **150 ns**
- E. Minimum Time Between Clock Activation and Strobe ..... **300 ns**
- F. Minimum Strobe Pulse Width ..... **100 ns**
- G. Typical Time Between Strobe Activation and Output Transition ..... **500 ns**

Timing is representative of a 3.3 MHz clock. Higher speeds may be attainable with increased supply voltage; operation at high temperatures will reduce the specified maximum clock frequency.

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (off) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

### TRUTH TABLE

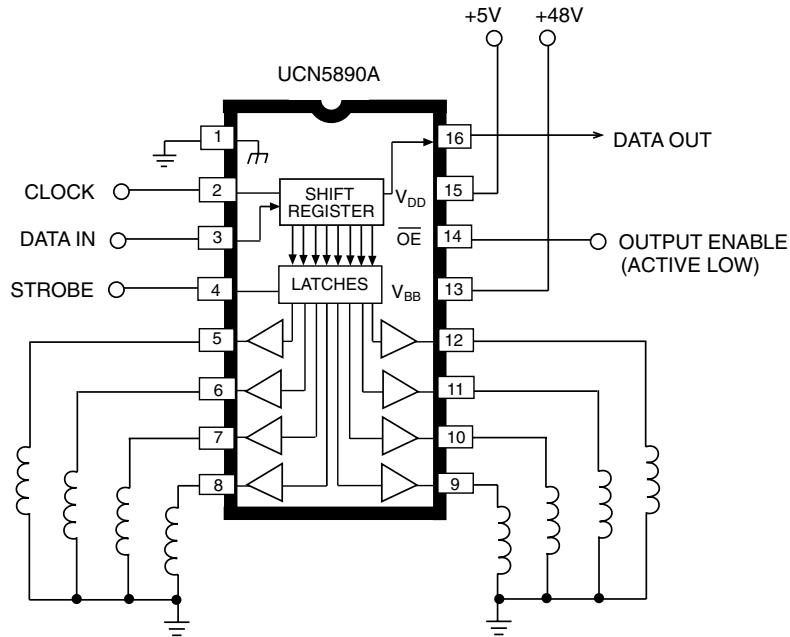
Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Output Enable	Output Contents					
		I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	...	I <sub>N-1</sub>	I <sub>N</sub>			I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	...	I <sub>N-1</sub>	I <sub>N</sub>		I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	...	I <sub>N-1</sub>	I <sub>N</sub>
H	┌	H	R <sub>1</sub>	R <sub>2</sub>	...	R <sub>N-2</sub>	R <sub>N-1</sub>	R <sub>N-1</sub>														
L	┐	L	R <sub>1</sub>	R <sub>2</sub>	...	R <sub>N-2</sub>	R <sub>N-1</sub>	R <sub>N-1</sub>														
X	└	R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	...	R <sub>N-1</sub>	R <sub>N</sub>	R <sub>N</sub>														
		X	X	X	...	X	X	X	L	R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	...	R <sub>N-1</sub>	R <sub>N</sub>							
		P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	...	P <sub>N-1</sub>	P <sub>N</sub>	P <sub>N</sub>	H	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	...	P <sub>N-1</sub>	P <sub>N</sub>	L						
							X	X	X	...	X	X	H	L	L	L						

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State



# 5890 AND 5891 8-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS

## TYPICAL APPLICATION SOLENOID OR RELAY DRIVER



Dwg. No. A-12,548

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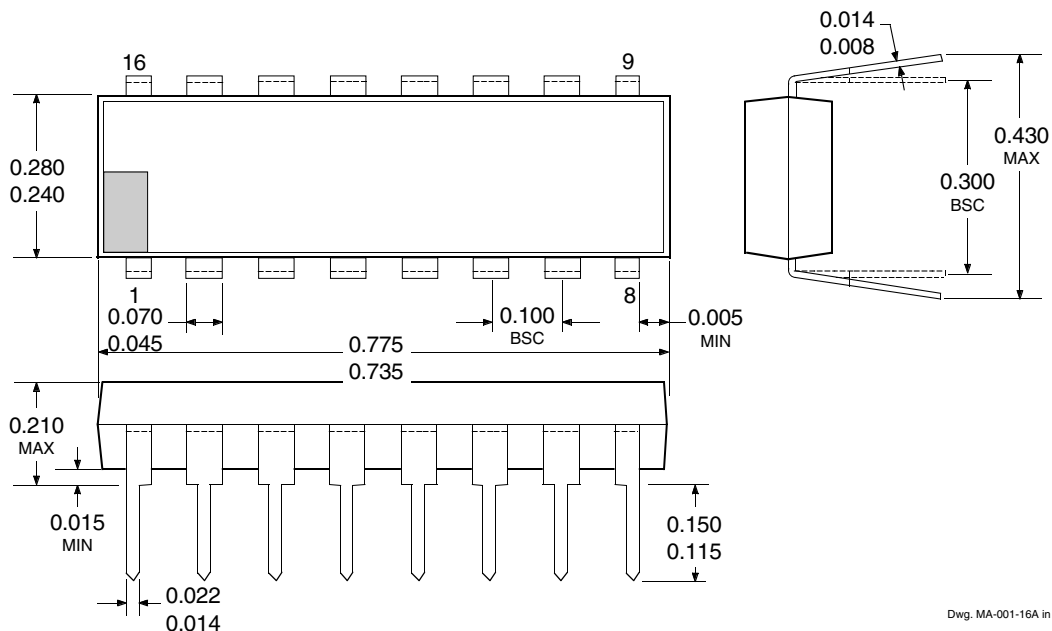
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# 5890 AND 5891 8-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS

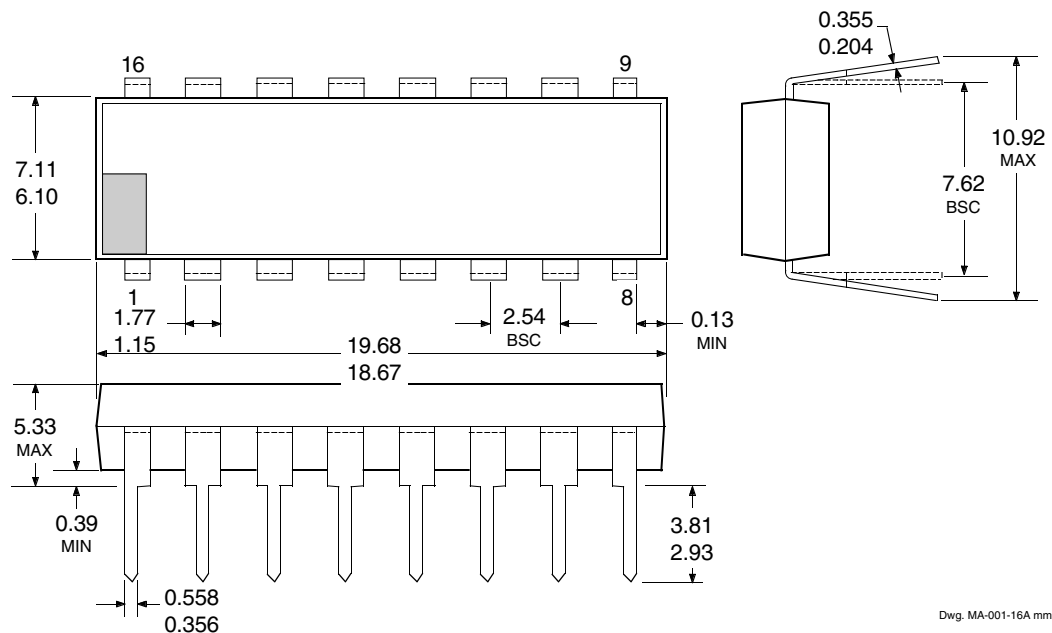
## UCN5890A and UCN5891A

Dimensions in Inches  
(controlling dimensions)



Dwg. MA-001-16A in

Dimensions in Millimeters  
(for reference only)



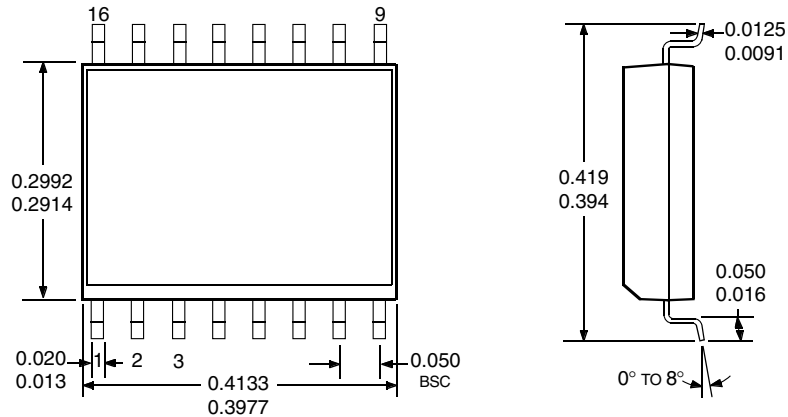
Dwg. MA-001-16A mm

- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.  
2. Lead spacing tolerance is non-cumulative.  
3. Lead thickness is measured at seating plane or below.  
4. Supplied in standard sticks/tubes of 25 devices.

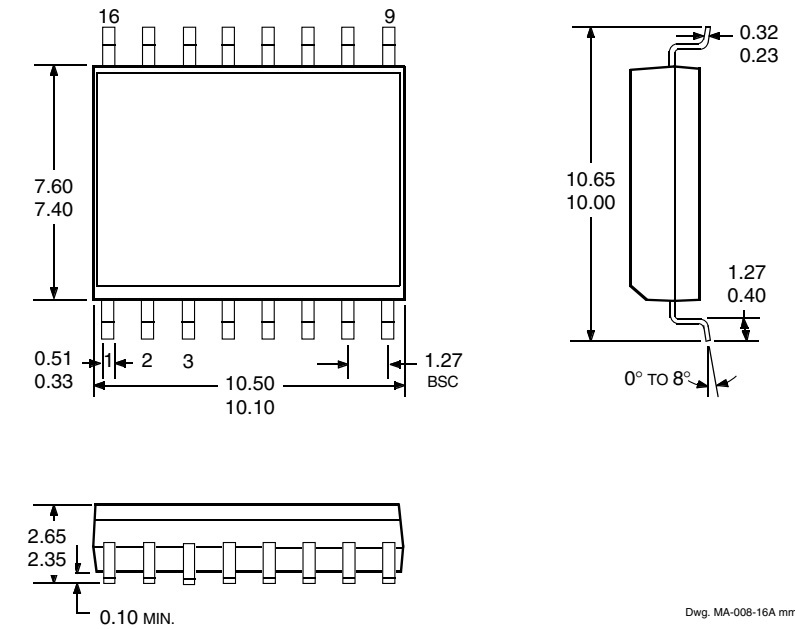
# 5890 AND 5891 8-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS

## UCN5890LW and UCN5891LW

Dimensions in Inches  
(for reference only)



Dimensions in Millimeters  
(controlling dimensions)



- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.  
2. Lead spacing tolerance is non-cumulative.  
3. Supplied in standard sticks/tubes of 47 devices or add "TR" to part number for tape and reel.

**5890 AND 5891**  
**8-BIT SERIAL-INPUT,**  
**LATCHED SOURCE DRIVERS**

**POWER**  
**INTERFACE DRIVERS**

Function	Output Ratings*		Part Number†
<b>SERIAL-INPUT LATCHED DRIVERS</b>			
8-Bit (saturated drivers)	-120 mA	50 V‡	5895
8-Bit	350 mA	50 V	5821
8-Bit	350 mA	80 V	5822
8-Bit	350 mA	50 V‡	5841
8-Bit	350 mA	80 V‡	5842
8-Bit (constant-current LED driver)	75 mA	17 V	6275
8-Bit (DMOS drivers)	250 mA	50 V	6595
8-Bit (DMOS drivers)	350 mA	50 V‡	6A595
8-Bit (DMOS drivers)	100 mA	50 V	6B595
10-Bit (active pull-downs)	-25 mA	60 V	5810-F and 6809/10
12-Bit (active pull-downs)	-25 mA	60 V	5811 and 6811
16-Bit (constant-current LED driver)	75 mA	17 V	6276
20-Bit (active pull-downs)	-25 mA	60 V	5812-F and 6812
32-Bit (active pull-downs)	-25 mA	60 V	5818-F and 6818
32-Bit	100 mA	30 V	5833
32-Bit (saturated drivers)	100 mA	40 V	5832
<b>PARALLEL-INPUT LATCHED DRIVERS</b>			
4-Bit	350 mA	50 V‡	5800
8-Bit	-25 mA	60 V	5815
8-Bit	350 mA	50 V‡	5801
8-Bit (DMOS drivers)	100 mA	50 V	6B273
8-Bit (DMOS drivers)	250 mA	50 V	6273
<b>SPECIAL-PURPOSE DEVICES</b>			
Unipolar Stepper Motor Translator/Driver	1.25 A	50 V‡	5804
Addressable 8-Bit Decoder/DMOS Driver	250 mA	50 V	6259
Addressable 8-Bit Decoder/DMOS Driver	350 mA	50 V‡	6A259
Addressable 8-Bit Decoder/DMOS Driver	100 mA	50 V	6B259
Addressable 28-Line Decoder/Driver	450 mA	30 V	6817

\* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits. Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Internal transient-suppression diodes included for inductive-load protection.

