2.25-MHz, 600-mA Step-Down Converter in TSOT and 2 × 2 × 0.8-mm QFN Package

Check for Samples: TPS62560, TPS62561, TPS62562

FEATURES

- **Output Current up to 600 mA**
- **V_{IN} Range from 2.5 V to 5.5 V**
- **Output Voltage Accuracy in PWM Mode ±2.5%**
- **Typical 15-μA Quiescent Current**
- **100% Duty Cycle for Lowest Dropout**
- **Soft Start**
- **Available in a Small TSOT, and 2 mm × 2 mm × 0.8 mm QFN Package**
- **For Improved Features Set, see TPS62260**

APPLICATIONS

- **PDAs, Pocket PCs, Portable Media Players**
- **Low-Power DSP Supply**
- **POL Applications**

DESCRIPTION

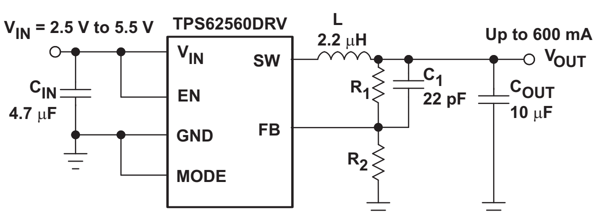
The TPS62560 device is a high efficiency synchronous step down converter, optimized for battery powered portable applications. It provides up to 1000-mA output current from batteries, such as single Li-Ion or other common chemistry AA and AAA cells.

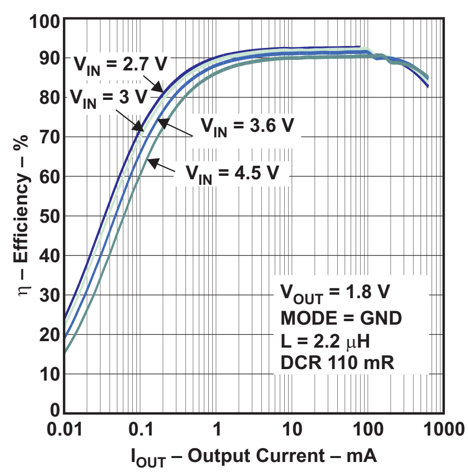
With an input voltage range of 2.5 V to 5.5 V, the device is targeted to power a large variety of portable handheld equipment or POL applications.

The TPS62560 family operates at 2.25-MHz fixed switching frequency and enters a Power Save Mode operation at light load currents to maintain a high efficiency over the entire load current range.

The Power Save Mode is optimized for low output voltage ripple. For low noise applications, the device can be forced into fixed frequency PWM mode by pulling the MODE pin high. In the shutdown mode the current consumption is reduced to less than 1 μA. The TPS62560 allows the use of small inductors and capacitors to achieve a small solution size.

TPS62560 and TPS62562 are available in a 2-mm × 2-mm, 6-terminal QFN package, whereas the TPS62561 is available in a 5-terminal TSOT23 package.





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

T_A	PART NUMBER(1)	OUTPUT VOLTAGE(2)	PACKAGE(3)	PACKAGE DESIGNATOR	ORDERING	PACKAGE MARKING
–40°C to 85°C	TPS62560	Adjustable	QFN 2×2-6	DRV	TPS62560DRV	CEY
–40°C to 85°C	TPS62561	Adjustable	TSOT-23-5	DDC	TPS62561DDC	CVO
–40°C to 85°C	TPS62562	1.8-V fixed	QFN 2×2-6	DRV	TPS62562DRV	NXT

(1) The DRV (2-mm x 2-mm 6-terminal QFN) and the DDC (TSOT-23-5) packages are available in tape on reel. Add R suffix to order quantities of 3000 parts per reel and T suffix to order quantities with 250 parts per reel.
(2) Contact TI for other fixed-output-voltage options.
(3) For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
	Input voltage range(2)		–0.3 to 7	V
	Voltage range at EN, MODE		–0.3 to V_{IN} +0.3, ≤ 7	
	Voltage on SW		–0.3 to 7	
	Peak output current		Internally limited	A
	ESD rating(3)	HBM human-body model	2	kV
		CDM charged-device model	1	
		Machine model	200	V
T_J	Maximum operating junction temperature		–40 to 125	°C
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.
(3) The human-body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each terminal. The machine model is a 200-pF capacitor discharged directly into each terminal.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$	POWER RATING FOR T_A ≤ 25°C	DERATING FACTOR ABOVE T_A = 25°C
DRV	76°C/W	1300 mW	13 mW/°C
DDC	250°C/W	400 mW	4 mW/°C

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage	2.5		5.5	V
	Output voltage range for adjustable voltage	0.85		V_{IN}	V
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6 V. External components C_{IN} = 4.7 µF 0603, C_{OUT} = 10 µF 0603, L = 2.2 µH; see the Parameter Measurement Information section.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.5		5.5	V
I_{OUT}	Output current	V_{IN} 2.5 V to 5.5 V			600	mA
I_Q	Operating quiescent current	I_{OUT} = 0 mA, PFM mode enabled (MODE = GND), device not switching		15		µA
		I_{OUT} = 0 mA, PFM mode enabled (MODE = GND), device switching, V_{OUT} = 1.8 V, See (1)		18.5		µA
		I_{OUT} = 0 mA, switching with no load (MODE = V_{IN}), PWM operation, V_{OUT} = 1.8 V, V_{IN} = 3 V		3.8		mA
I_{SD}	Shutdown current	EN = GND		0.5		µA
UVLO	Undervoltage lockout threshold	Falling		1.85		V
		Rising		1.95		V
ENABLE, MODE						
V_{IH}	High-level input voltage, EN, MODE	2 V ≤ V_{IN} ≤ 5.5 V	1		V_{IN}	V
V_{IL}	Low-level input voltage, EN, MODE	2 V ≤ V_{IN} ≤ 5.5 V	0		0.4	V
I_{IN}	Input bias current, EN, MODE	EN, MODE = GND or V_{IN}		0.01	1	µA
POWER SWITCH						
$R_{DS(on)}$	High side MOSFET on-resistance	V_{IN} = V_{GS} = 3.6 V, T_A = 25°C		252	492	mΩ
	Low side MOSFET on-resistance			194	391	mΩ
I_{LIMF}	Forward current limit, high and low side MOSFET	V_{IN} = V_{GS} = 3.6 V	0.8	1	1.2	A
T_{SD}	Thermal shutdown	Increasing junction temperature		140		°C
	Thermal-shutdown hysteresis	Decreasing junction temperature		20		°C
OSCILLATOR						
f_{SW}	Oscillator frequency	2 V ≤ V_{IN} ≤ 5.5 V		2.25		MHz
OUTPUT						
V_{OUT}	Adjustable-output voltage range		0.85		V_{IN}	V
V_{OUT}	TPS62562 fixed output voltage	V_{IN} ≥ 1.8 V		1.8		V
V_{ref}	Reference voltage			600		mV
V_{FB}	Feedback voltage, PWM mode	MODE = V_{IN}, PWM operation, for fixed-output-voltage versions V_{FB} = V_{OUT}, 2.5 V ≤ V_{IN} ≤ 5.5 V, 0 mA ≤ I_{OUT} ≤ 600 mA (2)	–2.5%	0%	2.5%	
	Feedback voltage, PFM mode	MODE = GND, device in PFM mode, voltage positioning active(1)		1%		
	Load regulation	PWM mode		–1		%/A
$t_{Start\ Up}$	Start-up time	Time from active EN to reach 95% of V_{OUT} nominal		500		µs
t_{Ramp}	V_{OUT} ramp-up time	Time to ramp from 5% to 95% of V_{OUT}		250		µs
I_{lkg}	Leakage current into SW terminal	V_{IN} = 3.6 V, V_{IN} = V_{OUT} = V_{SW}, EN = GND (3)		0.5	1	µA

(1) In PFM mode, the internal reference voltage is set to typ. 1.01 × V_{ref}. See the Parameter Measurement Information section.
(2) For V_{IN} = V_{OUT} + 0.6 V
(3) In fixed-output-voltage versions, the internal resistor divider network is disconnected from the FB terminal.

PIN ASSIGNMENTS

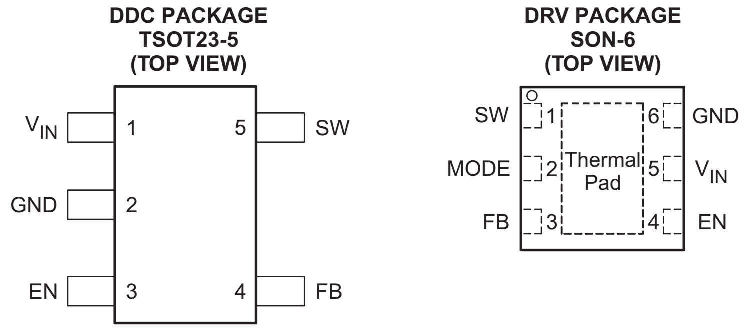
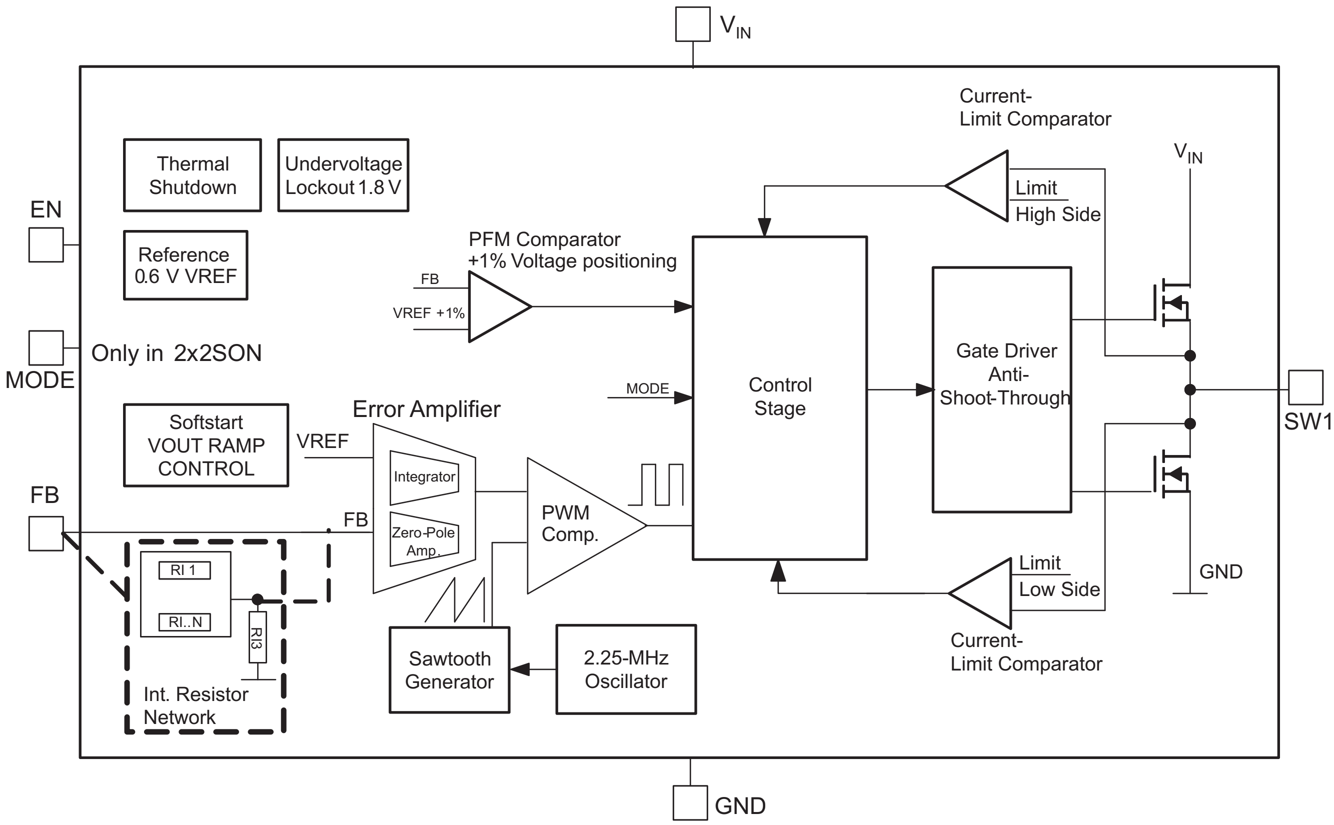


Figure 1.

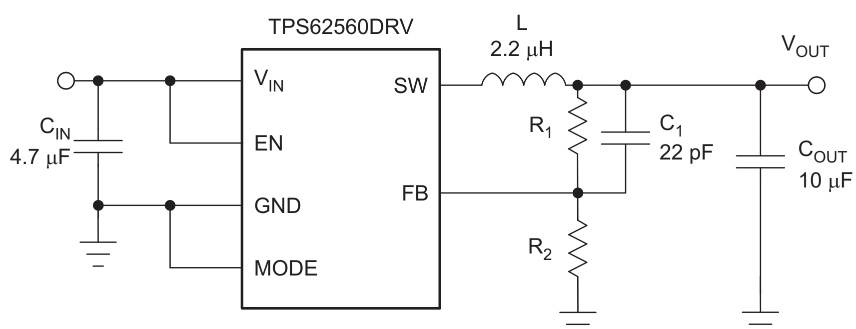
PIN FUNCTIONS

PIN			I/O	DESCRIPTION
NAME	No. QFN-6	No. TSOT23-5		
EN	4	3	I	This is the enable terminal of the device. Pulling this terminal to low forces the device into shutdown mode. Pulling this terminal to high enables the device. This terminal must be terminated.
FB	3	4	I	Feedback terminal for the internal regulation loop. Connect the external resistor divider to this terminal. In the fixed-output-voltage option, connect this terminal directly to the output capacitor.
GND	6	2	—	GND supply terminal
MODE	2	—	I	This terminal is only available as an QFN package option. MODE terminal = high forces the device to operate in the fixed-frequency PWM mode. MODE terminal = low enables the power-save mode with automatic transition from PFM mode to fixed-frequency PWM mode.
SW	1	5	O	This is the switch terminal and is connected to the internal MOSFET switches. Connect the external inductor between this terminal and the output capacitor.
V_{IN}	5	1	—	V_{IN} power-supply terminal

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



L: LPS3015, 2.2 µH, 110 mΩ
C_{IN}: GRM188R60J475K, 4.7 µF, Murata, 0603 size
C_{OUT}: GRM188R60J106M, 10 µF, Murata, 0603 size

TYPICAL CHARACTERISTICS

Table 1. Table of Graphs

			FIGURE
η	Efficiency	vs Output Current, V_{OUT} = 1.8 V, Power Save Mode, MODE = GND	Figure 2
		vs Output Current, V_{OUT} = 1.8 V, PWM Mode, MODE = V_{IN}	Figure 3
		vs Output Current, V_{OUT} = 3.3 V, PWM Mode, MODE = V_{IN}	Figure 4
		vs Output Current, V_{OUT} = 3.3 V, Power Save Mode, MODE = GND	Figure 5
		vs Output Current, MODE = V_{IN}	Figure 6
		vs Output Current, MODE = GND	Figure 7
	Typical Operation	PWM Mode, V_{OUT} = 1.8 V	Figure 8
	Mode Transition	MODE Terminal Transition From PFM to Forced PWM Mode at Light Load	Figure 9
		MODE Terminal Transition From Forced PWM to PFM Mode at Light Load	Figure 10
	Start-up Timing		Figure 11
	Load Transient	Forced PWM Mode, V_{OUT} = 1.5 V, 50 mA to 200 mA	Figure 12
		Forced PWM Mode, V_{OUT} = 1.5 V, 200 mA to 400 mA	Figure 13
		Forced PFM Mode to PWM Mode, V_{OUT} = 1.5 V, 150 µA to 400 mA	Figure 14
		Forced PWM Mode to PFM Mode, V_{OUT} = 1.5 V, 400 mA to 150 µA	Figure 15
		PFM Mode, V_{OUT} = 1.5 V, 1.5 mA to 50 mA	Figure 16
		PFM Mode, V_{OUT} = 1.5 V, 50 mA to 1.5 mA	Figure 17
		PFM Mode to PWM Mode, V_{OUT} = 1.8 V, 50 mA to 250 mA	Figure 18
		PFM Mode to PWM Mode, V_{OUT} = 1.5 V, 50 mA to 400 mA	Figure 19
		PWM Mode to PFM Mode, V_{OUT} = 1.5 V, 400 mA to 50 mA	Figure 20
	Line Transient	PFM Mode, V_{OUT} = 1.8 V, 50 mA	Figure 21
		PFM Mode, V_{OUT} = 1.8 V, 250 mA	Figure 22
	Typical Operation	PFM Mode, V_{OUT} Ripple, V_{OUT} = 1.8 V, 10 mA, L = 2.2 µH, C_{OUT} = 10 µF	Figure 23
		PFM Mode, V_{OUT} Ripple, V_{OUT} = 1.8 V, 10 mA, L = 4.7 µH, C_{OUT} = 10 µF	Figure 24
	Quiescent Current	vs Input Voltage, (T_A = 85°C, T_A = 25°C, T_A = –40°C)	Figure 25
	Static Drain-Source On-State Resistance	vs Input Voltage, (T_A = 85°C, T_A = 25°C, T_A = –40°C), High-Side Switching	Figure 26
		vs Input Voltage, (T_A = 85°C, T_A = 25°C, T_A = –40°C), Low-Side Switching	Figure 27

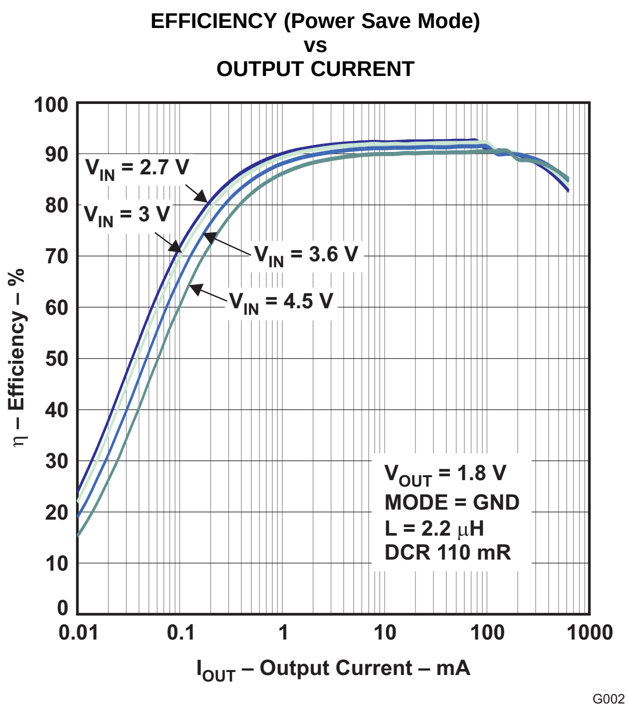


Figure 2.

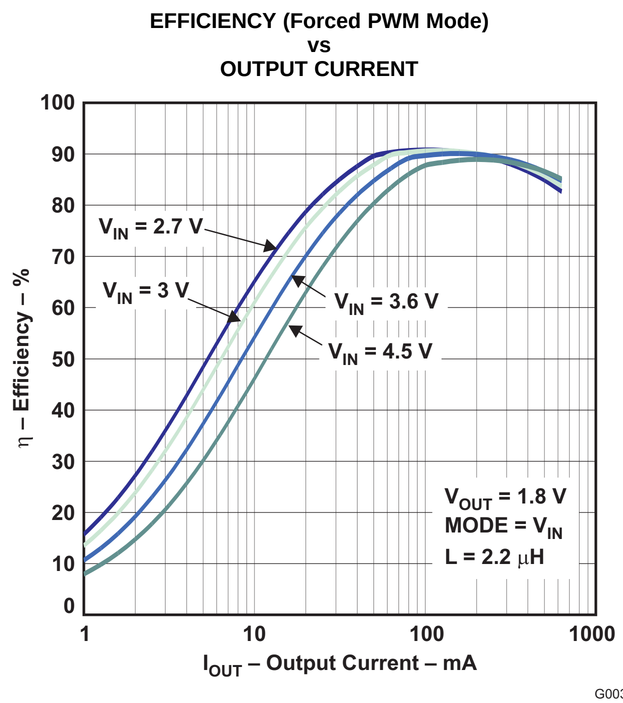


Figure 3.

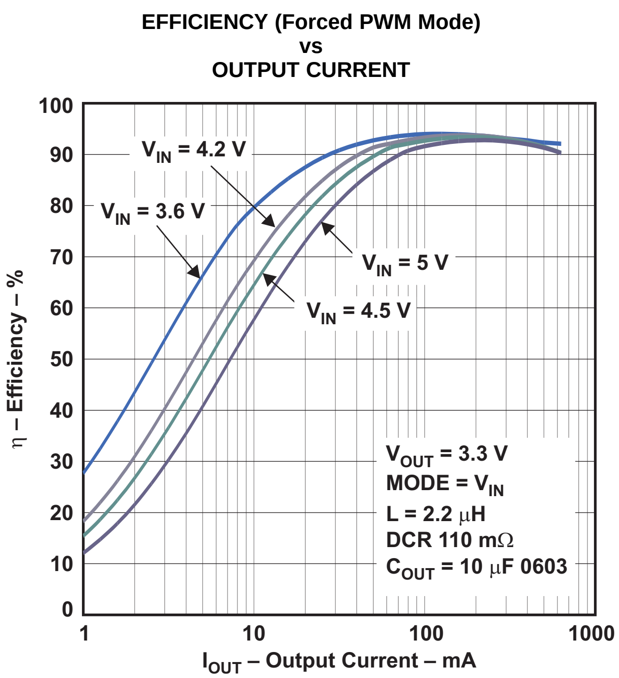


Figure 4.

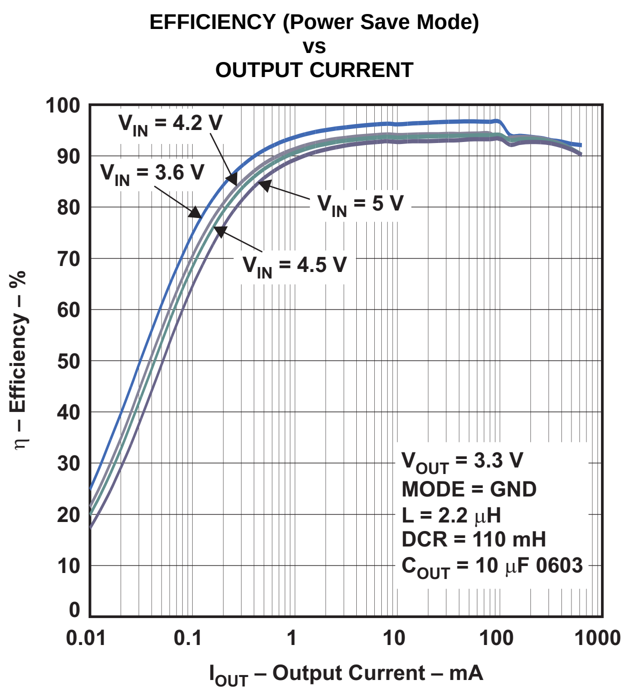


Figure 5.

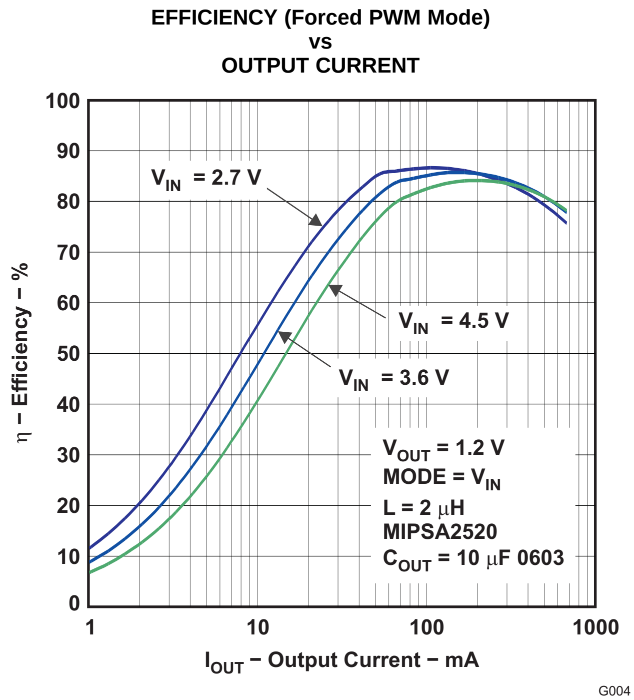


Figure 6.

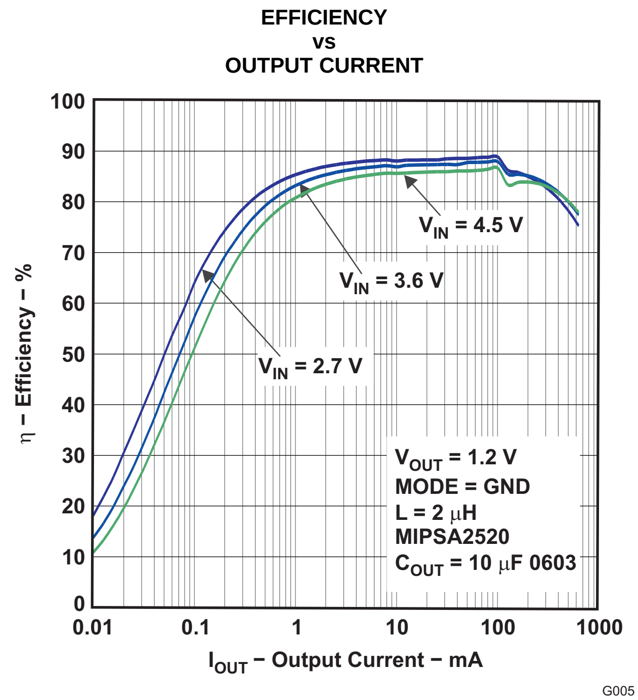


Figure 7.

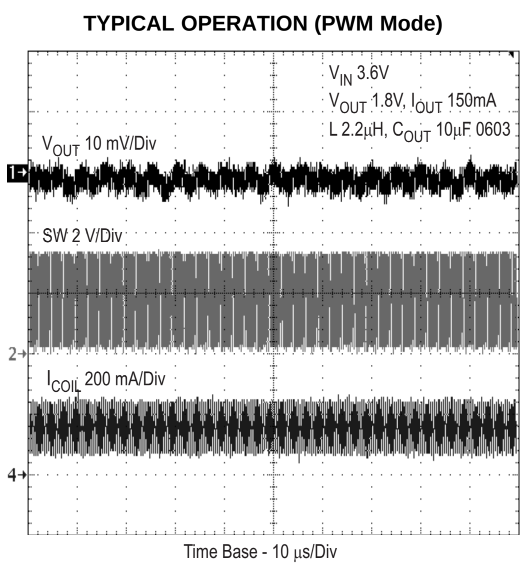


Figure 8.

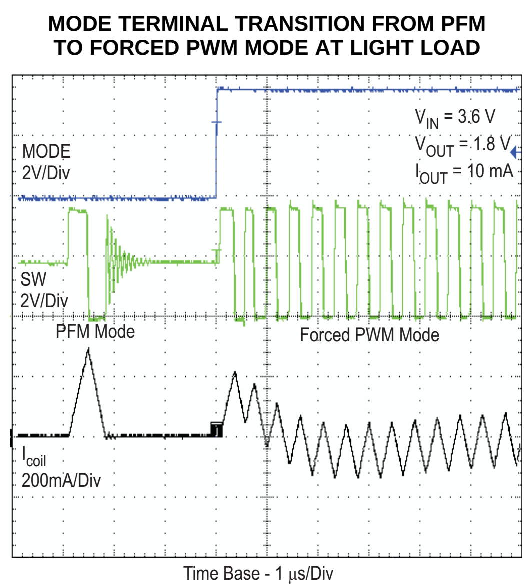


Figure 9.

MODE TERMINAL TRANSITION FROM PWM TO PFM MODE AT LIGHT LOAD

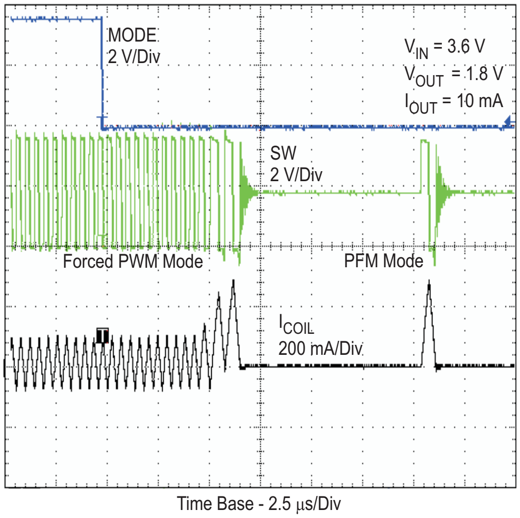


Figure 10.

START-UP TIMING

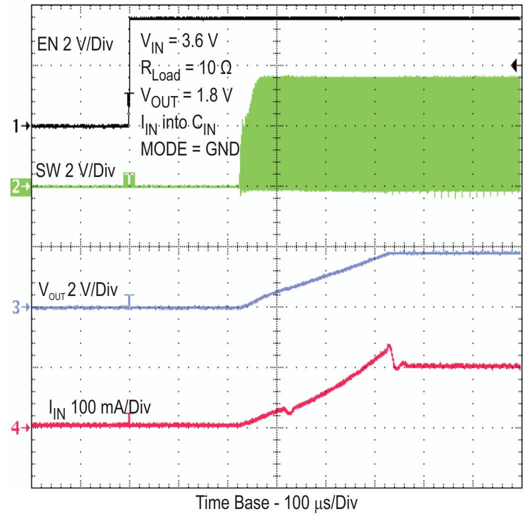


Figure 11.

LOAD TRANSIENT (Forced PWM Mode)

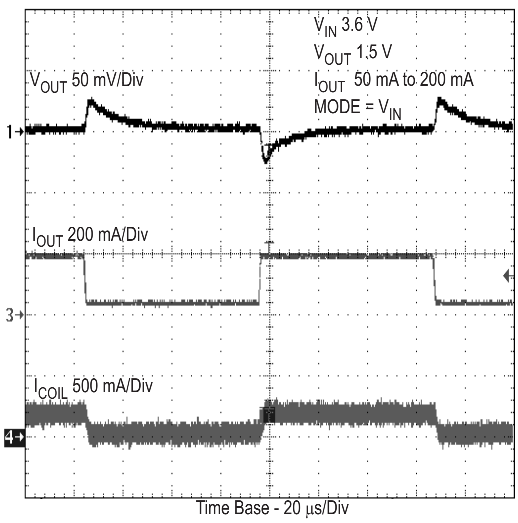


Figure 12.

LOAD TRANSIENT (Forced PWM Mode)

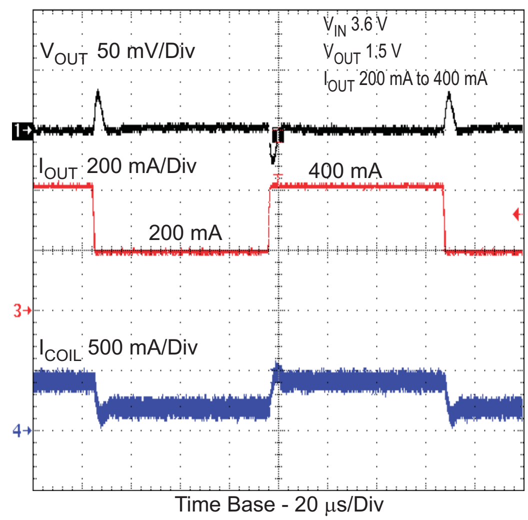


Figure 13.

LOAD TRANSIENT (Forced PFM Mode To PWM Mode)

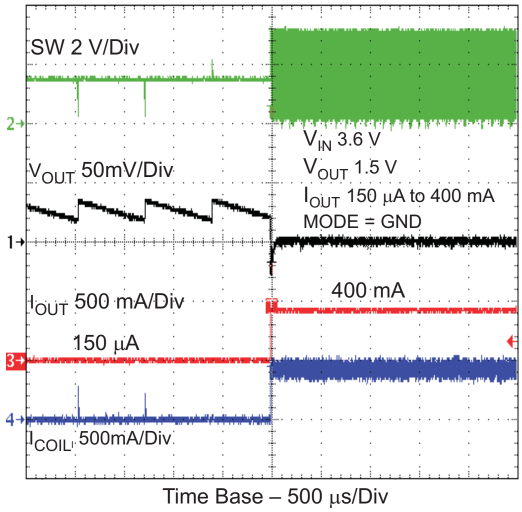


Figure 14.

LOAD TRANSIENT (Forced PWM Mode To PFM Mode)

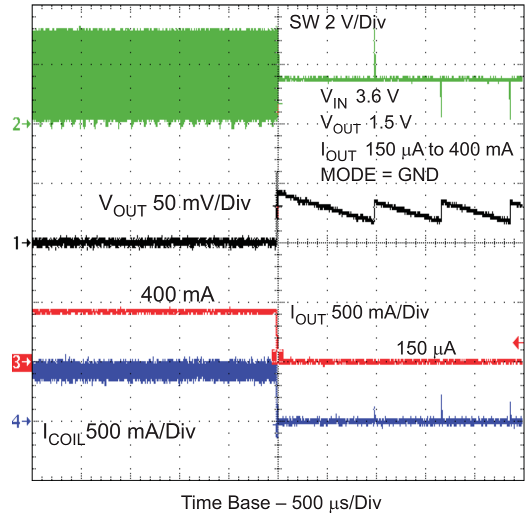


Figure 15.

LOAD TRANSIENT (PFM Mode)

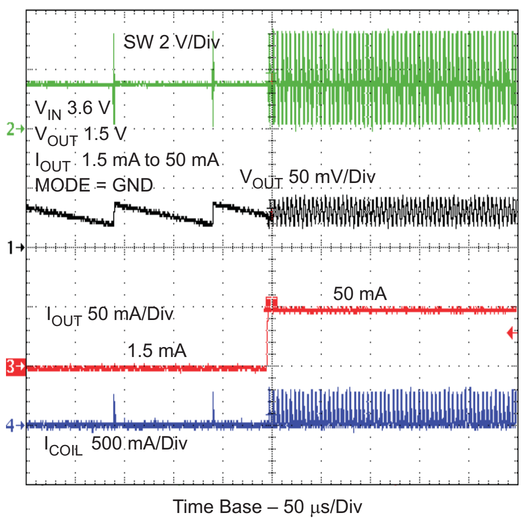


Figure 16.

LOAD TRANSIENT (PFM Mode)

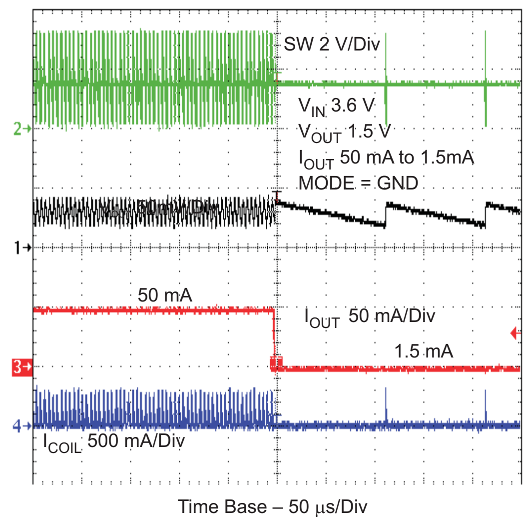
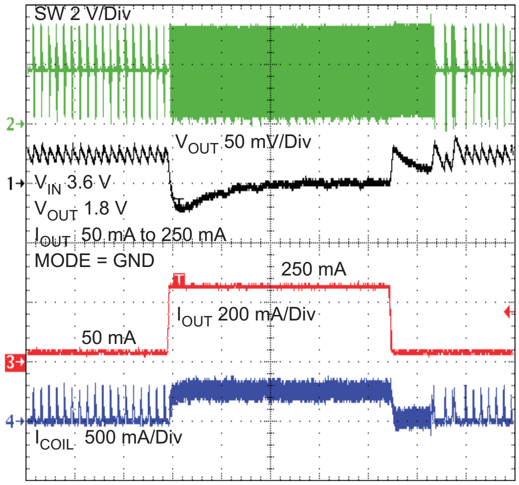


Figure 17.

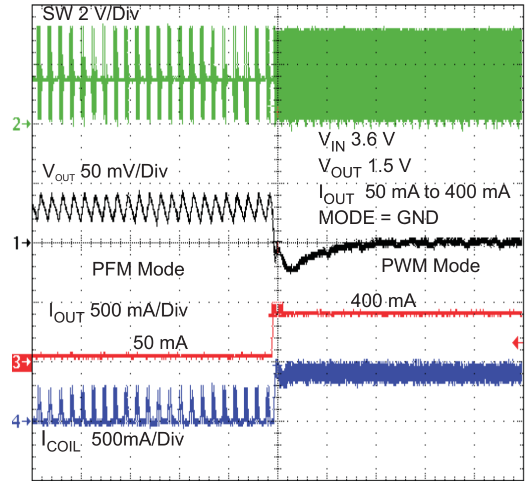
LOAD TRANSIENT (PFM Mode To PWM Mode)



Time Base – 20 µs/Div

Figure 18.

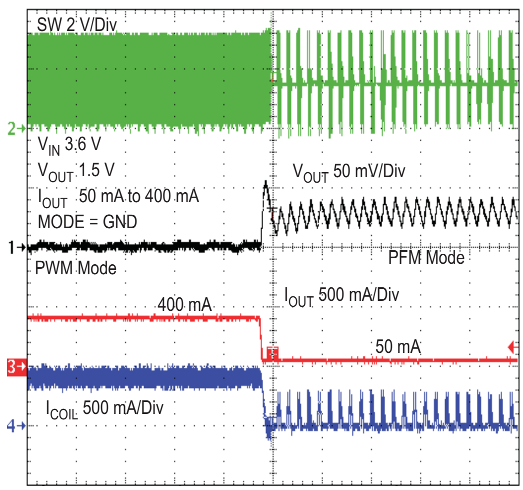
LOAD TRANSIENT (PFM Mode To PWM Mode)



Time Base – 20 µs/Div

Figure 19.

LOAD TRANSIENT (PWM Mode To PFM Mode)



Time Base – 20 µs/Div

Figure 20.

LINE TRANSIENT (PFM Mode)

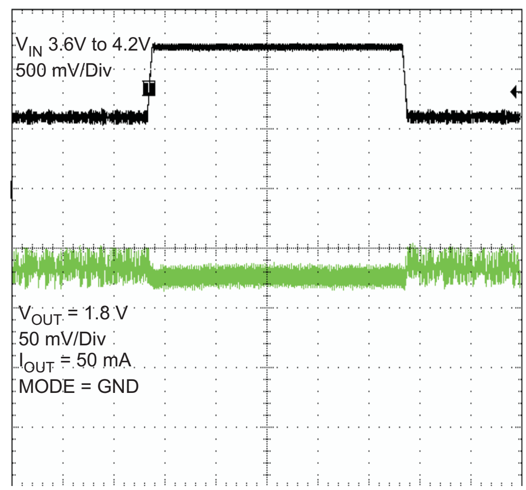


Figure 21.

LINE TRANSIENT (PWM Mode)

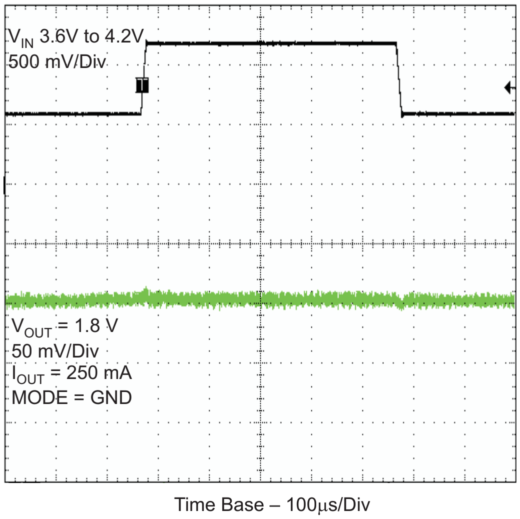


Figure 22.

TYPICAL OPERATION (PFM Mode)

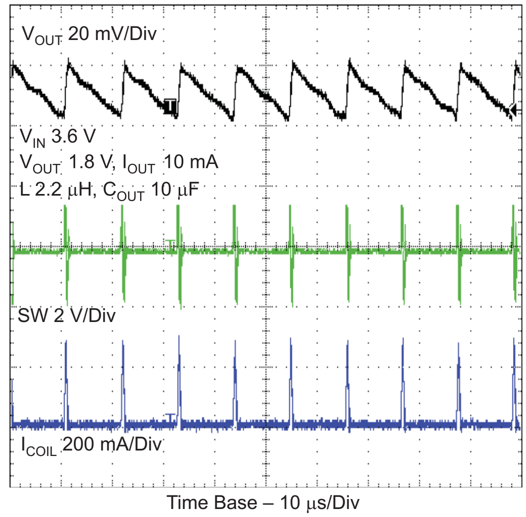


Figure 23.

TYPICAL OPERATION (PFM Mode)

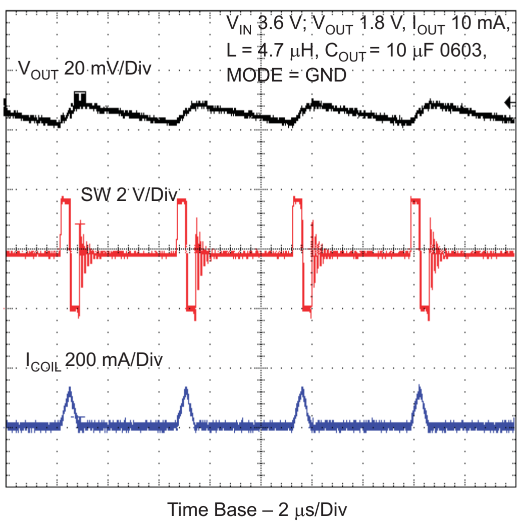


Figure 24.

QUIESCENT CURRENT vs INPUT VOLTAGE

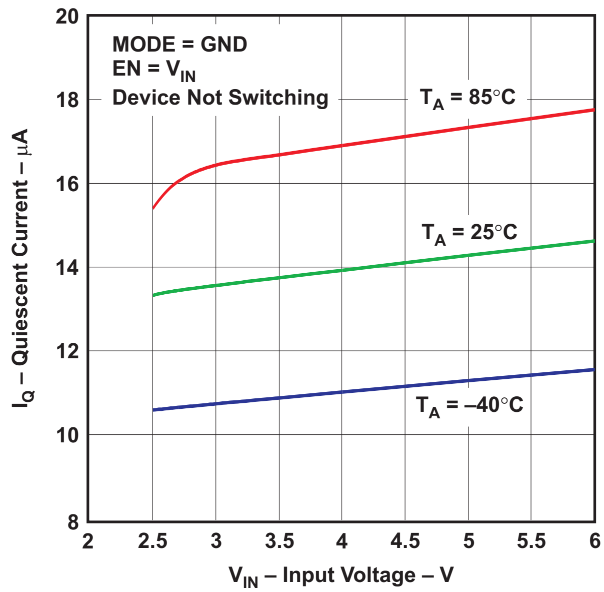


Figure 25.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
INPUT VOLTAGE

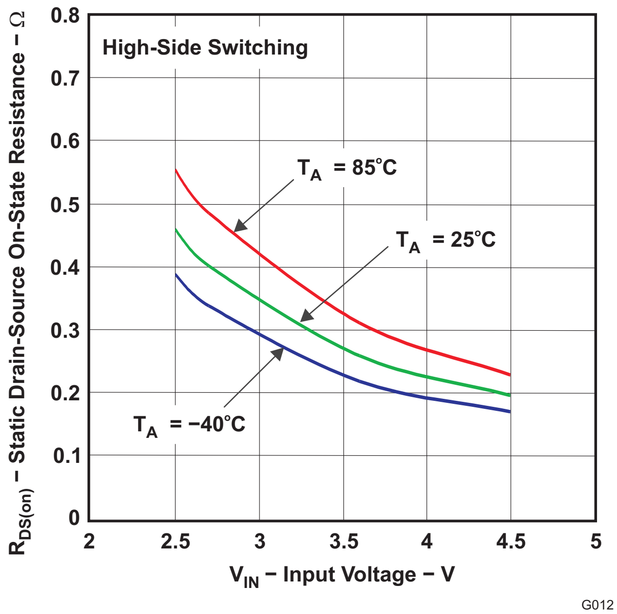


Figure 26.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
INPUT VOLTAGE

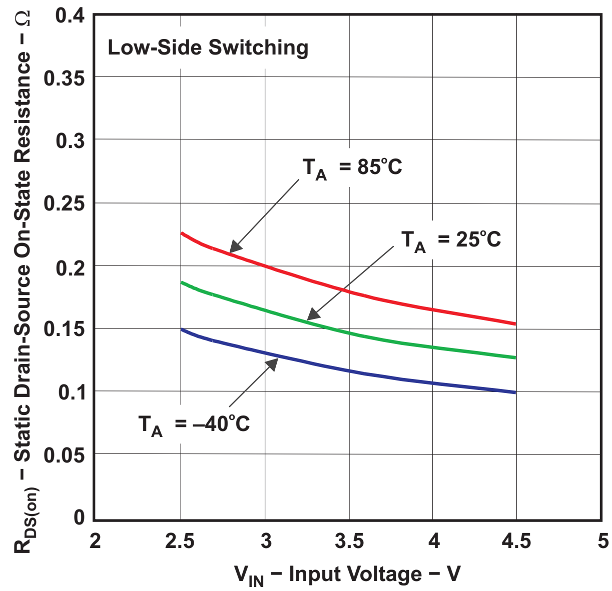


Figure 27.

DETAILED DESCRIPTION

OPERATION

The TPS62560/62 step-down converters operate with typically 2.25-MHz fixed-frequency pulse-width modulation (PWM) at moderate to heavy load currents. At light load currents, the converter can automatically enter power-save mode, and then operates in PFM mode. However, the TPS62561 operates with fixed-frequency PWM only, also at light load conditions.

During PWM operation, the converter uses a unique fast-response voltage-mode control scheme with input-voltage feed-forward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the high-side MOSFET switch is turned on. The current flows from the input capacitor via the high-side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turns off the switch. The current-limit comparator also turns off the switch in case the current limit of the high-side MOSFET switch is exceeded. After a dead time, which prevents shoot-through current, the low-side MOSFET rectifier is turned on and the inductor current ramps down. The current flows from the inductor to the output capacitor and to the load. It returns back to the inductor through the low-side MOSFET rectifier.

The next cycle is initiated by the clock signal again turning off the low-side MOSFET rectifier and turning on the on the high-side MOSFET switch.

POWER-SAVE MODE

The power-save mode is enabled with the MODE terminal set to the low level. If the load current decreases, the converter enters the power-save mode of operation automatically. During power-save mode, the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage typically 1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

The transition from PWM mode to PFM mode occurs once the inductor current in the low-side MOSFET switch becomes zero, which indicates discontinuous conduction mode.

During the power-save mode, the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of V_{OUT} nominal + 1%, the device starts a PFM current pulse. The high-side MOSFET switch turns on, and the inductor current ramps up. After the on-time expires, the switch is turned off and the low-side MOSFET switch is turned on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current, the output voltage rises. If the output voltage is equal to or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with typical 15-µA current consumption.

If the output voltage is still below the PFM comparator threshold, a sequence of further PFM current pulses is generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold.

With a fast single-threshold comparator, the output-voltage ripple during PFM-mode operation can be kept small. The PFM pulse is time controlled, which allows modifying the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output-voltage ripple and PFM frequency depend primarily on the size of the output capacitor and the inductor value. Increasing output capacitor values and inductor values minimizes the output ripple. The PFM frequency decreases with smaller inductor values and increases with larger values.

The PFM mode is left and PWM mode entered in case the output current can no longer be supported in PFM mode. The power-save mode can be disabled by setting the MODE terminal to high. The converter then operates in the fixed-frequency PWM mode.

Dynamic Voltage Positioning

This feature reduces the voltage under/overshoots at load steps from light to heavy load and vice versa. It is active in power-save mode and regulates the output voltage 1% higher than the nominal value. This provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off.

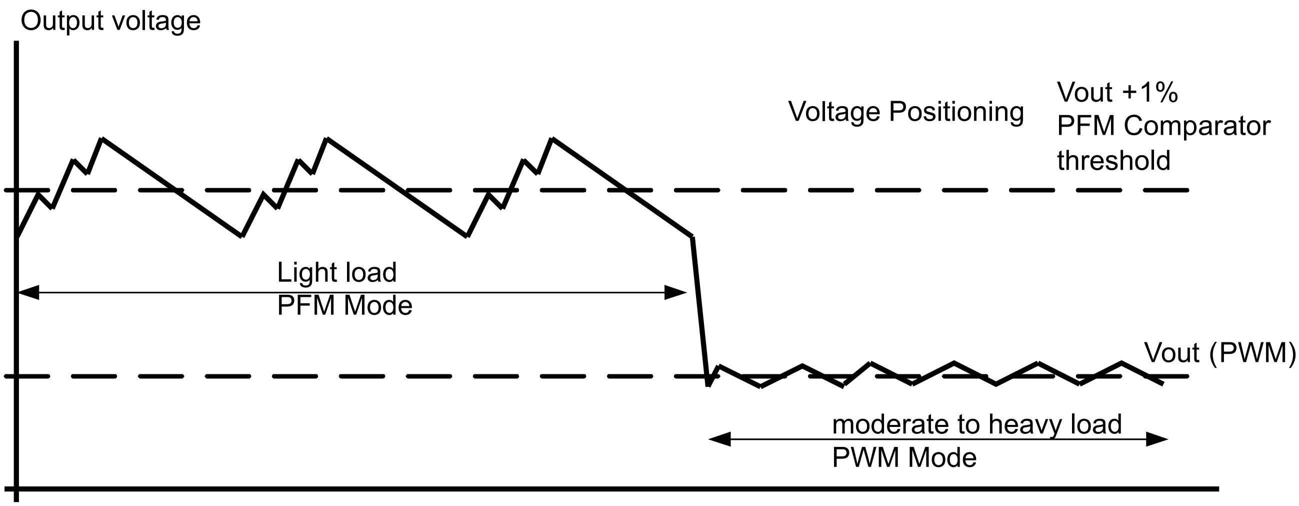


Figure 28. Power Save Mode Operation With Automatic Mode Transition

100% Duty-Cycle Low-Dropout Operation

The device starts to enter 100% duty-cycle mode once the input voltage comes close to the nominal output voltage. In order to maintain the output voltage, the high-side MOSFET switch is turned on 100% for one or more cycles.

With further decreasing V_{IN}, the high-side MOSFET switch is turned on completely. In this case, the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery-voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN}min = V_{OUT}max + I_{OUT}max \times (R_{DS(on)}max + R_L)$$

with:

$I_{OUT}max$ = maximum output current plus inductor ripple current

$R_{DS(on)}max$ = maximum P-channel switch $R_{DS(on)}$

R_L = dc resistance of the inductor

$V_{OUT}max$ = nominal output voltage plus maximum output voltage tolerance

Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables the output stage of the converter. The undervoltage lockout threshold is typically 1.85 V with falling V_{IN}.

MODE SELECTION

The MODE terminal allows mode selection between forced-PWM mode and power-save mode.

Connecting this terminal to GND enables the power-save mode with automatic transition between PWM and PFM modes. Pulling the MODE terminal high forces the converter to operate in fixed-frequency PWM mode even at light load currents. This allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads.

The state of the MODE terminal can be changed during operation to allow efficient power management by adjusting the operation mode of the converter to the specific system requirements.

ENABLE

The device is enabled by setting the EN terminal to high. During the start-up time $t_{Start\ Up}$, the internal circuits are settled and the soft-start circuit is activated. The EN input can be used to control power sequencing in a system with various dc/dc converters. The EN terminal can be connected to the output of another converter, to drive the EN terminal high to achieve a sequencing of the given supply rails. With EN = GND, the device enters shutdown mode, in which all internal circuits are disabled. In fixed-output-voltage versions, the internal resistor divider network is then disconnected from the FB terminal.

SOFT START

The TPS62560 has an internal soft-start circuit that controls the ramp-up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value typically within 250 µs. This limits the inrush current into the converter during ramp-up and prevents possible input voltage drops when a battery or high-impedance power source is used. The soft-start circuit is enabled within the start-up time $t_{Start\ Up}$.

SHORT-CIRCUIT PROTECTION

The high-side and low-side MOSFET switches are short-circuit protected with maximum switch current = I_{LIMF}. The current in the switches is monitored by current-limit comparators. Once the current in the high-side MOSFET switch exceeds the threshold of its current-limit comparator, it turns off and the low-side MOSFET switch is activated to ramp down the current in the inductor and high-side MOSFET switch. The high-side MOSFET switch can only turn on again after the current in the low-side MOSFET switch has decreased below the threshold of its current-limit comparator.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds 140°C (typical), the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

APPLICATION INFORMATION

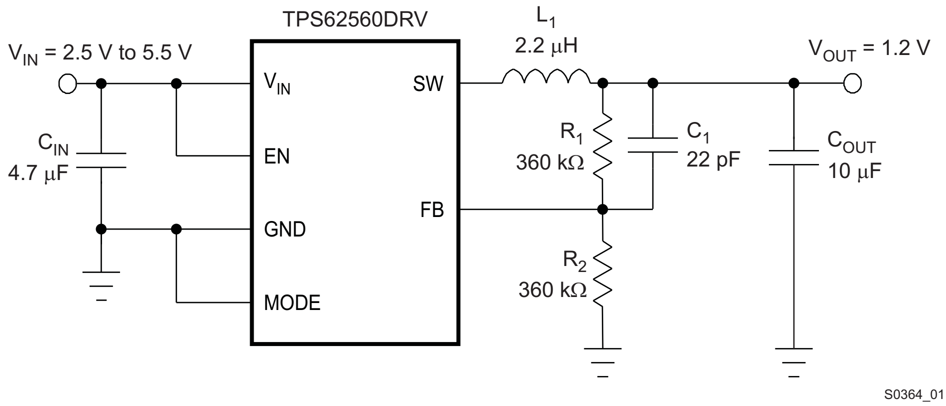


Figure 29. TPS62560 Adjustable 1.2-V Output

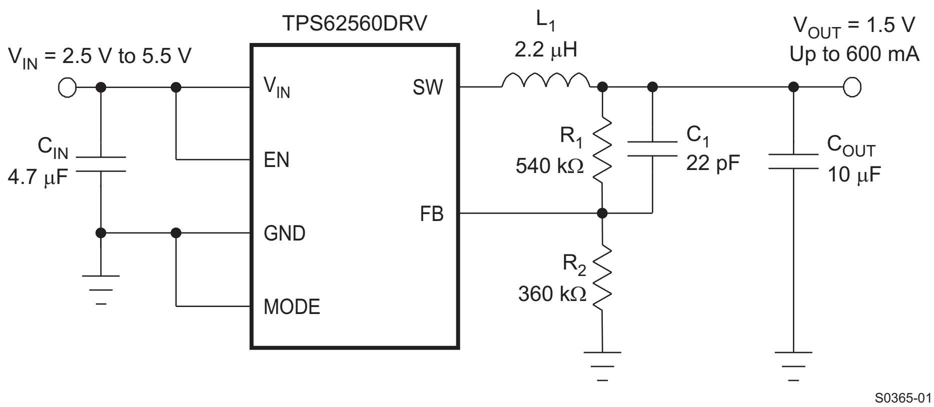


Figure 30. TPS62560 Adjustable 1.5-V Output

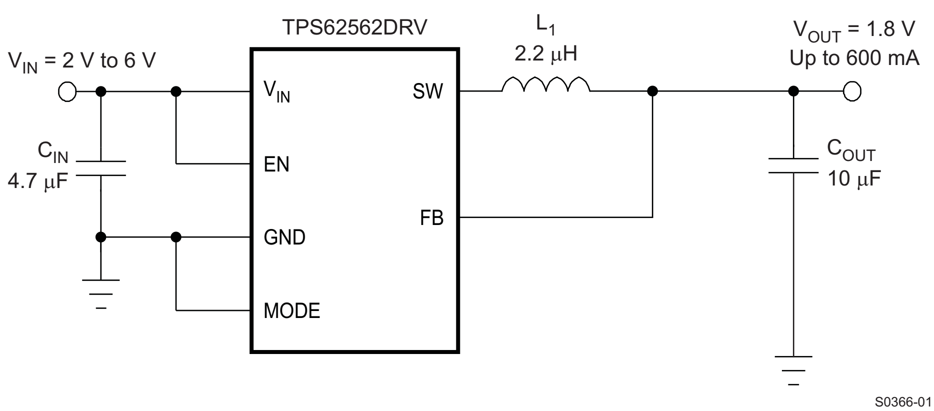


Figure 31. TPS62562 Fixed 1.8-V Output

OUTPUT VOLTAGE SETTING

For adjustable output voltage versions, the output voltage can be calculated as:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$ with an internal reference voltage V_{REF}, typically 0.6 V.

To minimize the current through the feedback divider network, R_2 should be 180 kΩ or 360 kΩ. The sum of R_1 and R_2 should not exceed ~1 MΩ, to keep the network robust against noise. An external feed-forward capacitor, C_1, is required for optimum load transient response. The value of C_1 should be in the range between 22 pF and 33 pF.

In case of using the fixed output voltage version (TPS62562), V_{out} has to be connected to the feedback pin FB.

Route the FB line away from noise sources, such as the inductor or the SW line.

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

The TPS62560 is designed to operate with inductors in the range of 1.5 µH to 4.7 µH and with output capacitors in the range of 4.7 µF to 22 µF. The part is optimized for operation with a 2.2-µH inductor and 10-µF output capacitor.

Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For stable operation, the L and C values of the output filter may not fall below 1 µH effective inductance and 3.5 µF effective capacitance.

Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor must be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT}.

The inductor selection also impacts the output voltage ripple in PFM mode. Higher inductor values lead to lower output voltage ripple and higher PFM frequency; lower inductor values lead to a higher output voltage ripple but lower PFM frequency.

Equation 1 calculates the maximum inductor current in PWM mode under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 2. This is recommended because during heavy load transients the inductor current rises above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \quad (1)$$

$$I_L max = I_{out} max + \frac{\Delta I_L}{2} \quad (2)$$

where:

- f = Switching frequency (2.25 MHz, typical)
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current
- $I_L$max = Maximum inductor current

Table 2. List of Inductors

DIMENSIONS, mm	INDUCTANCE, µH	INDUCTOR TYPE	SUPPLIER
2,5 × 2 × 1 max	2	MIPS2520D2R2	FDK
2,5 × 2 × 1,2 max	2	MIPSA2520D2R2	FDK
2,5 × 2 × 1 max	2.2	KSLI-252010AG2R2	Hitachi Metals
2,5 × 2 × 1,2 max	2.2	LQM2HPN2R2MJ0L	Murata
3 × 3 × 1,5 max	2.2	LPS3015 2R2	Coilcraft

A more conservative approach is to select the inductor current rating just for the switch current limit I_{LIMF} of the converter.

Accepting larger values of ripple current allows the use of lower inductance values, but results in higher output voltage ripple, greater core losses, and lower output current capability.

The total losses of the coil have a strong impact on the efficiency of the dc/dc conversion and consist of both the losses in the dc resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

Output Capacitor Selection

The advanced fast-response voltage-mode control scheme of the TPS62560 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode, and the RMS ripple current is calculated as:

$$I_{RMSC_{OUT}} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2\sqrt{3}} \tag{3}$$

At nominal load current, the device operates in PWM mode, and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right) \tag{4}$$

At light load currents, the converter operates in power-save mode, and the output voltage ripple is dependent on the output capacitor and inductor values. Larger output capacitor and inductor values minimize the voltage ripple in PFM mode and tighten dc output accuracy in PFM mode.

Input Capacitor Selection

An input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications, a 4.7-μF to 10-μF ceramic capacitor is recommended. Because a ceramic capacitor loses up to 80% of its initial capacitance at 5 V, it is recommended that 10-μF input capacitors be used for input voltages > 4.5 V. The input capacitor can be increased without any limit for better input voltage filtering. Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or V_{IN} step on the input can induce ringing at the V_{IN} terminal. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

Table 3. List of Capacitors

CAPACITANCE	TYPE	SIZE	SUPPLIER
4.7 μF	GRM188R60J475K	0603—1,6 × 0,8 × 0,8 mm	Murata
10 μF	GRM188R60J106M69D	0603—1,6 × 0,8 × 0,8 mm	Murata

LAYOUT CONSIDERATIONS

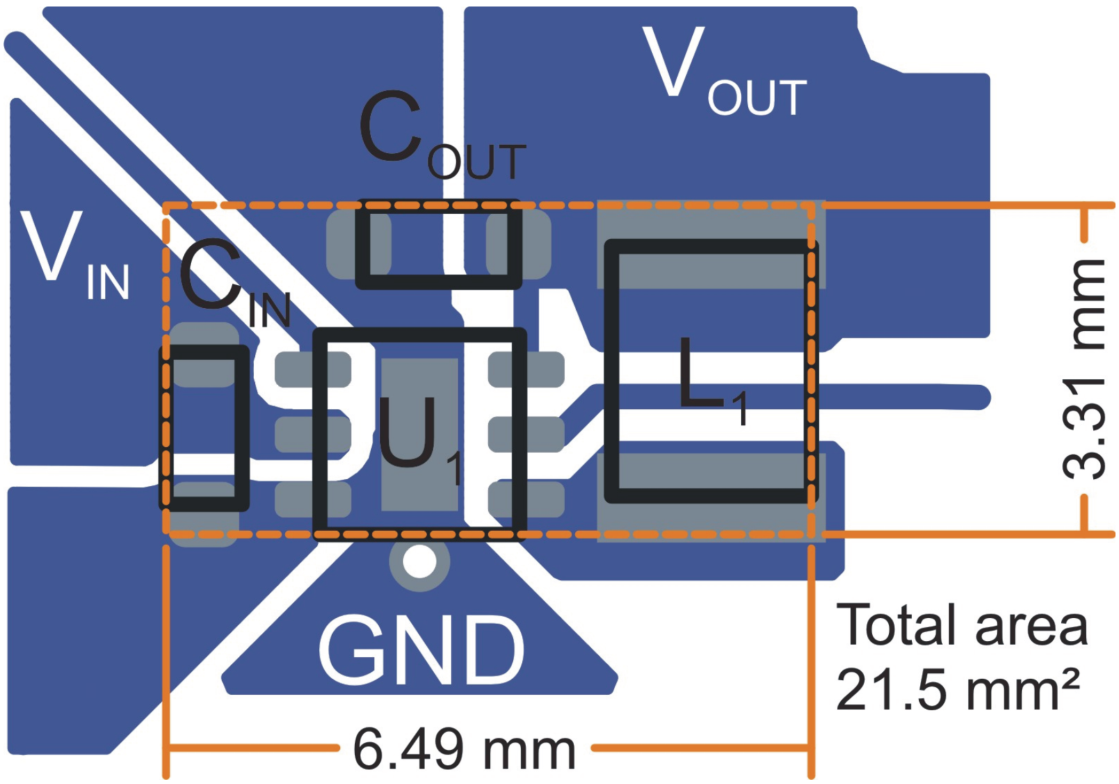


Figure 32. Suggested Layout for Fixed-Output-Voltage Options

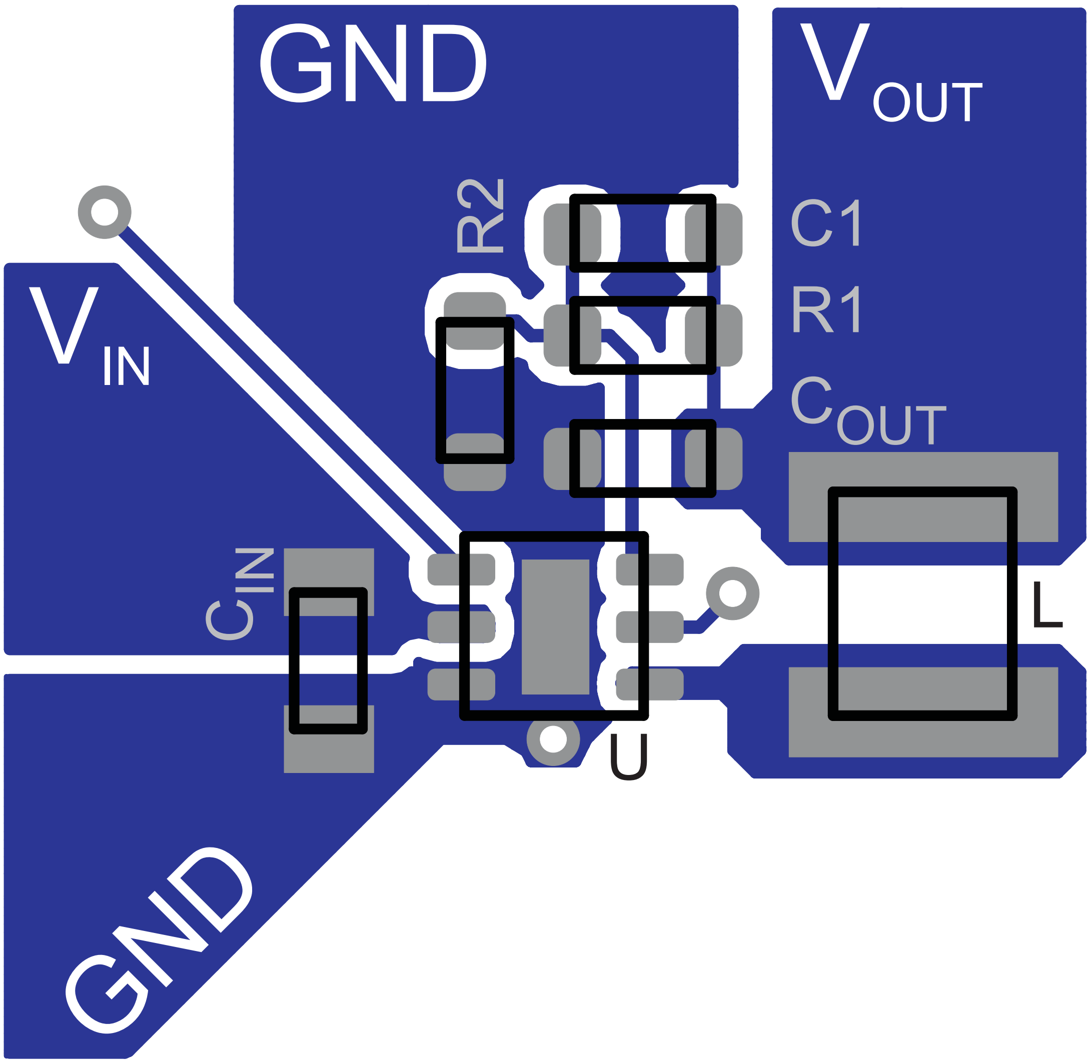


Figure 33. Suggested Layout for Adjustable-Output-Voltage Version

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation and stability issues, as well as EMI problems. It is critical to provide a low-inductance, low-impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor, inductor, and output capacitor should be placed as close as possible to the IC terminals.

Connect the GND terminal of the device to the thermal-pad land of the PCB and use this pad as a star point. Use a common power-GND node and a different node for the signal GND to minimize the effects of ground noise. Connect these ground nodes together to the thermal-pad land (star point) underneath the IC. Keep the common path to the GND terminal, which returns the small signal components and the high current of the output capacitors, as short as possible to avoid ground noise. The FB line should be connected directly to the output capacitor and routed away from noisy components and traces (e.g., the SW line).

Changes from Original (January 2008) to Revision A **Page**

- Changed at all levels. Revision A is a complete rewrite of this data sheet. 1

Changes from Revision A (July 2008) to Revision B **Page**

- Added TPS62562 device number. 1

Changes from Revision B (March 2009) to Revision C **Page**

- Deleted High Efficiency Step Down Converter 1
- Deleted "Wide" from Features bullet 1
- Deleted "for Li-Ion Batteries With Extended Voltage Range" from Features 1
- Deleted "Adjustable and Fixed Output-Voltage Options" from Features 1
- Deleted "2.25 MHz Fixed Frequency Operation" from Features 1
- Deleted "Power Save Mode at Light Load Currents" from Features 1
- Deleted "Voltage Positioning at Light Loads" from Features 1
- Deleted "Allows < 1-mm Solution Height" from Features 1
- Added reference to TPS62260 1
- Changed Description to better reflect device capabilities and differences to TPS62260 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62560DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CEY	Samples
TPS62560DRVRG4	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CEY	Samples
TPS62560DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CEY	Samples
TPS62560DRVTG4	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CEY	Samples
TPS62561DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CVO	Samples
TPS62561DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CVO	Samples
TPS62562DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NXT	Samples
TPS62562DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NXT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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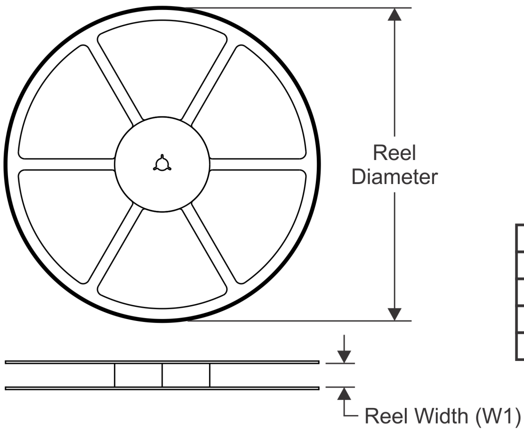
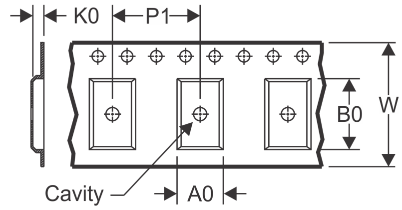
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

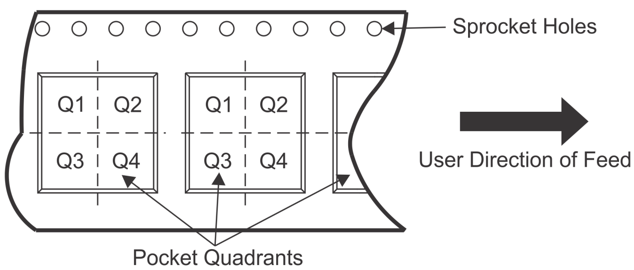


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

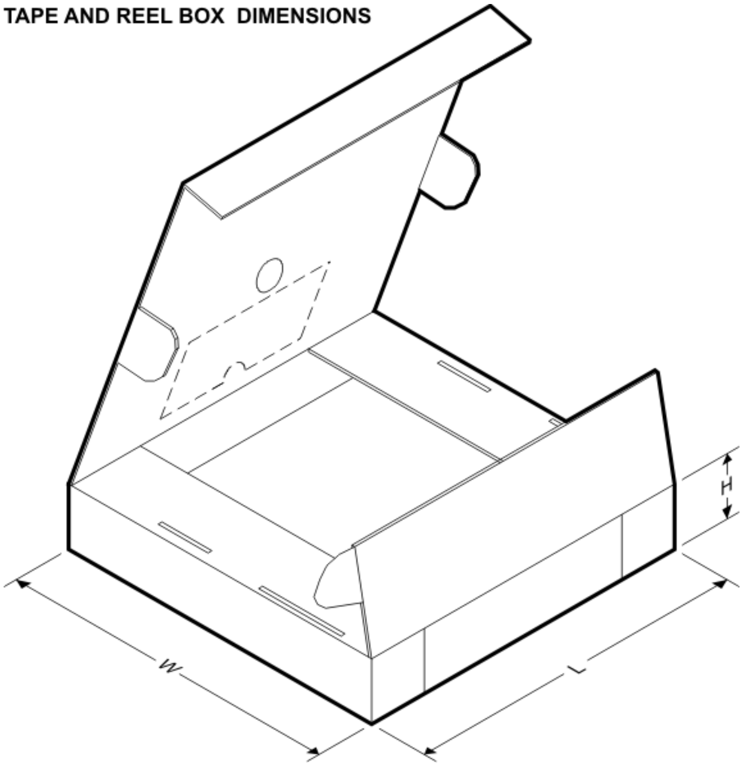
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62560DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62560DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62561DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62561DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62562DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62562DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

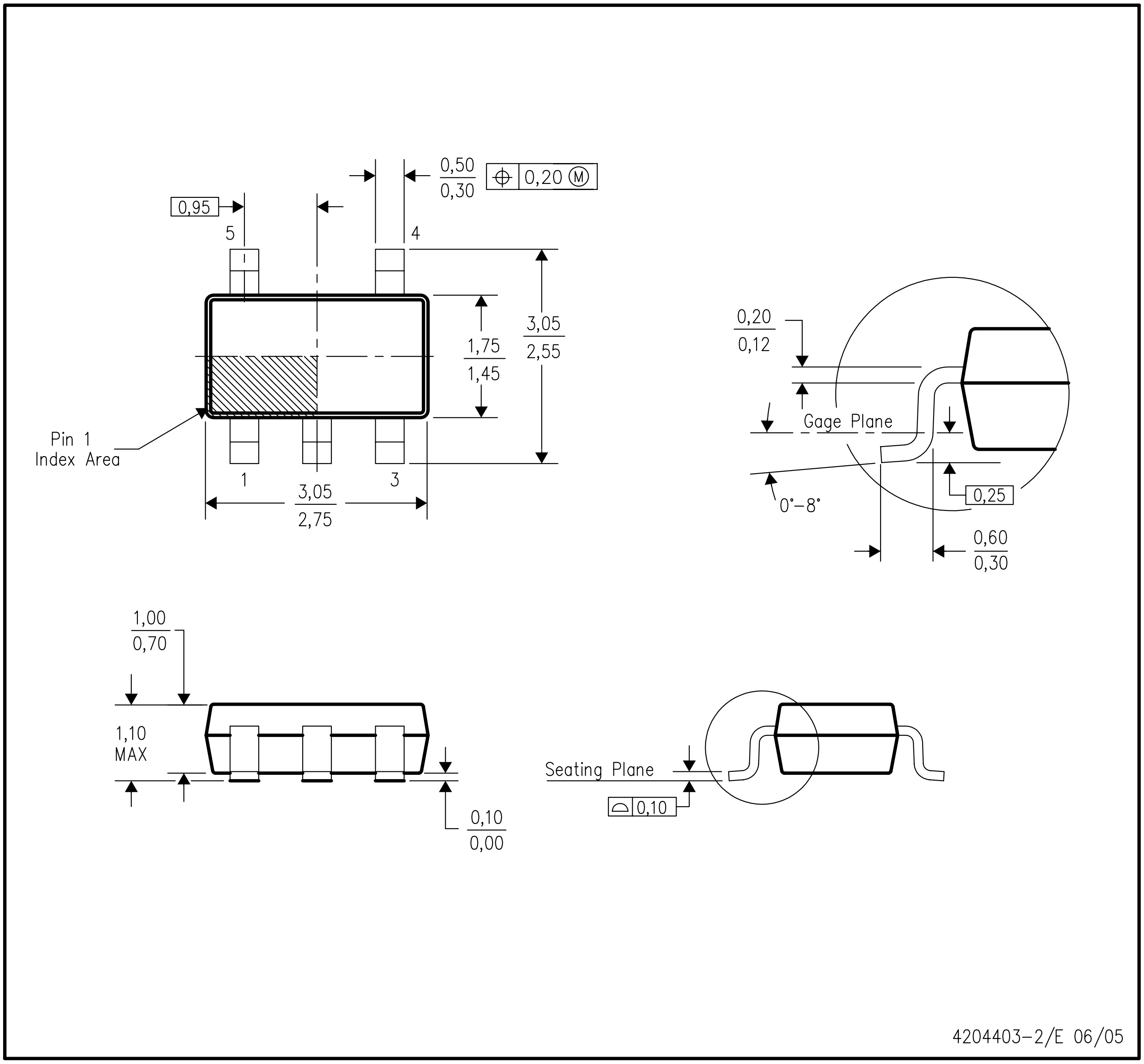
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

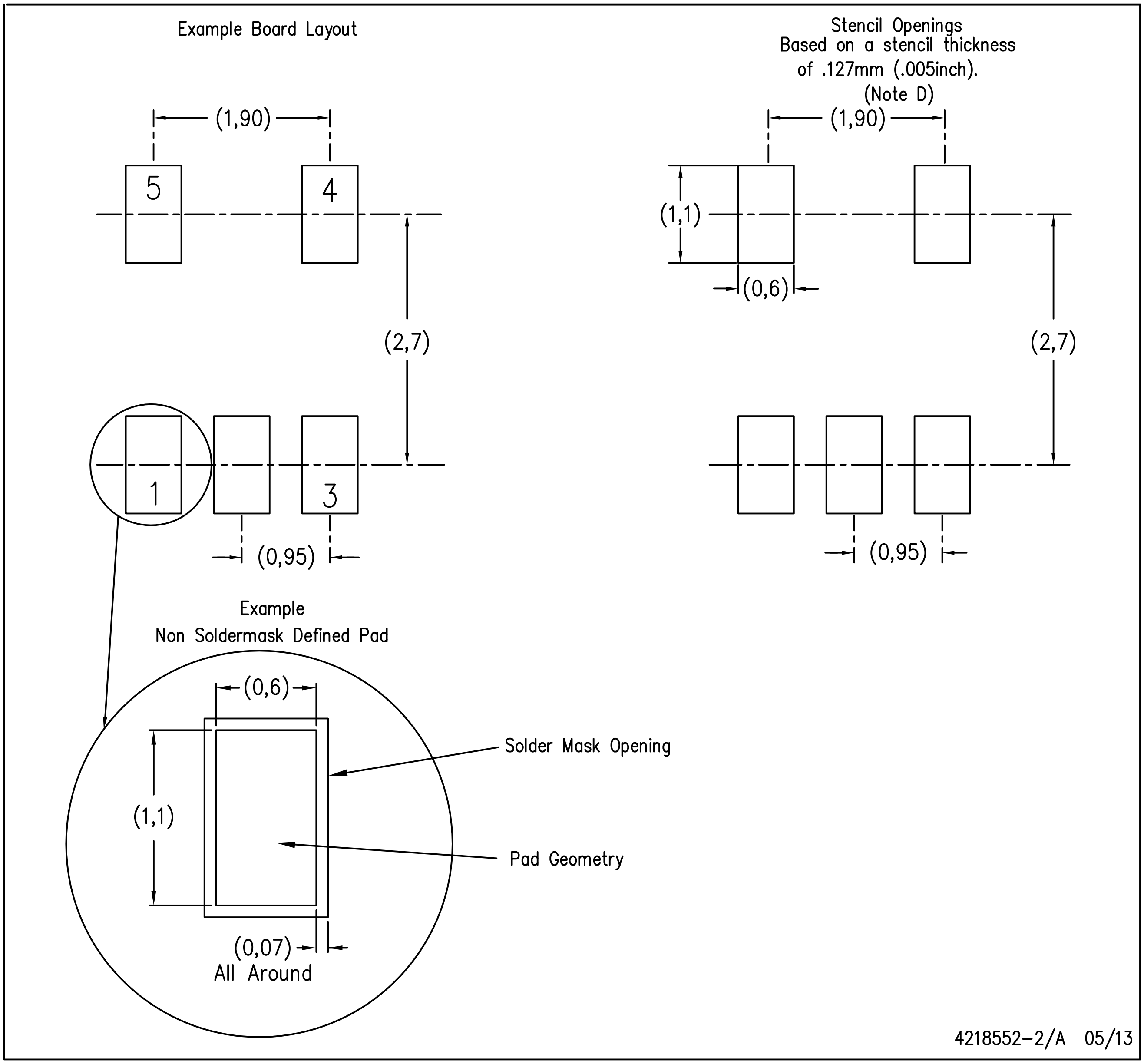
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62560DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS62560DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS62561DDCR	SOT	DDC	5	3000	203.0	203.0	35.0
TPS62561DDCT	SOT	DDC	5	250	203.0	203.0	35.0
TPS62562DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS62562DRVT	WSON	DRV	6	250	203.0	203.0	35.0

DDC (R-PDSO-G5) PLASTIC SMALL-OUTLINE



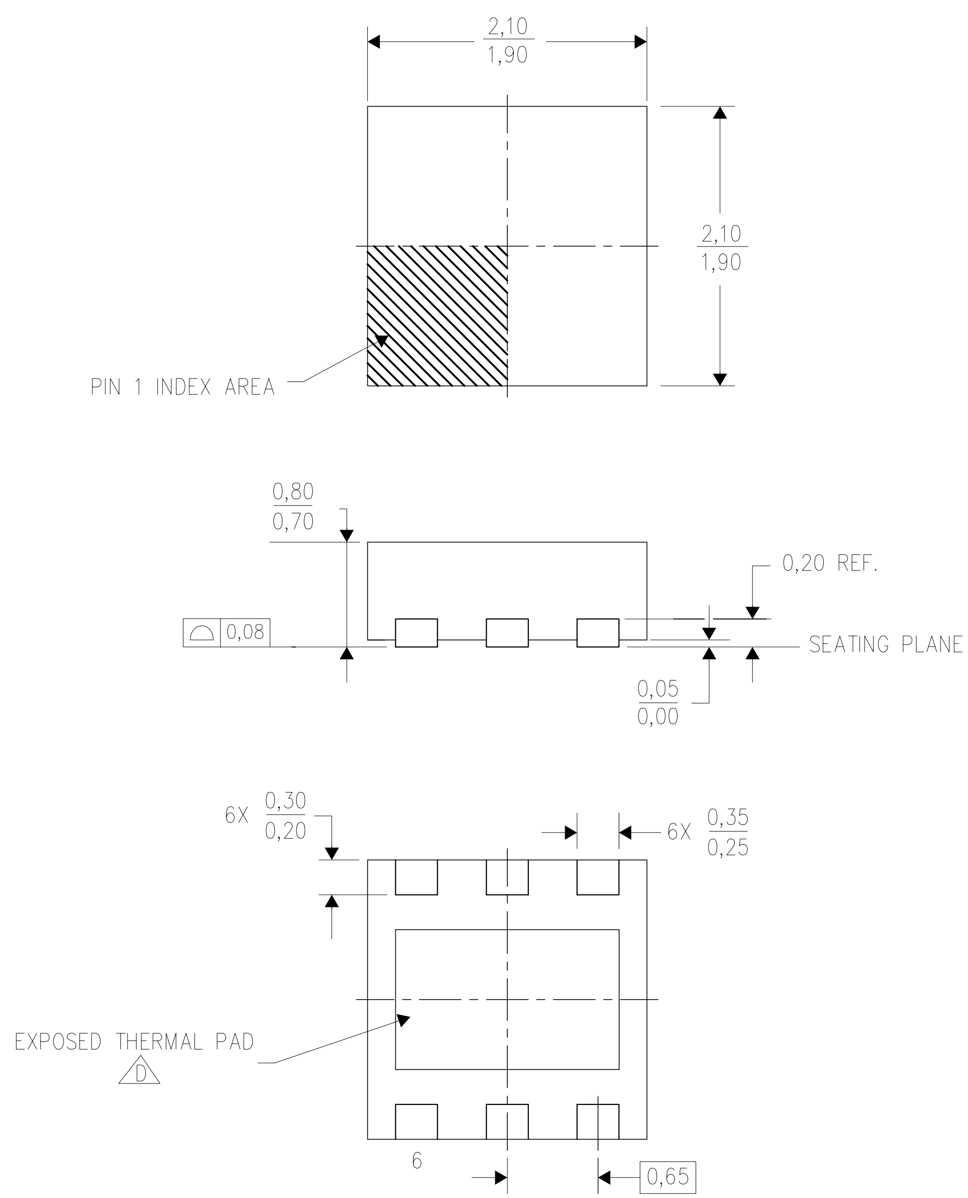
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO-193 variation AB (5 pin).

DDC (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

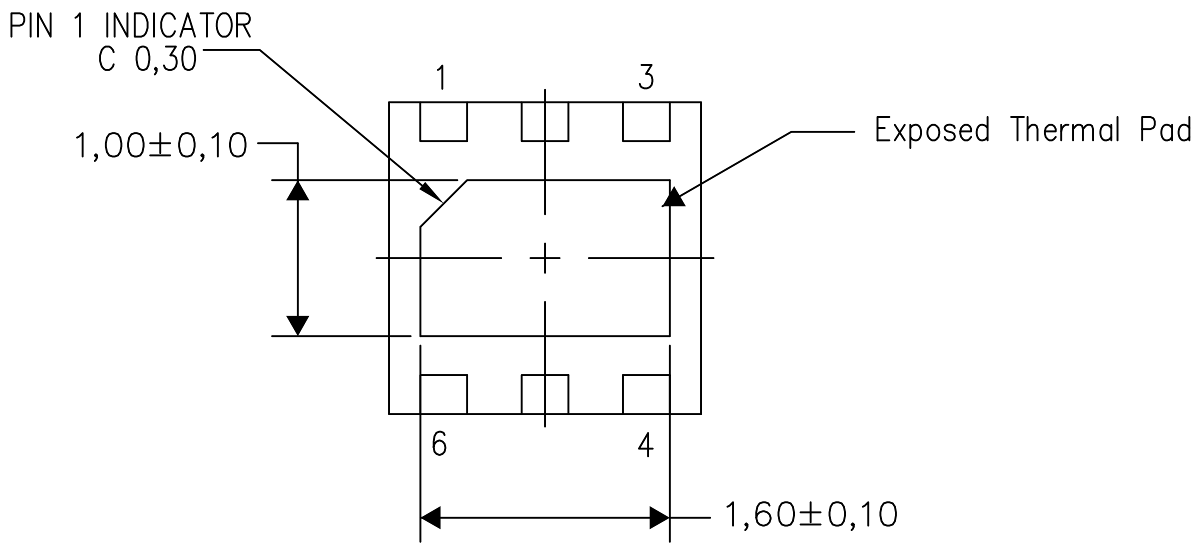
DRV (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



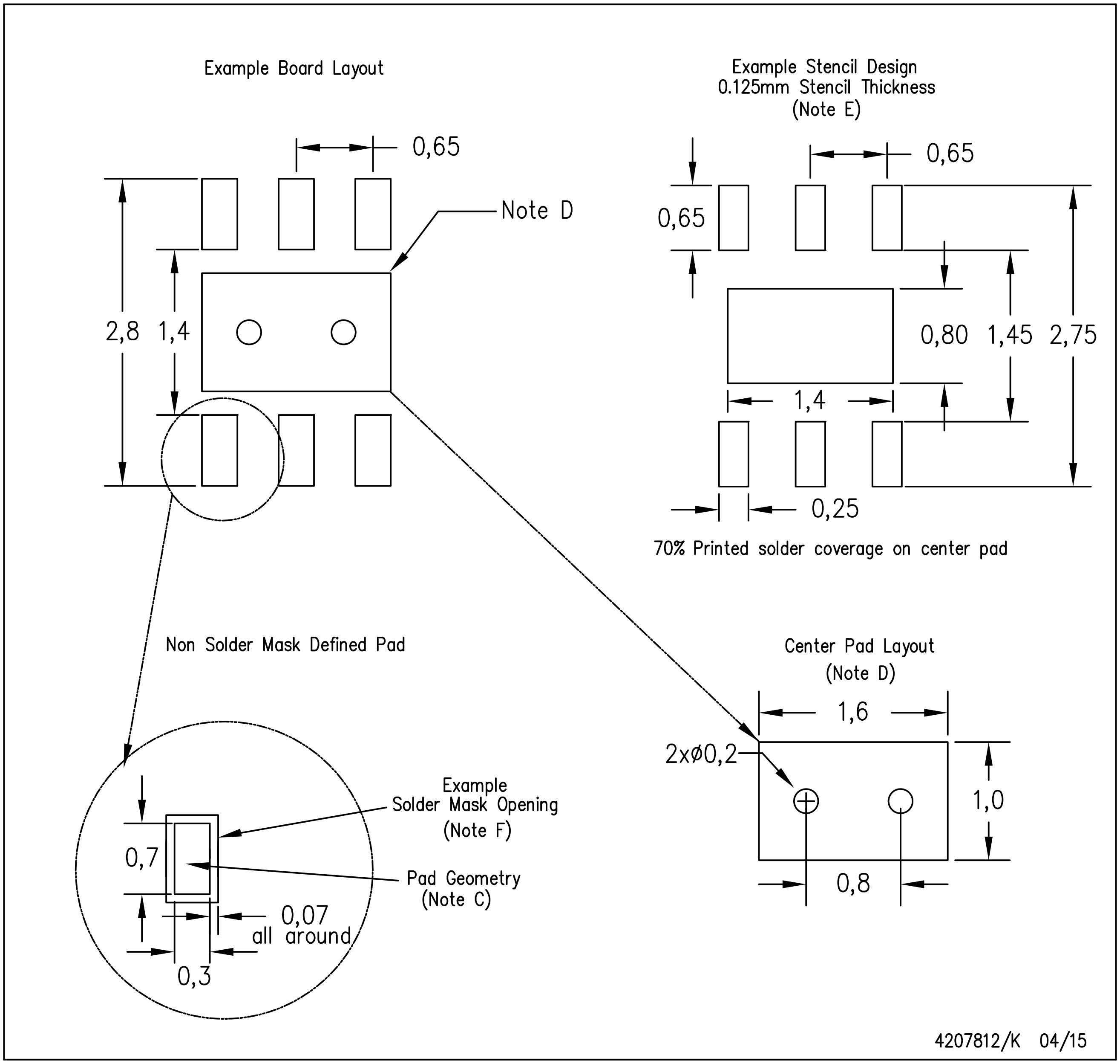
Bottom View

Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

DRV (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Publication IPC-7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

F. Customers should contact their board fabrication site for solder mask tolerances.