4.5V to 18V Input, 2-A Synchronous Step-Down SWIFT™ Converter with Eco-Mode™

Check for Samples: TPS54226

FEATURES

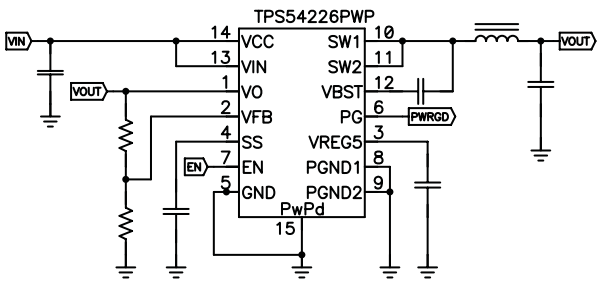
- **D-CAP2™ Mode Enables Fast Transient Response**
- **Low Output Ripple and Allows Ceramic Output Capacitor**
- **Wide V_{CC} Input Voltage Range: 4.5 V to 18 V**
- **Wide V_{IN} Input Voltage Range: 2 V to 18 V**
- **Output Voltage Range: 0.76 V to 5.5 V**
- **Highly Efficient Integrated FET's Optimized for Lower Duty Cycle Applications**
  – 160 mΩ (High Side) and 110 mΩ (Low Side)
- **High Efficiency, less than 10 μA at shutdown**
- **Auto-Skip Eco-Mode™ for High Efficiency at Light Load**
- **High Initial Bandgap Reference Accuracy**
- **Adjustable Soft Start**
- **Pre-Biased Soft Start**
- **700-kHz Switching Frequency (f_{SW})**
- **Cycle By Cycle Over Current Limit**
- **Power Good Output**
- **Auto-Skip Mode**

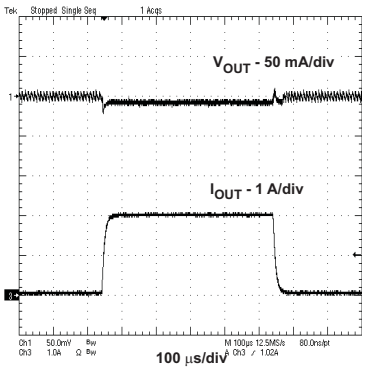
APPLICATIONS

- **Wide Range of Applications for Low Voltage System**
  - **Digital TV Power Supply**
  - **High Definition Blu-ray Disc™ Players**
  - **Networking Home Terminal**
  - **Digital Set Top Box (STB)**

DESCRIPTION

The TPS54226 is a adaptive on-time D-CAP2™ mode synchronous buck converter. TheTPS54226 enables system designers to complete the suite of various end equipment's power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS54226 uses the D-CAP2™ mode control which provides a fast transient response with no external compensation components. The adoptive on-time control supports seamless operation between PWM mode at heavy load condition and reduced frequency Eco-Mode™ operation at light load for high efficiency. The TPS54226 also has a proprietary circuit that enables the device to adopt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18-V VCC input, and from 2-V to 18-V VIN input power supply voltage. The output voltage can be programmed between 0.76 V and 5.5 V. The device also features an adjustable slow start time and a power good function. The TPS54226 is available in the 14 pin HTSSOP or 16 pin QFN package, and designed to operate from –40°C to 85°C.





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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE(2) (3)	ORDERABLE PART NUMBER	PIN	TRANSPORT MEDIA
–40°C to 85°C	PowerPAD™ (HTSSOP) – PWP	TPS54226PWP	14	Tube
		TPS54226PWPR		Tape and Reel
	Plastic Quad Flat Pack (QFN)	TPS54226RGTT	16	Tape and Reel
		TPS54226RGTR		Tape and Reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) All package options have Cu NIPDAU lead/ball finish.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			VALUE	UNIT
V_I	Input voltage range	V_{IN}, V_{CC}, EN	–0.3 to 20	V
		V_{BST}	–0.3 to 26	V
		V_{BST} (vs SW1, SW2)	–0.3 to 6.5	V
		V_{FB}, V_O, SS, PG	–0.3 to 6.5	V
		SW1, SW2	–2 to 20	V
		SW1, SW2 (10 ns transient)	–3 to 20	V
V_O	Output voltage range	V_{REG5}	–0.3 to 6.5	V
		P_{GND1}, P_{GND2}	–0.3 to 0.3	V
I_O	Output current range	I_{VREG5}		
V_{diff}	Voltage from GND to POWERPAD		–0.2 to 0.2	V
ESD rating	Electrostatic discharge	Human Body Model (HBM)	2	kV
		Charged Device Model (CDM)	500	V
T_J	Operating junction temperature		–40 to 150	°C
T_{stg}	Storage temperature		–55 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS54226 PWP 14 PINS	TPS54226 RGT 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	55.6	46.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	51.3	58.1	
θ_{JB}	Junction-to-board thermal resistance	26.4	18.8	
ψ_{JT}	Junction-to-top characterization parameter	1.8	1.3	
ψ_{JB}	Junction-to-board characterization parameter	20.6	18.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(2)	4.3	4.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply input voltage range		4.5	18	V
V_{IN}	Power input voltage range		2	18	V
V_I	Input voltage range	V_{BST}	–0.1	24	V
		V_{BST} (vs SW1, SW2)	–0.1	5.7	
		SS, PG	–0.1	5.7	
		EN	–0.1	18	
		V_O, V_{FB}	–0.1	5.5	
		SW1, SW2	–1.8	18	
		SW1, SW2 (10 ns transient)	–3	18	
		P_{GND1}, P_{GND2}	–0.1	0.1	
V_O	Output voltage range	V_{REG5}	–0.1	5.7	V
I_O	Output Current range	I_{VREG5}	0	10	mA
T_A	Operating free-air temperature		–40	85	°C
T_J	Operating junction temperature		–40	125	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{CC},V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VCC}	Operating - non-switching supply current	V_{CC} current, T_A = 25°C, EN = 5 V, V_{FB} = 0.8 V		800	1200	µA
I_{VCCSDN}	Shutdown supply current	V_{CC} current, T_A = 25°C, EN = 0 V		1.8	10	µA
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage	EN	1.5			V
V_{ENL}	EN low-level input voltage	EN			0.4	V
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V_{FBTH}	V_{FB} threshold voltage	VFB voltage light load mode, T_A = 25°C, V_O = 1.05 V, IO=10mA		771		mV
		T_A = 25°C, V_O = 1.05 V, continuous mode	757	765	773	
		T_A = 0°C to 85°C, V_O = 1.05 V, continuous mode(1)	753		777	
		T_A = –40°C to 85°C, V_O = 1.05 V, continuous mode(1)	751		779	
I_{VFB}	V_{FB} input current	V_{FB} = 0.8 V, T_A = 25°C		0	±0.1	µA
R_{Dischg}	V_O discharge resistance	EN = 0 V, V_O = 0.5 V, T_A = 25°C		50	100	Ω
V_{REG5} OUTPUT						
V_{VREG5}	V_{REG5} output voltage	T_A = 25°C, 6 V < V_{CC} < 18 V, 0 < I_{VREG5} < 5 mA	5.3	5.5	5.7	V
V_{LN5}	Line regulation	6.0 V < V_{CC} < 18 V, I_{VREG5} = 5 mA			20	mV
V_{LD5}	Load regulation	0 mA < I_{VREG5} < 5 mA			100	mV
I_{VREG5}	Output current	V_{CC} = 6 V, V_{REG5} = 4 V, T_A = 25°C		70		mA
MOSFET						
R_{dsonh}	High side switch resistance	25°C, V_{BST} - SW1,2 = 5.5 V		160		mΩ
R_{dsonl}	Low side switch resistance	25°C		110		mΩ
CURRENT LIMIT						
I_{ocl}	Current limit	L out = 2.2 µH(1)	2.5	3.1	4.5	A

(1) Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

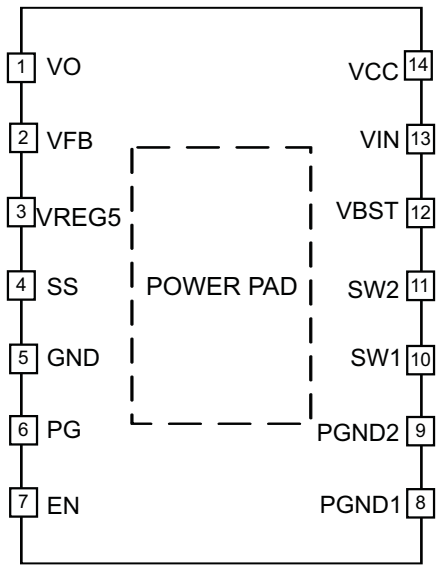
over operating free-air temperature range, V_{CC},V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature (2)		150		°C
		Hysteresis (2)		25		
ON-TIME TIMER CONTROL						
T_{ON}	On time	V_{IN} = 12 V, V_O = 1.05 V		145		ns
$T_{OFF(MIN)}$	Minimum off time	T_A = 25°C, V_{FB} = 0.7 V		260	310	ns
SOFT START						
I_{SSC}	SS charge current	V_{SS} = 0 V	1.4	2.0	2.6	µA
I_{SSD}	SS discharge current	V_{SS} = 0.5 V	0.1	0.2		mA
POWER GOOD						
V_{THPG}	PG threshold	V_{FB} rising (good)	85	90	95	%
		V_{FB} falling (fault)		85		%
I_{PG}	PG sink current	PG = 0.5 V	2.5	5		mA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect	115	120	125	%
T_{OVPDEL}	Output OVP prop delay			5		µs
V_{UVP}	Output UVP trip threshold	UVP detect	65	70	75	%
		Hysteresis		10		%
T_{UVPDEL}	Output UVP delay			0.25		ms
T_{UVPEN}	Output UVP enable delay	Relative to soft-start time		x 1.7		
UVLO						
V_{UVLO}	UVLO threshold	Wake up V_{REG5} voltage	3.55	3.8	4.05	V
		Hysteresis V_{REG5} voltage	0.23	0.35	0.47	

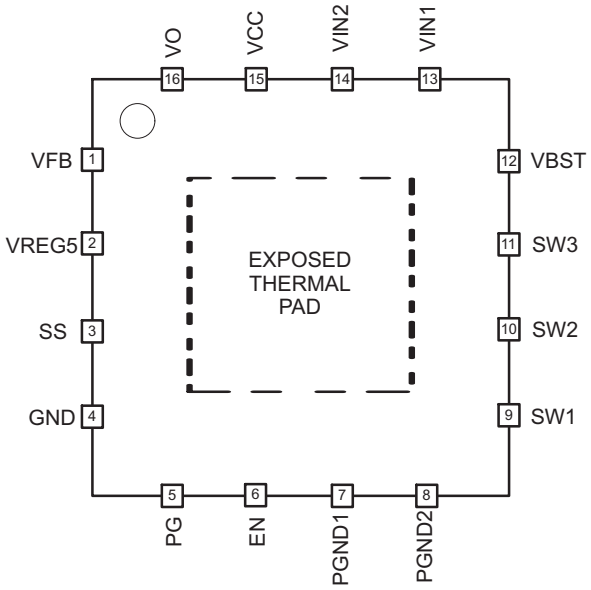
(2) Not production tested.

DEVICE INFORMATION

PWP PACKAGE
(TOP VIEW)



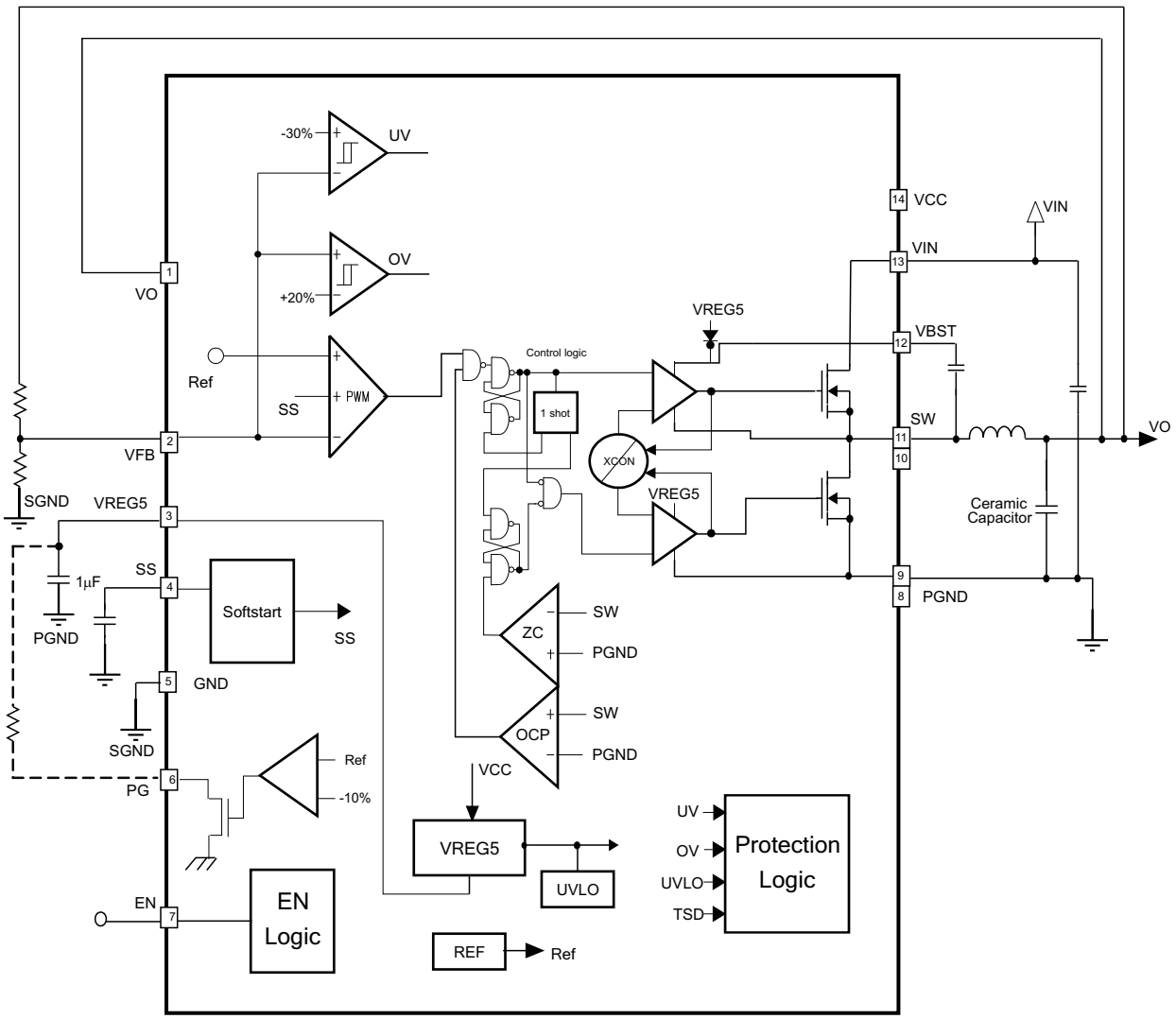
RGT PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN			DESCRIPTION
NAME	PWP 14	RGT 16	
VO	1	16	Connect to output of converter. This pin is used for On-Time Adjustment.
VFB	2	1	Converter feedback input. Connect with feedback resistor divider.
VREG5	3	2	5.5 V power supply output. A capacitor (typical 1µF) should be connected to GND.
SS	4	3	Soft-start control. A external capacitor should be connected to GND.
GND	5	4	Signal ground pin
PG	6	5	Open drain power good output
EN	7	6	Enable control input
PGND1, PGND2	8, 9	7, 8	Ground returns for low-side MOSFET. Also serve as inputs of current comparators. Connect PGND and GND strongly together near the IC.
SW1, SW2	10, 11	9, 10, 11	Switch node connection between high-side NFET and low-side NFET. Also serve as inputs to current comparators.
VBST	12	12	Supply input for high-side NFET gate driver (boost terminal). Connect capacitor from this pin to respective SW1, SW2 terminals. An internal PN diode is connected between VREG5 to VBST pin.
VIN	13	13, 14	Power input and connected to high side NFET drain
VCC	14	15	Supply input for 5 V internal linear regulator for the control circuitry
Exposed Thermal Pad or PowerPAD™	Back side	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Should be connected to PGND.

FUNCTIONAL BLOCK DIAGRAM



A. Block diagram shown is for PWP 14 pin package. QFN 16 pin package block diagram is identical except for pin out.

OVERVIEW

The TPS54226 is a 2-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs and Auto-Skip Eco-Mode™ to improve light lode efficiency. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

DETAILED DESCRIPTION

PWM Operation

The main control loop of the TPS54226 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one

shot timer expires. This one shot is set by the converter input voltage, VIN, and the output voltage, VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

PWM Frequency and Adaptive On-Time Control

TPS54226 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54226 runs with a pseudo-constant frequency of 700 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

Auto-Skip Eco-Mode™ Control

The TPS54226 is designed with Auto-Skip Eco-Mode™ to increase light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept almost the same as is was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \bullet L \bullet f_{ws}} \bullet \frac{(V_{IN} - V_{OUT}) \bullet V_{OUT}}{V_{IN}} \quad (1)$$

Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 2-µA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in Equation 2. VFB voltage is 0.765 V and SS pin source current is 2 µA.

$$Tss(ms) = \frac{C6(nF) \bullet Vref}{Iss(\mu A)} = \frac{C6(nF) \bullet 0.765}{2} \quad (2)$$

A unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage V_{FB}), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage (VO) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

Power Good

The power good function is activated after soft start has finished. The power good function becomes active after 1.7 times soft-start time. When the output voltage is within –10% of the target value, internal comparators detect power good state and the power good signal becomes high. Rpg resister value, which is connected between PG and VREG5, is required from 20 kΩ to 150 kΩ. If the feedback voltage goes under 15% of the target value, the power good signal becomes low after a 10 ms internal delay.

Output Discharge Control

TPS54226 discharges the output when EN is low, or the controller is turned off by the protection functions (OVP, UVP, UVLO and thermal shutdown). The output is discharged by an internal 50-Ω MOSFET which is connected from VO to PGND. The internal low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output.

Current Protection

The output over-current protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by Vin, Vout, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current Iout. If the measured voltage is above the voltage proportional to the current limit, then the device constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time.

The converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over-current protection. The load current one half of the peak-to-peak inductor current higher than the over-current threshold. Also when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output under-voltage protection circuit to be activated. When the over current condition is removed, the output voltage returns to the regulated value. This protection is non-latching.

Over/Under Voltage Protection

The TPS54226 detects over and undervoltage conditions by monitoring the feedback voltage (VFB). This function is enabled after approximately 1.7 times the soft-start time. When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches the high-side MOSFET driver turns off and the low-side MOSFET turns on. When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins. After 250 µs, the device latches off both internal top and bottom MOSFET.

UVLO Protection

Undervoltage lock out protection (UVLO) monitors the voltage of the V_{REG5} pin. When the V_{REG5} voltage is lower than UVLO threshold voltage, the TPS54226 is shut off. This is protection is non-latching.

Thermal Shutdown

Thermal protection is self-activating. If the junction temperature exceeds the threshold value (typically 150°C), the TPS54226 shuts off. This protection is non-latching.

TYPICAL CHARACTERISTICS

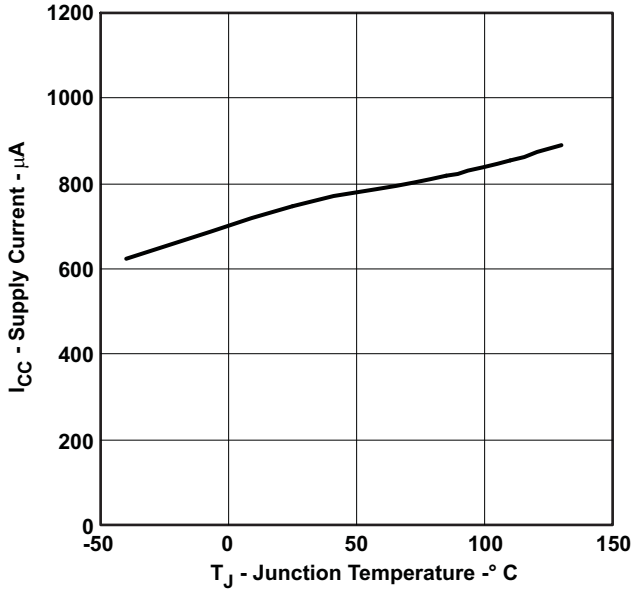


Figure 1. V_{CC} CURRENT vs JUNCTION TEMPERATURE

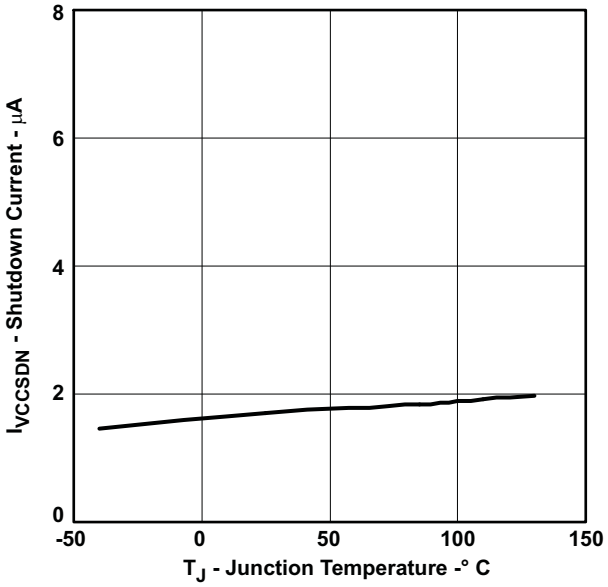


Figure 2. V_{CC} SHUTDOWN CURRENT vs JUNCTION TEMPERATURE

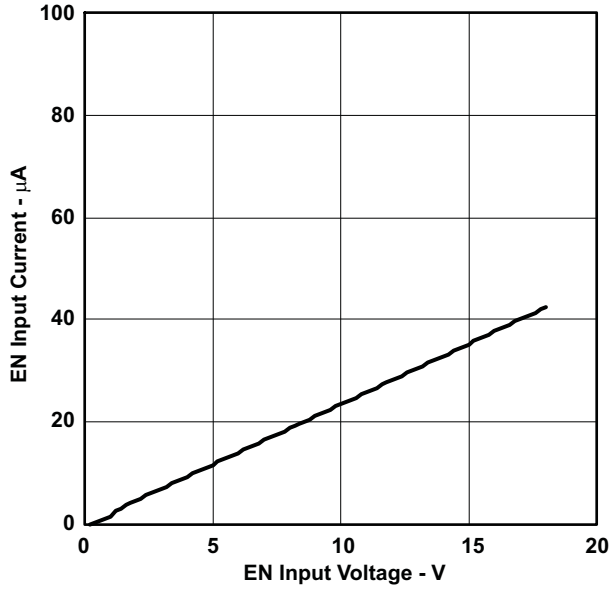


Figure 3. EN CURRENT vs EN VOLTAGE

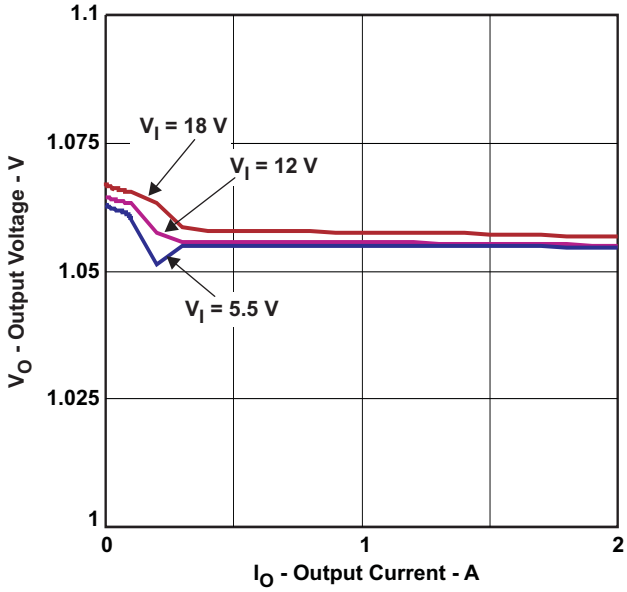


Figure 4. 1.05-V OUTPUT VOLTAGE vs OUTPUT CURRENT

TYPICAL CHARACTERISTICS (continued)

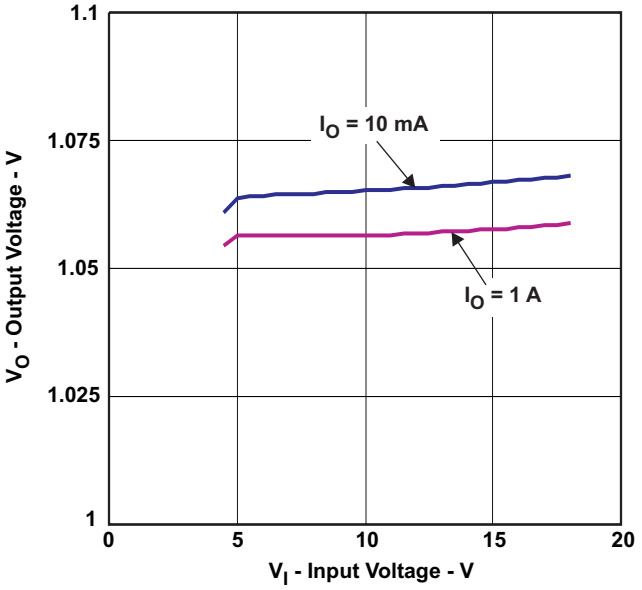


Figure 5. 1.05-V OUTPUT VOLTAGE vs INPUT VOLTAGE

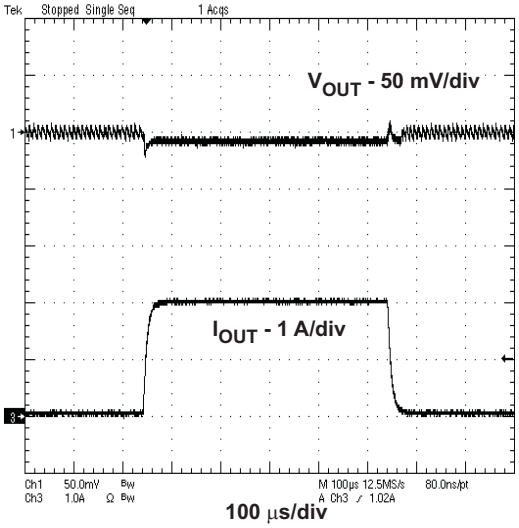


Figure 6. 1.05 V 50 mA TO 2A LOAD TRANSIENT RESPONSE

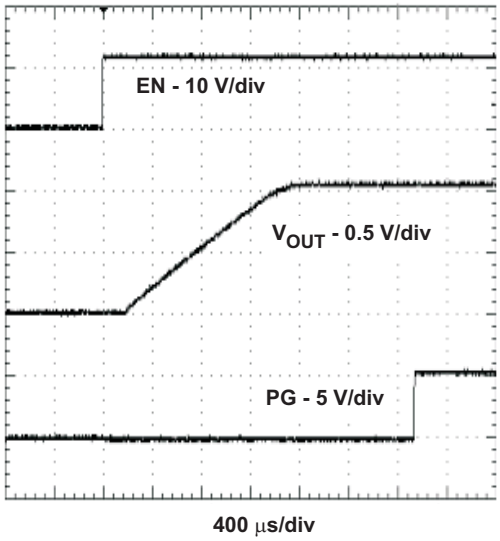


Figure 7. START-UP WAVE FORM

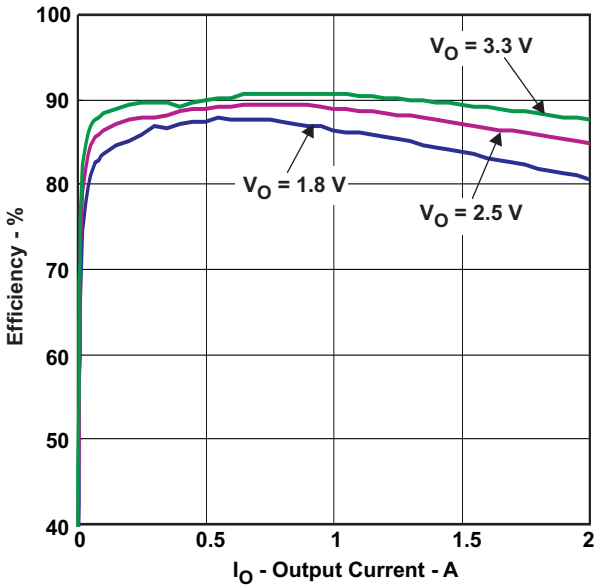


Figure 8. EFFICIENCY vs OUTPUT CURRENT

TYPICAL CHARACTERISTICS (continued)

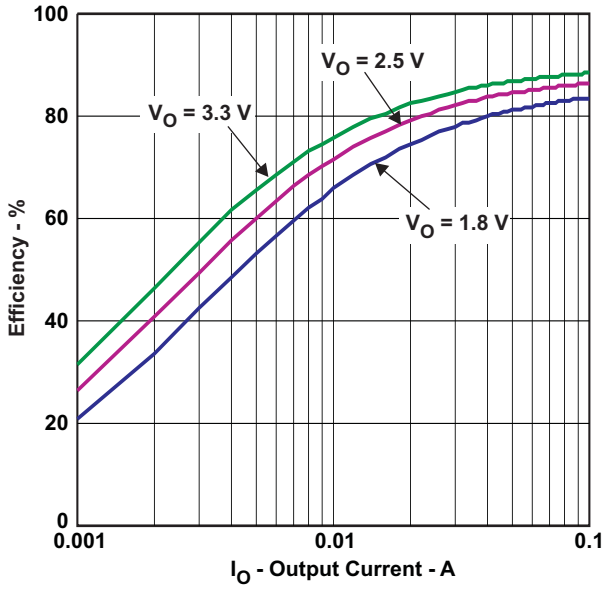


Figure 9. LIGHT LOAD EFFICIENCY vs OUTPUT CURRENT

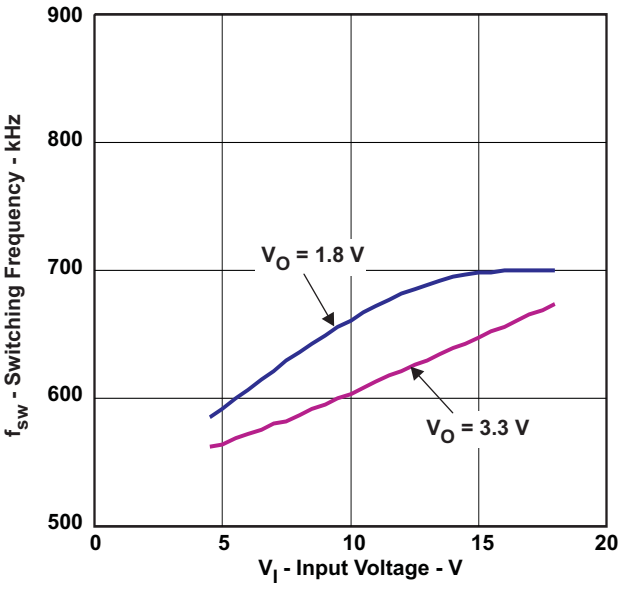


Figure 10. SWITCHING FREQUENCY vs INPUT VOLTAGE (I_O=1 A)

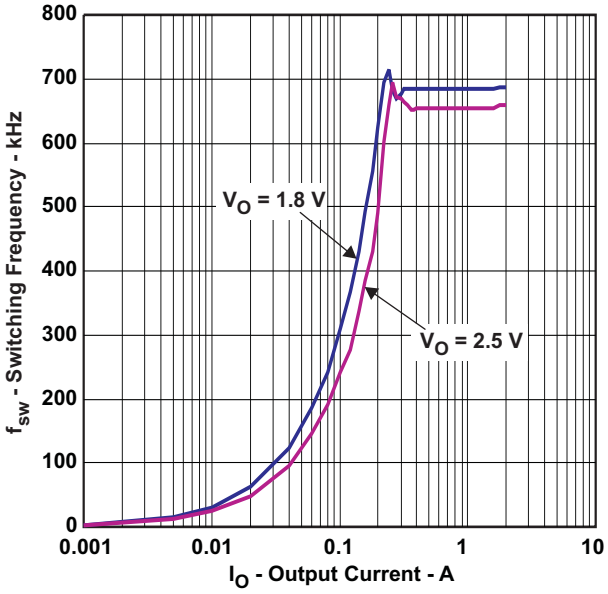


Figure 11. SWITCHING FREQUENCY vs OUTPUT CURRENT

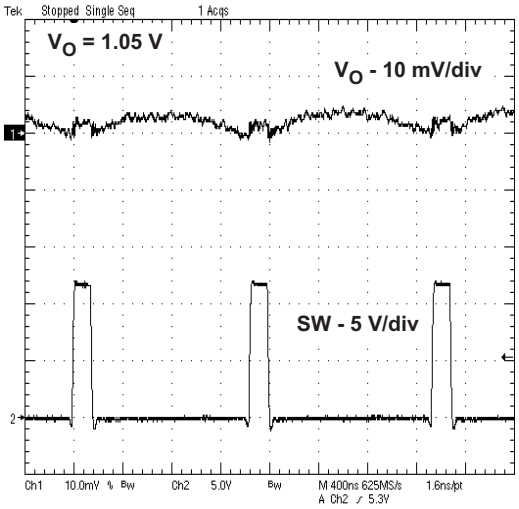


Figure 12. VOLTAGE RIPPLE AT OUTPUT (IO=2A)

TYPICAL CHARACTERISTICS (continued)

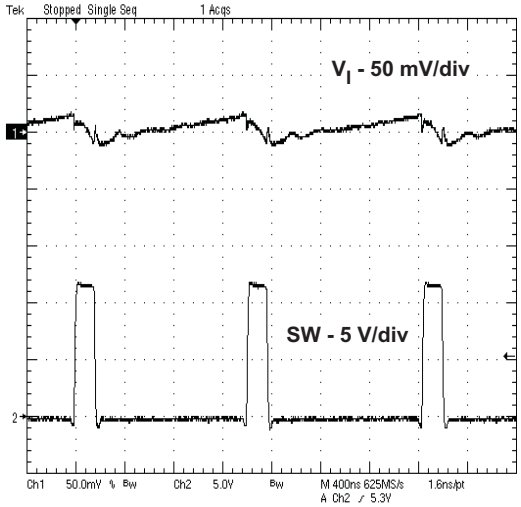


Figure 13. VOLTAGE RIPPLE AT INPUT (IO=2A)

DESIGN GUIDE

Step By Step Design Procedure

To begin the design process, the following application parameters must be known:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple

Figure 14 shows the schematic diagram for this design example.

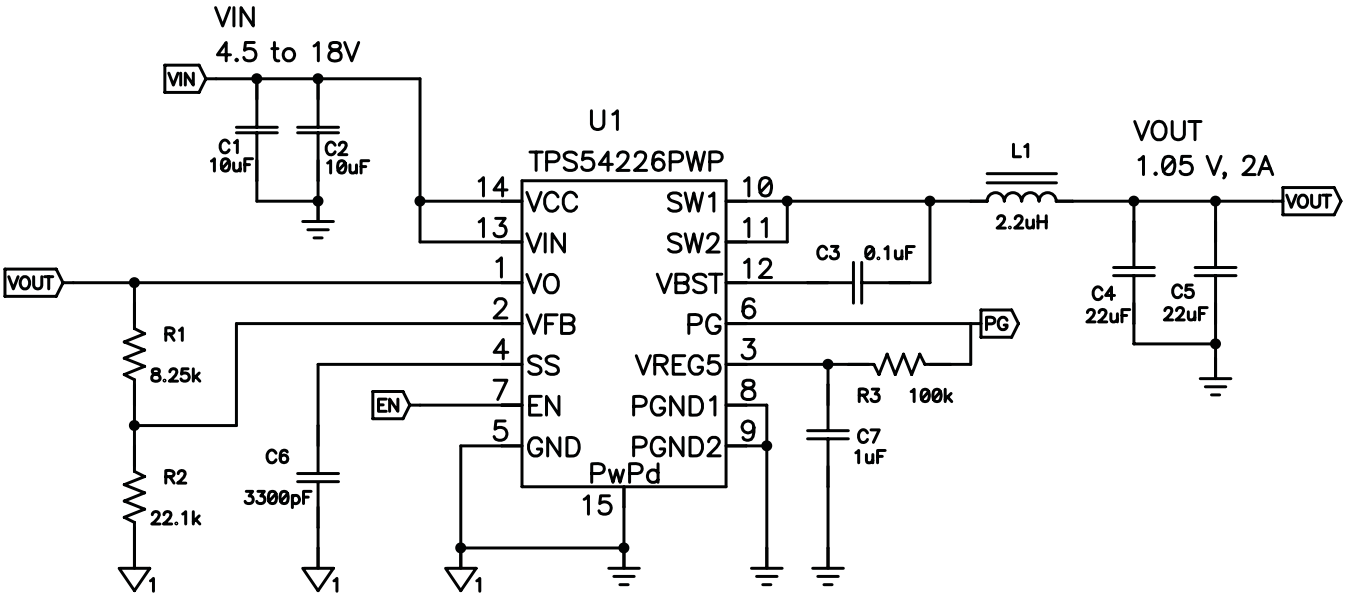


Figure 14. Schematic Diagram

Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation 3 and Equation 4 to calculate V_{OUT}.

To improve efficiency at very light loads consider using larger value resistors, too high of resistance is more susceptible to noise and voltage errors from the VFB input current are more noticeable.

For output voltage from 0.76 V to 2.5 V:

$$V_{OUT} = 0.765 \bullet \left(1 + \frac{R1}{R2}\right) \quad (3)$$

For output voltage over 2.5 V:

$$V_{OUT} = (0.763 + 0.0017 \bullet V_{OUT\_SET}) \bullet \left(1 + \frac{R1}{R2}\right) \quad (4)$$

Where:

V_{OUT_SET} = Target V_{OUT} voltage

Output Filter Selection

The output filter used with the TPS54226 is an LC circuit. This LC filter has double pole at:

$$F_P = \frac{1}{2\pi \sqrt{L_{OUT} \times C_{OUT}}} \quad (5)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54226. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a -40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to -20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 5 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 1.

Table 1. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF)(1)	L1 (µH)	C8 + C9 (µF)
1	6.81	22.1		2.2	22 - 68
1.05	8.25	22.1		2.2	22 - 68
1.2	12.7	22.1		2.2	22 - 68
1.8	30.1	22.1	10 - 47	3.3	22 - 68
2.5	49.9	22.1	10 - 47	3.3	22 - 68
3.3	73.2	22.1	10 - 47	3.3	22 - 68
5	121	22.1	10 - 47	4.7	22 - 68

(1) Optional

For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1.

The inductor peak-to-peak ripple current, peak current, and RMS current are calculated using Equation 6, Equation 7, and Equation 8. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 700 kHz for f_{SW}.

Use 700 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of Equation 7 and the RMS current of Equation 8.

$$Ilp\text{-}p = \frac{V_{OUT}}{V_{IN\,(max)}} \bullet \frac{V_{IN\,(max)} - V_{OUT}}{L_O \bullet f_{SW}} \quad (6)$$

$$I_{lpeak} = I_O + \frac{Ilp\text{-}p}{2} \quad (7)$$

$$I_{Lo(RMS)} = \sqrt{I_O^2 + \frac{1}{12} Ilp\text{-}p^2} \quad (8)$$

For this design example, the calculated peak current is 2.32 A and the calculated RMS current is 2.01 A. The inductor used is a TDK SPM6530-2R2M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54226 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22 µF to 68 µF. Use Equation 9 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})}{\sqrt{12} \bullet V_{IN} \bullet L_O \bullet f_{SW}} \quad (9)$$

For this design two TDK C3216X5R0J226M 22 µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.271 A and each output capacitor is rated for 4 A.

Input Capacitor Selection

The TPS54226 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. An additional 0.1 µF capacitor from pin 14 to ground is recommended to improve the stability of the over-current limit function. The capacitor voltage rating needs to be greater than the maximum input voltage.

Bootstrap Capacitor Selection

A 0.1 µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

VREG5 Capacitor Selection

A 1.0 µF ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. It is recommended to use a ceramic capacitor.

THERMAL INFORMATION

The PWP 14 pin package incorporates an exposed PowerPAD™ and the QFN 16 pin package incorporates a similar exposed thermal pad. These exposed thermal pads are designed to be connected to an external heatsink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD™ package and how to use the advantage of its heat dissipating abilities, see Technical Brief, PowerPAD™ Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD™ Made Easy, Texas Instruments Literature No. SLMA004.

The exposed thermal pad dimensions for the PWP 14 pin and QFN 16 pin packages are shown in the Thermal Pad Mechanical Data section of this data sheet.

LAYOUT CONSIDERATIONS

The following layout guidelines are provided using the PWP 14 pin package as an example. The general guidelines and routing are also applicable to the QFN 16 pin package. Allowance should be made for the differences in the package pin configurations.

1. Keep the input switching current loop as small as possible.
2. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.
3. Keep analog and non-switching components away from switching components.
4. Make a single point connection from the signal ground to power ground.
5. Do not allow switching current to flow under the device.
6. Keep the pattern lines for VIN and PGND broad.
7. Exposed pad of device must be connected to PGND with solder.
8. VREG5 capacitor should be placed near the device, and connected PGND.
9. Output capacitor should be connected to a broad pattern of the PGND.
10. Voltage feedback loop should be as short as possible, and preferably with ground shield.
11. Lower resistor of the voltage divider which is connected to the VFB pin should be tied to SGND.
12. Providing sufficient via is preferable for VIN, SW and PGND connection.
13. PCB pattern for VIN, SW, and PGND should be as broad as possible.
14. If VIN and VCC is shorted, VIN and VCC patterns need to be connected with broad pattern lines.
15. VIN Capacitor should be placed as near as possible to the device.

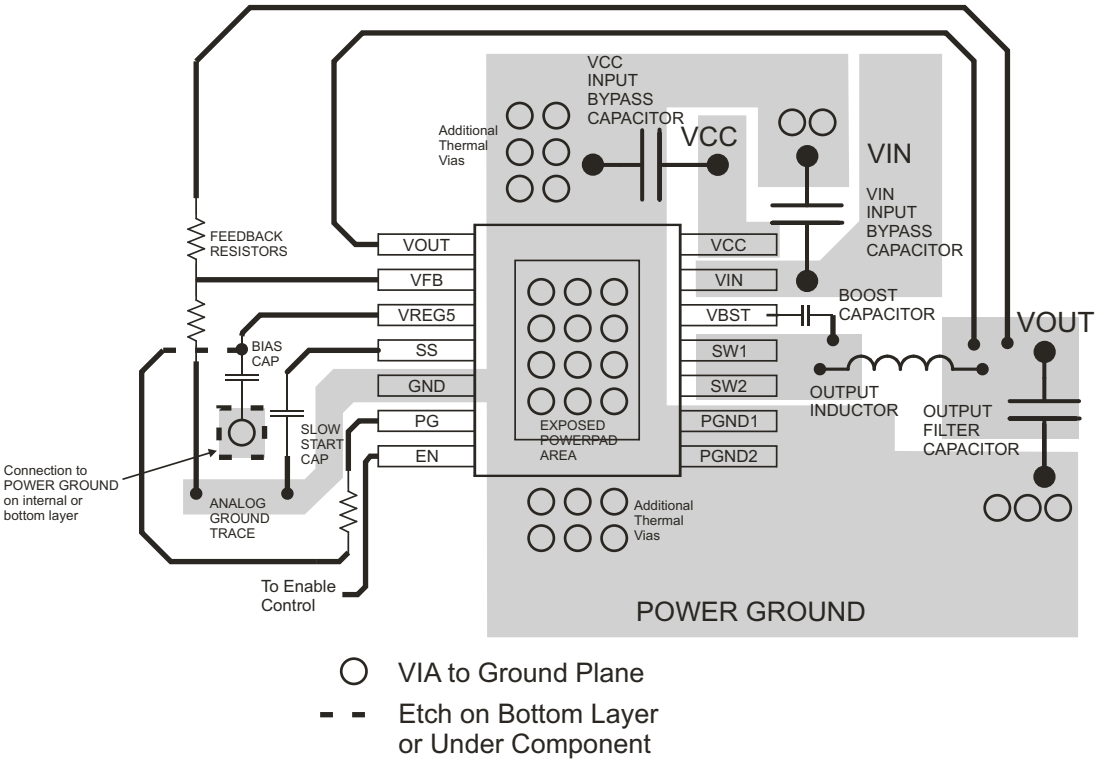


Figure 15. TPS54226 Layout

REVISION HISTORY

Changes from Original (October 2009) to Revision A **Page**

- Changed the device from Product Preview to Production 1

Changes from Revision A (October 2009) to Revision B **Page**

- Changed the title to include Eco-Mode 1
- Changed features bullet to reference Eco-Mode 1
- Added Eco-Mode text to the DESCRIPTION 1
- Added the QFN package to the DESCRIPTION 1
- Added the QFN package to the ORDERING INFORMATION table 2
- Added the RGT PACKAGE drawing 5
- Added the RGT 16 pin column to the PIN FUNCTIONS table 5
- Updated the FUNCTIONAL BLOCK DIAGRAM 6
- Added text Note to the FUNCTIONAL BLOCK DIAGRAM 6
- Added Eco-Mode text to the OVERVIEW section 6
- Changed section title From: Light Load Mode Control To: Light Load Eco-Mode Control 7
- Added Eco-Mode to text in the Light Load Eco-Mode Control section 7
- Added Note 1 to Table 1 14
- Added text to the THERMAL INFORMATION section for the QFN package 15
- Deleted figure "Thermal Pad Dimensions" 15

Changes from Revision B (June 2010) to Revision C **Page**

- Changed TPS54226PWPR tape and reel quantity From: 3000 To: 2000 2
- Added V_{CC},V_{IN} = 12V to the conditions statement in the Electrical Characteristics table 3

Changes from Revision C (October 2010) to Revision D **Page**

- Changed –45°C to 85°C to –40°C to 85°C in Ordering Information 2
- Deleted quantities from Transport Media column 2
- Added Thermal Information table 2
- Changed EN low-level input voltage max from 0.4 V to 0.48 V 3
- Changed Functional Block Diagram 6
- Changed section title From: Light Load Eco-Mode Control To: Auto-Skip Eco-Mode Control 7
- Added Auto-Skip to text in Auto-Skip Eco-Mode Control section 7
- Changed Equation 1 7
- Changed Power Good section text 7
- Changed Current Protection section text 8
- Changed Design Guide information 13
- Changed C4 values in Table 1 14

Changes from Revision D (February 2011) to Revision E **Page**

- Changed EN high-level input voltage min from 2 V to 1.5 V 3
- Changed EN low-level input voltage max from 0.48 V to 0.4 V 3

Changes from Revision D (February 2011) to Revision E **Page**

- Changed EN high-level input voltage min from 2 V to 1.5 V 3
- Changed EN low-level input voltage max from 0.48 V to 0.4 V 3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54226PWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54226	Samples
TPS54226PWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54226	Samples
TPS54226RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54226	Samples
TPS54226RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54226	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

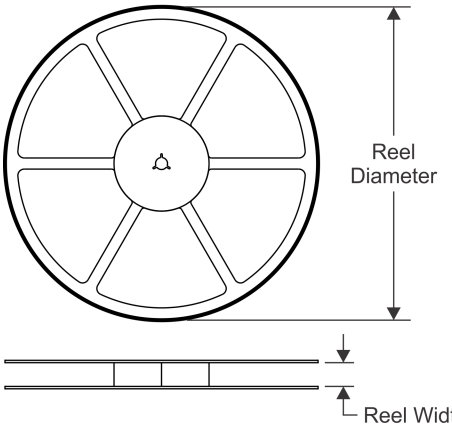
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

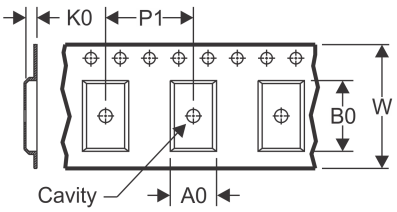
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

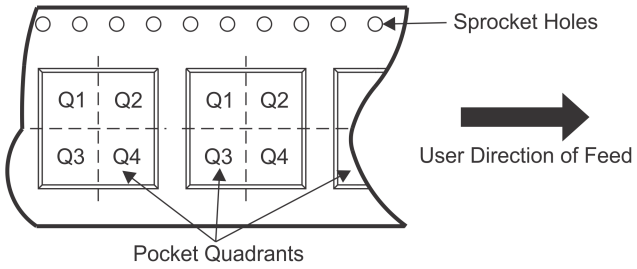


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

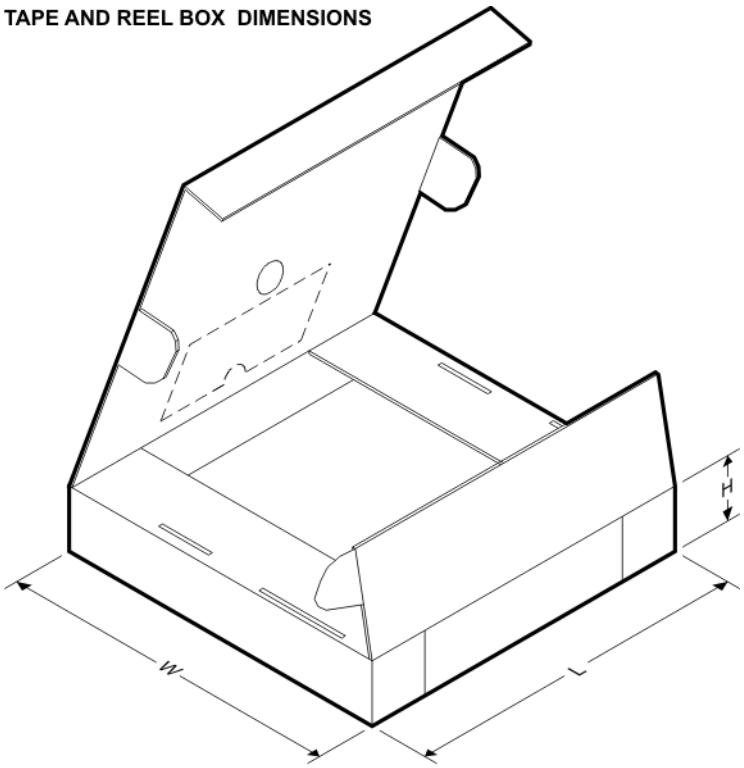
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54226PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS54226PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS54226RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54226RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

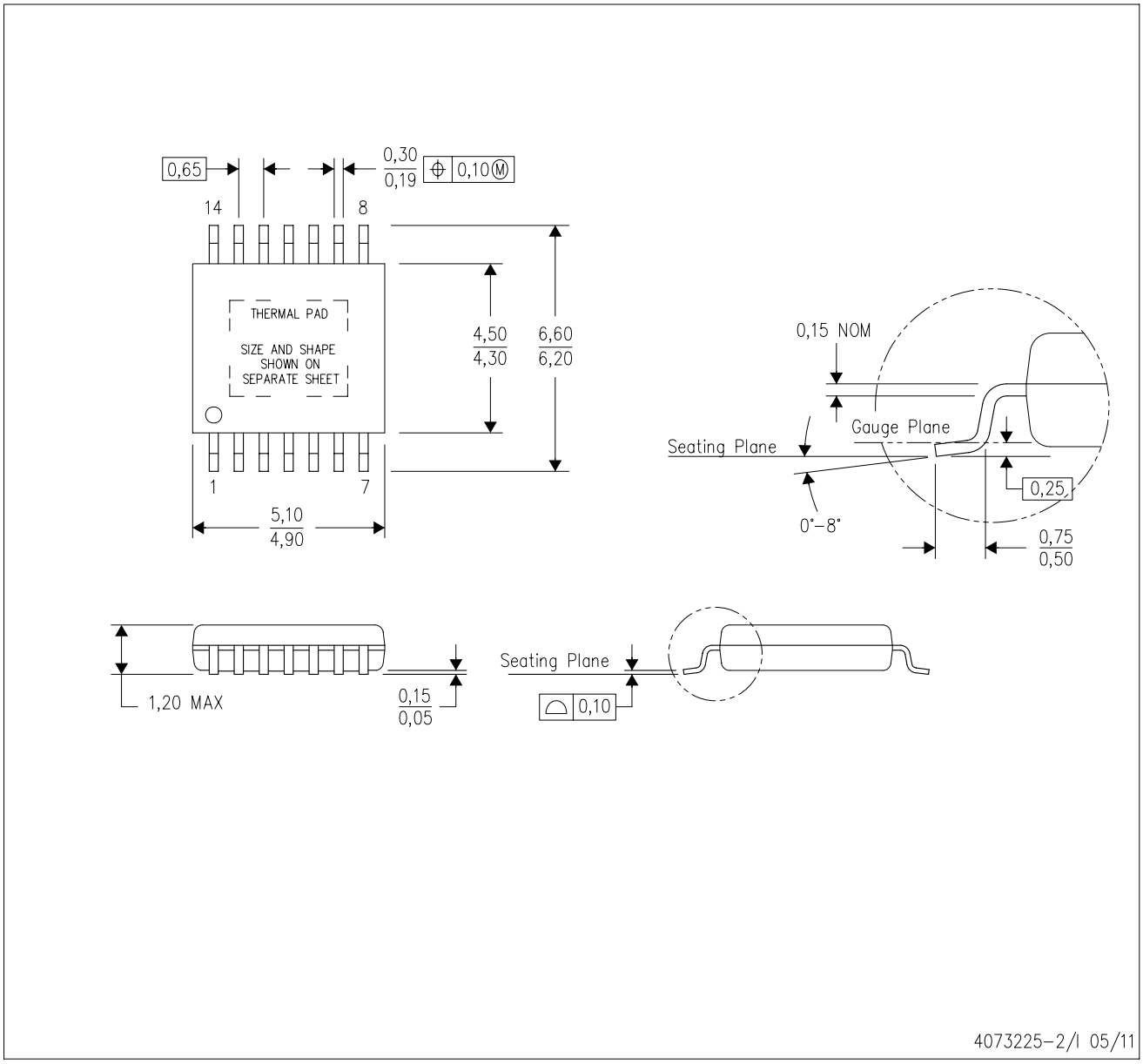
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54226PWPR	HTSSOP	PWP	14	2000	367.0	367.0	38.0
TPS54226PWPR	HTSSOP	PWP	14	2000	367.0	367.0	35.0
TPS54226RGTR	QFN	RGT	16	3000	367.0	367.0	35.0
TPS54226RGTT	QFN	RGT	16	250	210.0	185.0	35.0

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

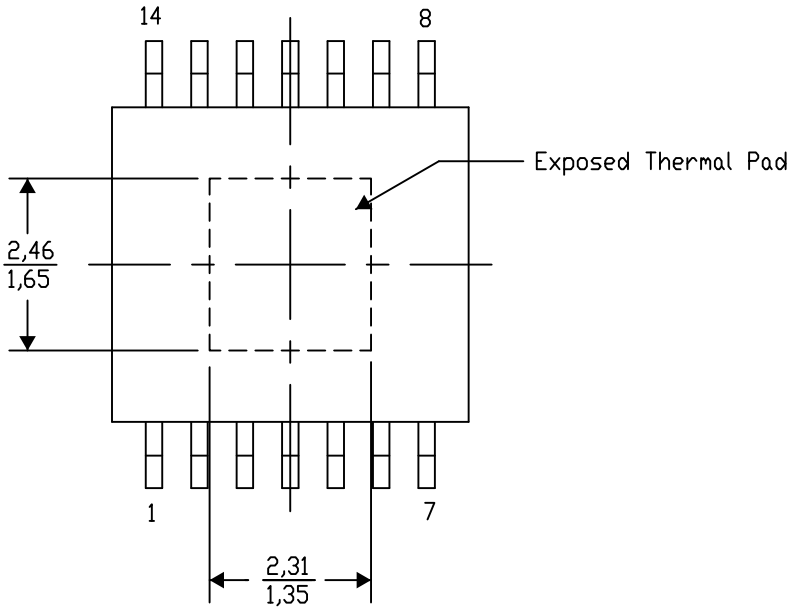
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

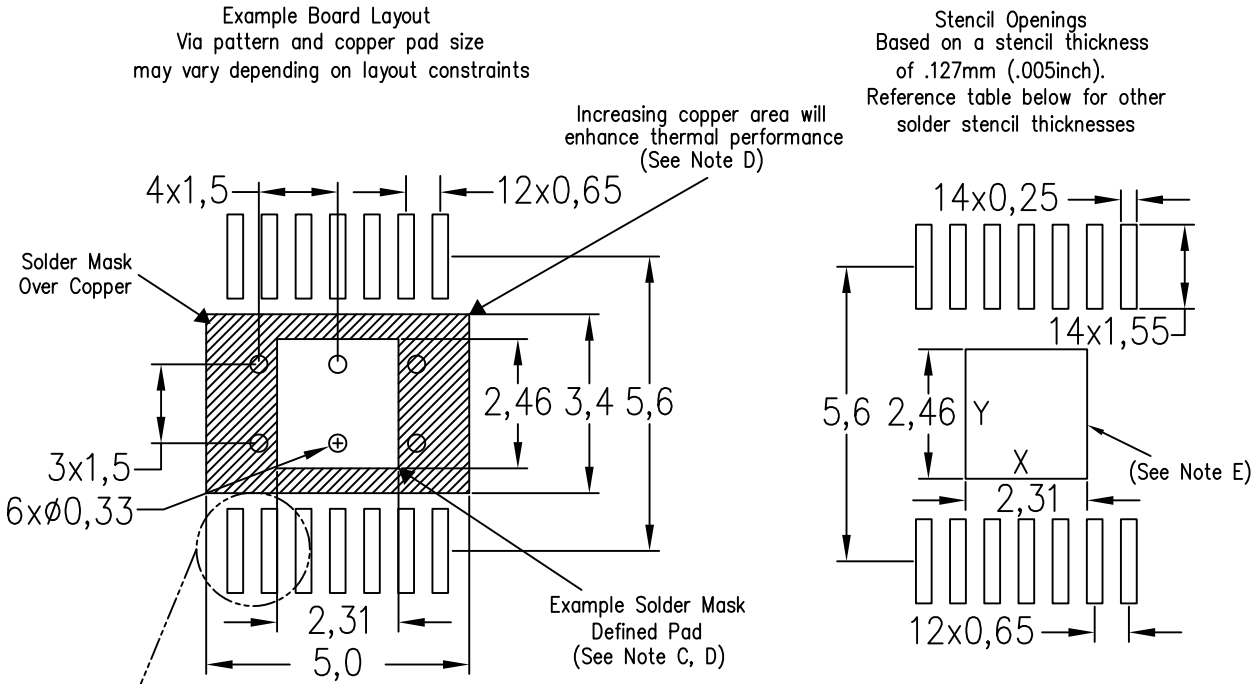
Exposed Thermal Pad Dimensions

4206332–2/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

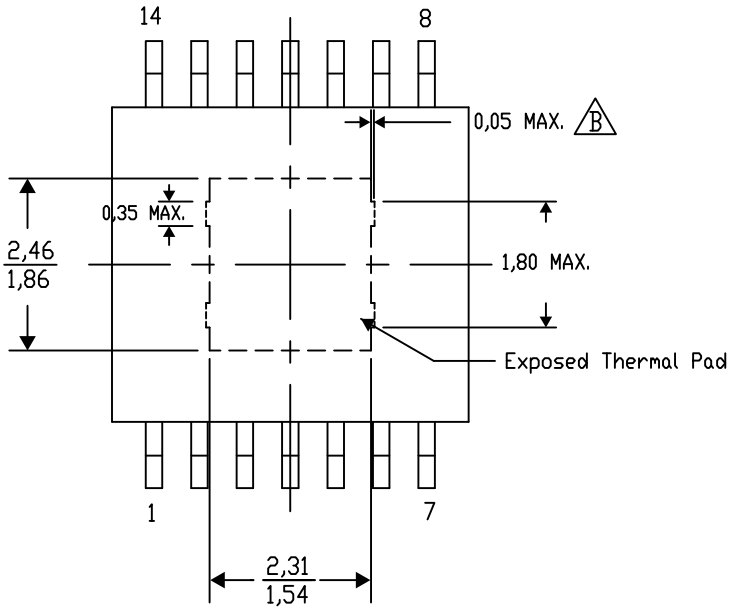
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

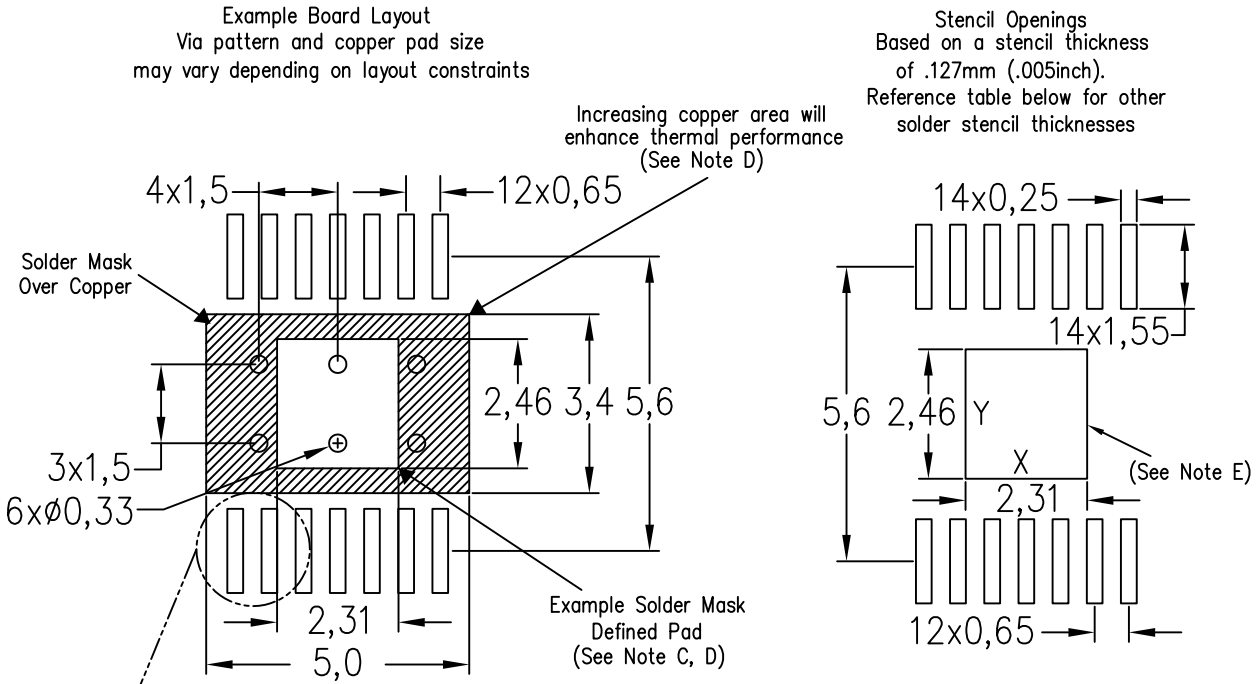
4206332–44/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE

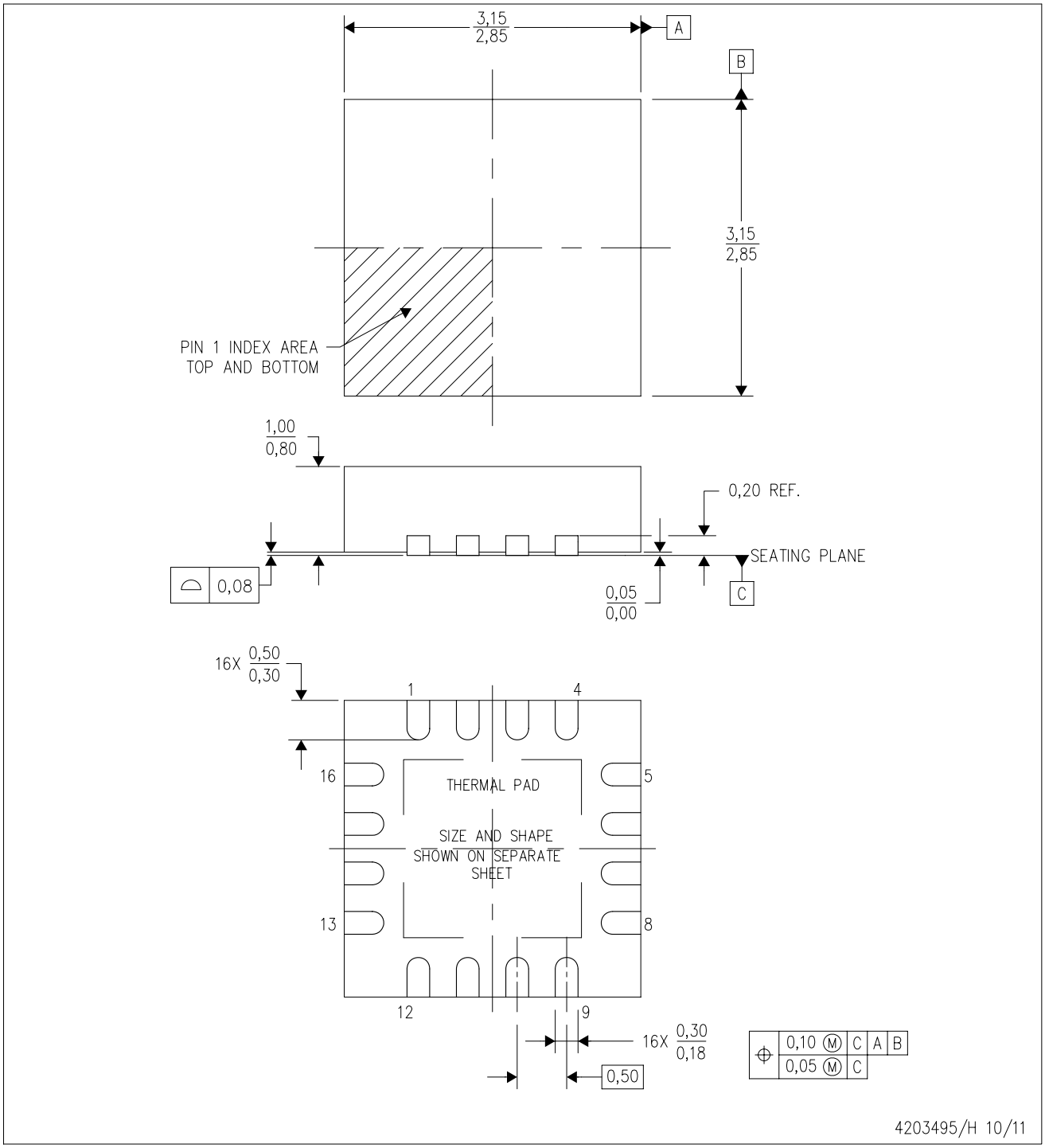


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

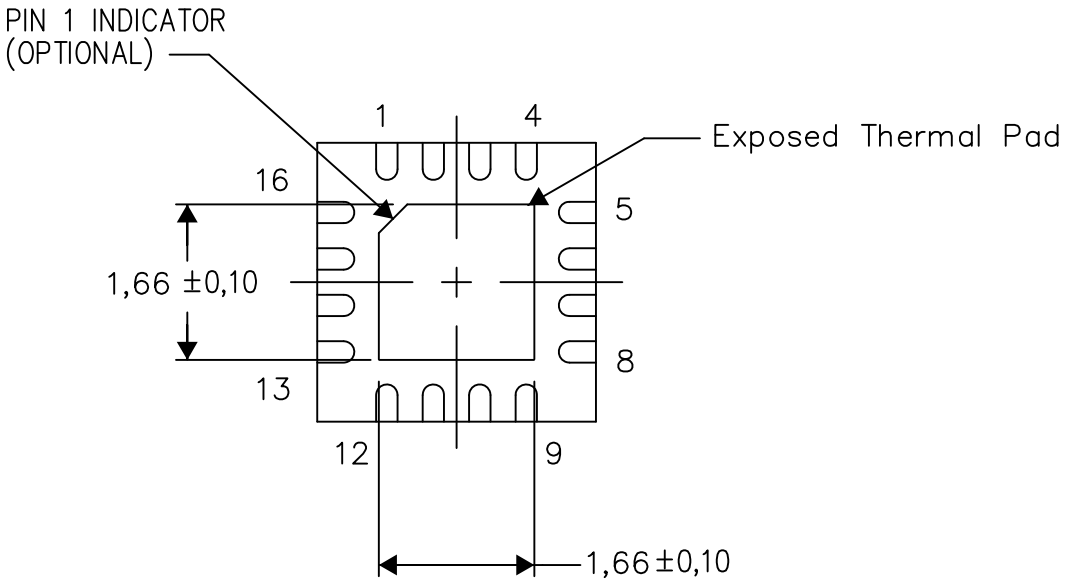
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



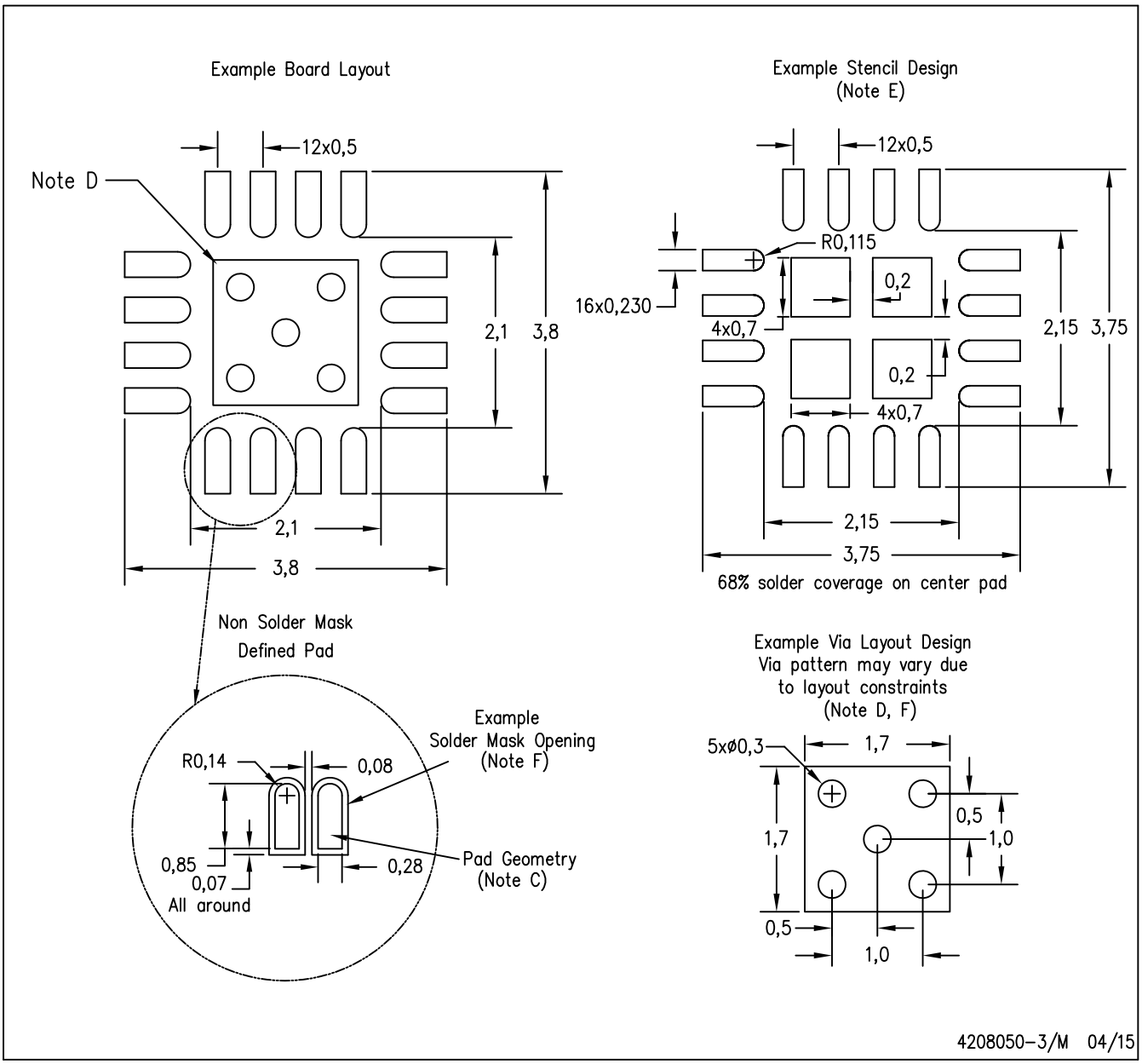
Bottom View

Exposed Thermal Pad Dimensions

4206349–10/Z 08/15

NOTE: All linear dimensions are in millimeters

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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