Low Cost, 80 MHz *Fast*FET Op Amps

AD8033/AD8034

FEATURES

FET input amplifier
- **1 pA typical input bias current**

Very low cost

High speed
- **80 MHz, −3 dB bandwidth (G = +1)**
- **80 V/μs slew rate (G = +2)**

Low noise
- **11 nV/√Hz (f = 100 kHz)**
- **0.7 fA/√Hz (f = 100 kHz)**

Wide supply voltage range: 5 V to 24 V

Low offset voltage: 1 mV typical

Single-supply and rail-to-rail output

High common-mode rejection ratio: −100 dB

Low power: 3.3 mA/amplifier typical supply current

No phase reversal

Small packaging: 8-lead SOIC, 8-lead SOT-23, and 5-lead SC70

APPLICATIONS

Instrumentation

Filters

Level shifting

Buffering

GENERAL DESCRIPTION

The AD8033/AD8034 *Fast*FET™ amplifiers are voltage feedback amplifiers with FET inputs, offering ease of use and excellent performance. The AD8033 is a single amplifier and the AD8034 is a dual amplifier. The AD8033/AD8034 *Fast*FET op amps in Analog Devices, Inc., proprietary XFCB process offer significant performance improvements over other low cost FET amps, such as low noise (11 nV/√Hz and 0.7 fA/√Hz) and high speed (80 MHz bandwidth and 80 V/μs slew rate).

With a wide supply voltage range from 5 V to 24 V and fully operational on a single supply, the AD8033/AD8034 amplifiers work in more applications than similarly priced FET input amplifiers. In addition, the AD8033/AD8034 have rail-to-rail outputs for added versatility.

Despite their low cost, the amplifiers provide excellent overall performance. They offer a high common-mode rejection of −100 dB, low input offset voltage of 2 mV maximum, and low noise of 11 nV/√Hz.

CONNECTION DIAGRAMS

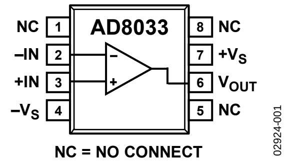

Figure 1. 8-Lead SOIC (R)

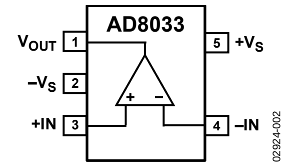

Figure 2. 5-Lead SC70 (KS)

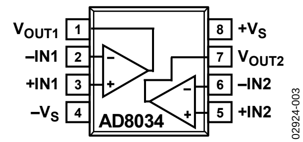

Figure 3. 8-Lead SOIC (R) and 8-Lead SOT-23 (RJ)

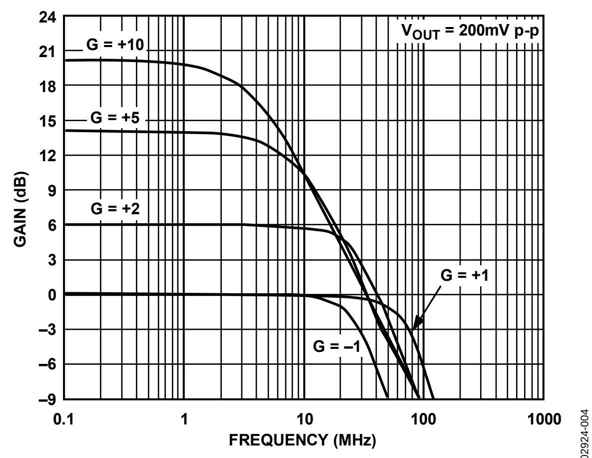

Figure 4. Small Signal Frequency Response

The AD8033/AD8034 amplifiers only draw 3.3 mA/amplifier of quiescent current while having the capability of delivering up to 40 mA of load current.

The AD8033 is available in a small package 8-lead SOIC and a small package 5-lead SC70. The AD8034 is also available in a small package 8-lead SOIC and a small package 8-lead SOT-23. They are rated to work over the industrial temperature range of −40°C to +85°C without a premium over commercial grade products.

Rev. D

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SPECIFICATIONS

T_A = 25°C, V_S = ±5 V, R_L = 1 kΩ, gain = +2, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +1, V_{OUT} = 0.2 V p-p	65	80		MHz
	G = +2, V_{OUT} = 0.2 V p-p		30		MHz
	G = +2, V_{OUT} = 2 V p-p		21		MHz
Input Overdrive Recovery Time	–6 V to +6 V input		135		ns
Output Overdrive Recovery Time	–3 V to +3 V input, G = +2		135		ns
Slew Rate (25% to 75%)	G = +2, V_{OUT} = 4 V step	55	80		V/µs
Settling Time to 0.1%	G = +2, V_{OUT} = 2 V step		95		ns
	G = +2, V_{OUT} = 8 V step		225		ns
NOISE/HARMONIC PERFORMANCE					
Distortion	f_C = 1 MHz, V_{OUT} = 2 V p-p				
Second Harmonic	R_L = 500 Ω		–82		dBc
	R_L = 1 kΩ		–85		dBc
Third Harmonic	R_L = 500 Ω		–70		dBc
	R_L = 1 kΩ		–81		dBc
Crosstalk, Output-to-Output	f = 1 MHz, G = +2		–86		dB
Input Voltage Noise	f = 100 kHz		11		nV/√Hz
Input Current Noise	f = 100 kHz		0.7		fA/√Hz
DC PERFORMANCE					
Input Offset Voltage	V_{CM} = 0 V		1	2	mV
	T_{MIN} – T_{MAX}			3.5	mV
Input Offset Voltage Match				2.5	mV
Input Offset Voltage Drift			4	27	µV/°C
Input Bias Current			1.5	11	pA
	T_{MIN} – T_{MAX}		50		pA
Open-Loop Gain	V_{OUT} = ± 3 V	89	92		dB
INPUT CHARACTERISTICS					
Common-Mode Input Impedance			1000‖2.3		GΩ‖pF
Differential Input Impedance			1000‖1.7		GΩ‖pF
Input Common-Mode Voltage Range					
FET Input Range			–5.0 to +2.2		V
Common-Mode Rejection Ratio	V_{CM} = –3 V to +1.5 V	–89	–100		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing		±4.75	±4.95		V
Output Short-Circuit Current			40		mA
Capacitive Load Drive	30% overshoot, G = +1, V_{OUT} = 400 mV p-p		35		pF
POWER SUPPLY					
Operating Range		5		24	V
Quiescent Current per Amplifier			3.3	3.5	mA
Power Supply Rejection Ratio	V_S = ±2 V	–90	–100		dB

T_A = 25°C, V_S = 5 V, R_L = 1 kΩ, gain = +2, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.2 V p-p	70	80		MHz
	G = +2, V_{OUT} = 0.2 V p-p		32		MHz
	G = +2, V_{OUT} = 2 V p-p		21		MHz
Input Overdrive Recovery Time	−3 V to +3 V input		180		ns
Output Overdrive Recovery Time	−1.5 V to +1.5 V input, G = +2		200		ns
Slew Rate (25% to 75%)	G = +2, V_{OUT} = 4 V step	55	70		V/μs
Settling Time to 0.1%	G = +2, V_{OUT} = 2 V step		100		ns
NOISE/HARMONIC PERFORMANCE					
Distortion	f_C = 1 MHz, V_{OUT} = 2 V p-p				
Second Harmonic	R_L = 500 Ω		−80		dBc
	R_L = 1 kΩ		−84		dBc
Third Harmonic	R_L = 500 Ω		−70		dBc
	R_L = 1 kΩ		−80		dBc
Crosstalk, Output to Output	f = 1 MHz, G = +2		−86		dB
Input Voltage Noise	f = 100 kHz		11		nV/√Hz
Input Current Noise	f = 100 kHz		0.7		fA/√Hz
DC PERFORMANCE					
Input Offset Voltage	V_{CM} = 0 V		1	2	mV
	T_{MIN} – T_{MAX}			3.5	mV
Input Offset Voltage Match				2.5	mV
Input Offset Voltage Drift			4	30	μV/°C
Input Bias Current			1	10	pA
	T_{MIN} – T_{MAX}		50		pA
Open-Loop Gain	V_{OUT} = 0 V to 3 V	87	92		dB
INPUT CHARACTERISTICS					
Common-Mode Input Impedance			1000||2.3		GΩ||pF
Differential Input Impedance			1000||1.7		GΩ||pF
Input Common-Mode Voltage Range					
FET Input Range			0 to 2.0		V
Common-Mode Rejection Ratio	V_{CM} = 1.0 V to 2.5 V	−80	−100		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 1 kΩ	0.16 to 4.83	0.04 to 4.95		V
Output Short-Circuit Current			30		mA
Capacitive Load Drive	30% overshoot, G = +1, V_{OUT} = 400 mV p-p		25		pF
POWER SUPPLY					
Operating Range		5		24	V
Quiescent Current per Amplifier			3.3	3.5	mA
Power Supply Rejection Ratio	V_S = ±1 V	−80	−100		dB

$T_A = 25°C$, $V_S = ±12$ V, $R_L = 1$ kΩ, gain = +2, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.2 V p-p	65	80		MHz
	G = +2, V_{OUT} = 0.2 V p-p		30		MHz
	G = +2, V_{OUT} = 2 V p-p		21		MHz
Input Overdrive Recovery Time	−13 V to +13 V input		100		ns
Output Overdrive Recovery Time	−6.5 V to +6.5 V input, G = +2		100		ns
Slew Rate (25% to 75%)	G = +2, V_{OUT} = 4 V step	55	80		V/µs
Settling Time to 0.1%	G = +2, V_{OUT} = 2 V step		90		ns
	G = +2, V_{OUT} = 10 V step		225		ns
NOISE/HARMONIC PERFORMANCE					
Distortion	f_C = 1 MHz, V_{OUT} = 2 V p-p				
Second Harmonic	R_L = 500 Ω		−80		dBc
	R_L = 1 kΩ		−82		dBc
Third Harmonic	R_L = 500 Ω		−70		dBc
	R_L = 1 kΩ		−82		dBc
Crosstalk, Output to Output	f = 1 MHz, G = +2		−86		dB
Input Voltage Noise	f = 100 kHz		11		nV/√Hz
Input Current Noise	f = 100 kHz		0.7		fA/√Hz
DC PERFORMANCE					
Input Offset Voltage	V_{CM} = 0 V		1	2	mV
	$T_{MIN} – T_{MAX}$			3.5	mV
Input Offset Voltage Match				2.5	mV
Input Offset Voltage Drift			4	24	µV/°C
Input Bias Current			2	12	pA
	$T_{MIN} – T_{MAX}$		50		pA
Open-Loop Gain	V_{OUT} = ±8 V	88	96		dB
INPUT CHARACTERISTICS					
Common-Mode Input Impedance			1000‖2.3		GΩ‖pF
Differential Input Impedance			1000‖1.7		GΩ‖pF
Input Common-Mode Voltage Range					
FET Input Range			−12.0 to +9.0		V
Common-Mode Rejection Ratio	V_{CM} = ±5 V	−92	−100		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing		±11.52	±11.84		V
Output Short-Circuit Current			60		mA
Capacitive Load Drive	30% overshoot, G = +1		35		pF
POWER SUPPLY					
Operating Range		5		24	V
Quiescent Current per Amplifier			3.3	3.5	mA
Power Supply Rejection Ratio	V_S = ±2 V	−85	−100		dB

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	26.4 V
Power Dissipation	See Figure 5
Common-Mode Input Voltage	26.4 V
Differential Input Voltage	1.4 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8033/AD8034 packages is limited by the associated rise in junction temperature (T_J) on the die. The plastic that encapsulates the die locally reaches the junction temperature. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8033/AD8034. Exceeding a junction temperature of 175°C for an extended period can result in changes in silicon devices, potentially causing failure.

The still-air thermal properties of the package and PCB (θ_{JA}), ambient temperature (T_A), and the total power dissipated in the package (P_D) determine the junction temperature of the die. The junction temperature can be calculated as

$$T_J = T_A + (P_D \times \theta_{JA})$$

P_D is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$). The difference between the total drive power and the load power is the drive power dissipated in the package

$$P_D = Quiescent\ Power + (Total\ Drive\ Power - Load\ Power)$$

$$P_D = [V_S \times I_S] + [(V_S/2) \times (V_{OUT}/R_L)] - [V_{OUT}^2/R_L]$$

RMS output voltages should be considered. If R_L is referenced to $-V_S$, as in single-supply operation, the total drive power is $V_S \times I_{OUT}$.

If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply

$$P_D = (V_S \times I_S) + (V_S/4)^2/R_L$$

In single-supply operation with R_L referenced to V_{S-}, worst case is $V_{OUT} = V_S/2$.

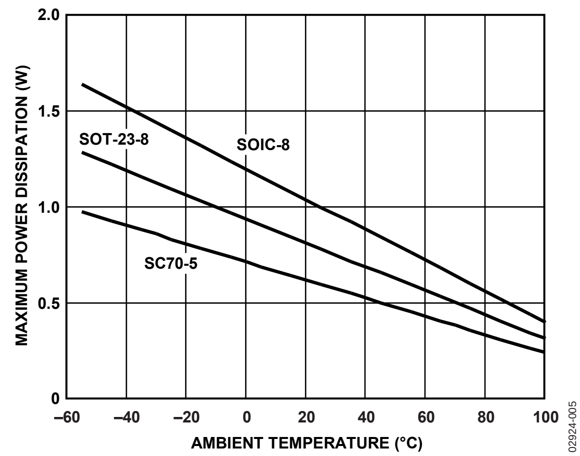


Figure 5. Maximum Power Dissipation vs. Ambient Temperature for a 4-Layer Board

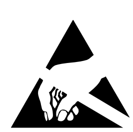
Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}. Care must be taken to minimize parasitic capacitances at the input leads of high speed op amps as discussed in the Layout, Grounding, and Bypassing Considerations section.

Figure 5 shows the maximum power dissipation in the package vs. the ambient temperature for the 8-lead SOIC (125°C/W), 5-lead SC70 (210°C/W), and 8-lead SOT-23 (160°C/W) packages on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

OUTPUT SHORT CIRCUIT

Shorting the output to ground or drawing excessive current for the AD8033/AD8034 will likely cause catastrophic failure.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

Default conditions: $V_S = \pm 5$ V, $C_L = 5$ pF, $R_L = 1$ kΩ, $T_A = 25°C$.

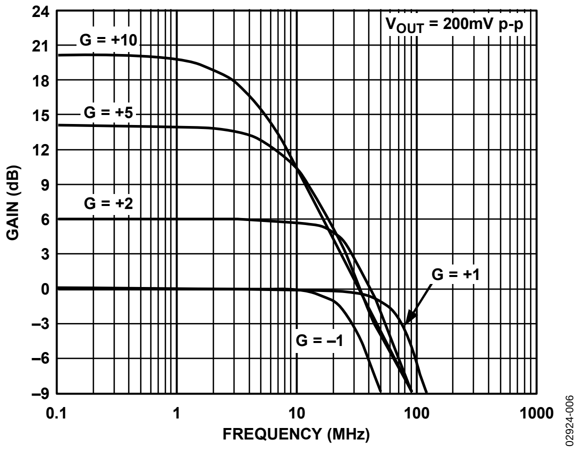


Figure 6. Small Signal Frequency Response for Various Gains

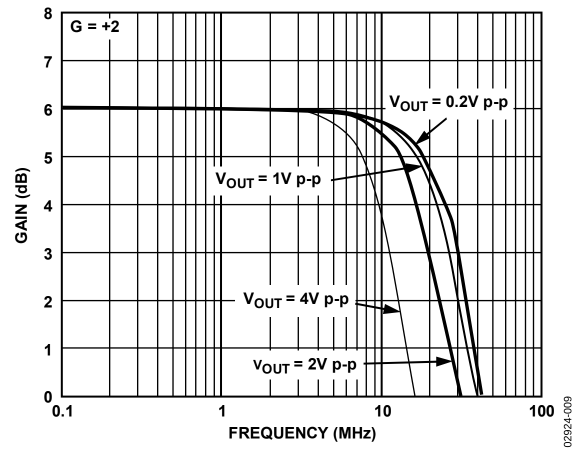


Figure 9. Frequency Response for Various Output Amplitudes (See Figure 45)

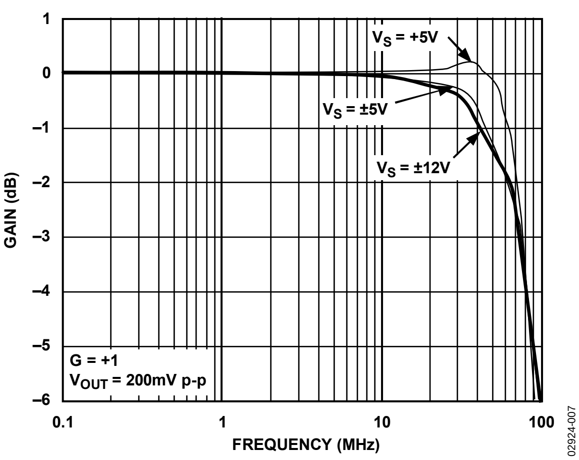


Figure 7. Small Signal Frequency Response for Various Supplies (See Figure 44)

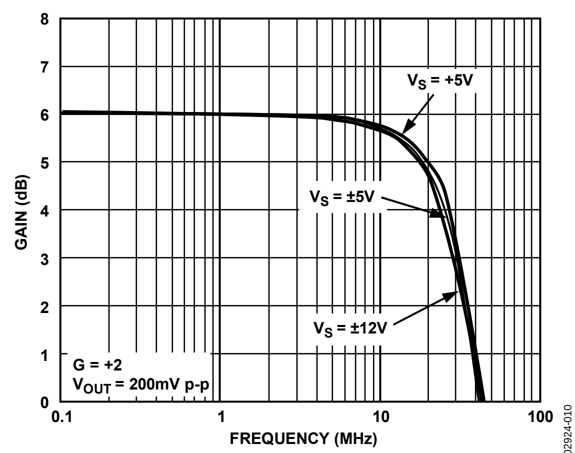


Figure 10. Small Signal Frequency Response for Various Supplies (See Figure 45)

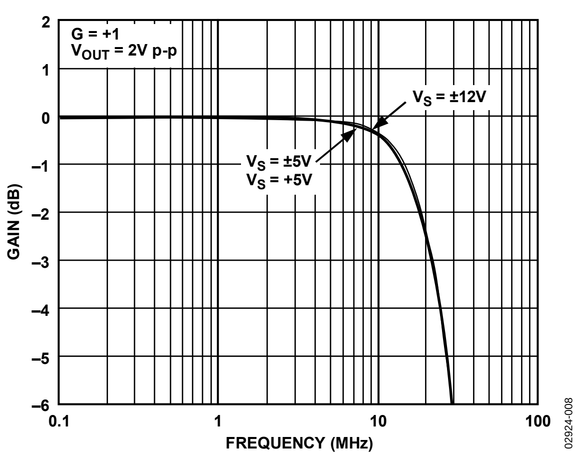


Figure 8. Large Signal Frequency Response for Various Supplies (See Figure 44)

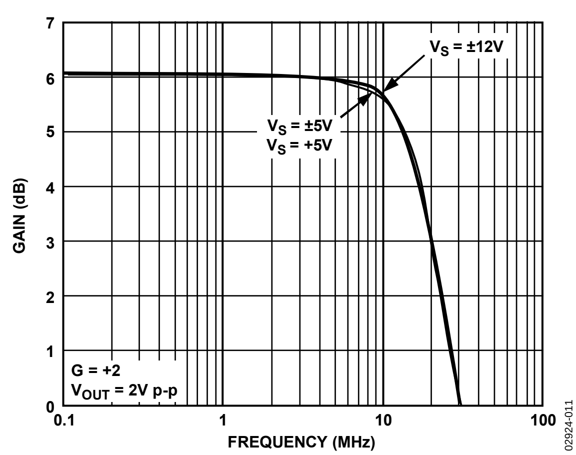


Figure 11. Large Signal Frequency Response for Various Supplies (See Figure 45)

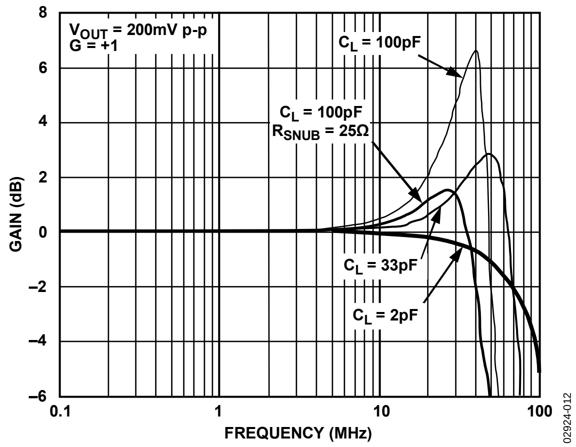


Figure 12. Small Signal Frequency Response for Various C_L (See Figure 44)

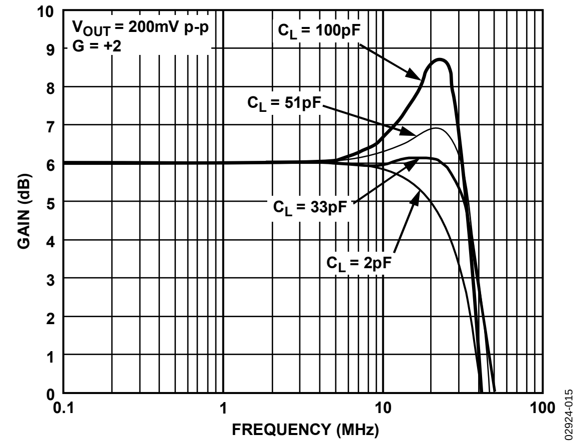


Figure 15. Small Signal Frequency Response for Various C_L (See Figure 45)

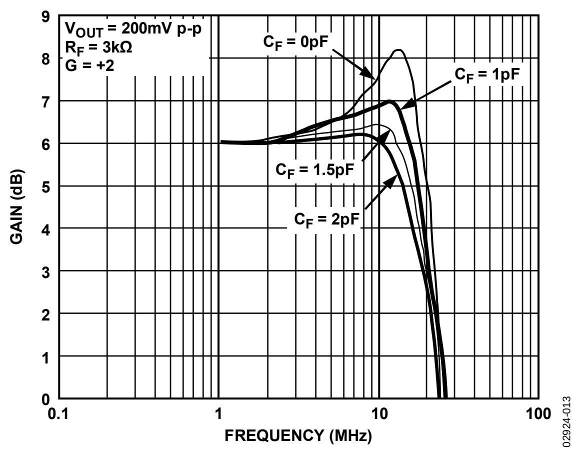


Figure 13. Small Signal Frequency Response for Various C_F (See Figure 45)

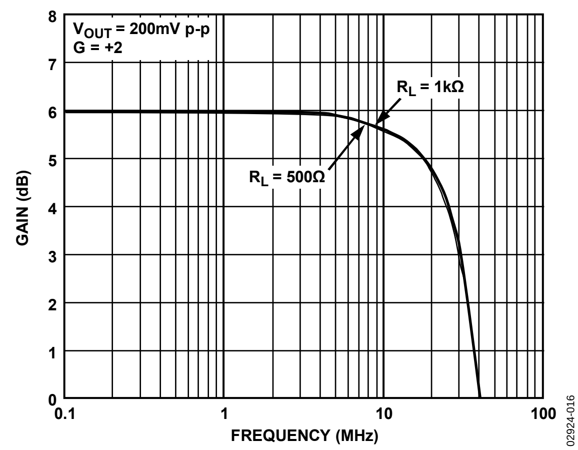


Figure 16. Small Signal Frequency Response for Various R_L (See Figure 45)

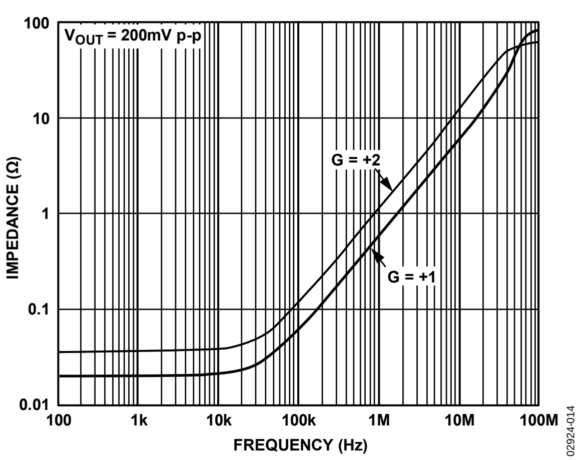


Figure 14. Output Impedance vs. Frequency (See Figure 47)

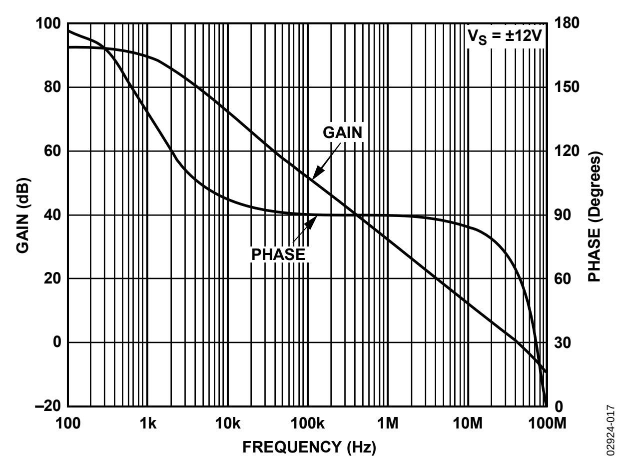


Figure 17. Open-Loop Response

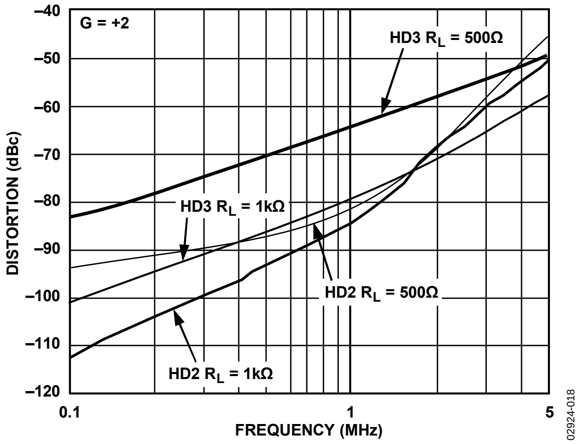


Figure 18. Harmonic Distortion vs. Frequency for Various Loads (See Figure 45)

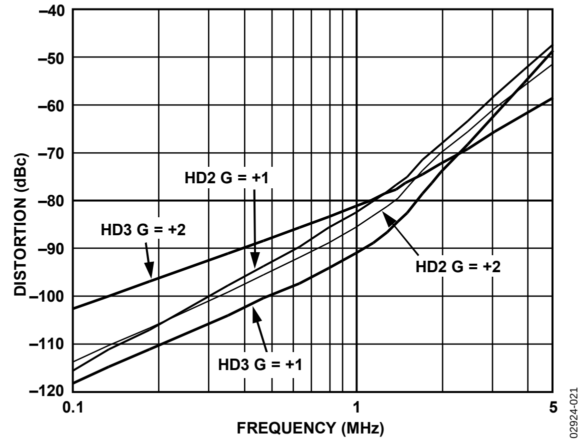


Figure 21. Harmonic Distortion vs. Frequency for Various Gains

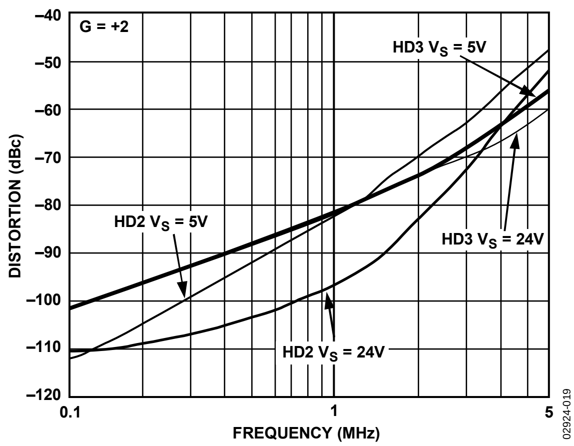


Figure 19. Harmonic Distortion vs. Frequency for Various Supply Voltages (See Figure 45)

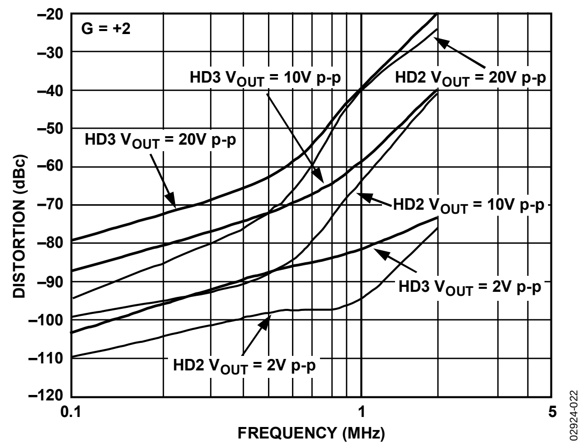


Figure 22. Harmonic Distortion vs. Frequency for Various Amplitudes (See Figure 45), V_S = 24 V

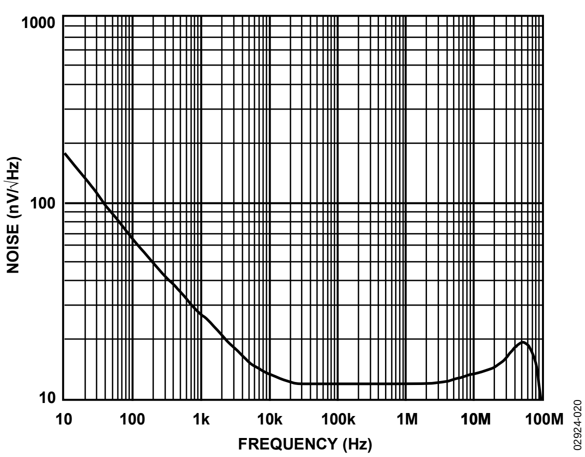


Figure 20. Voltage Noise vs. Frequency

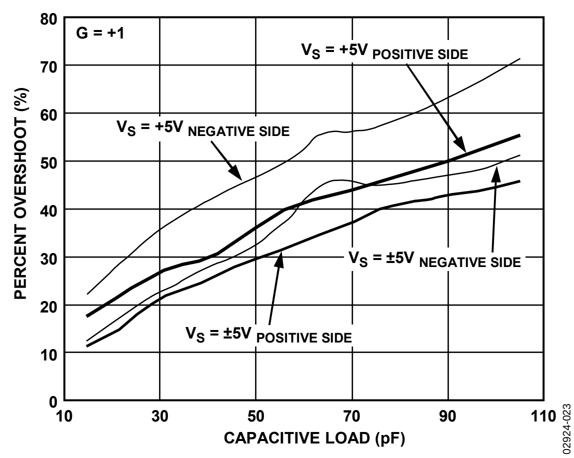


Figure 23. Percent Overshoot vs. Capacitive Load (See Figure 44)

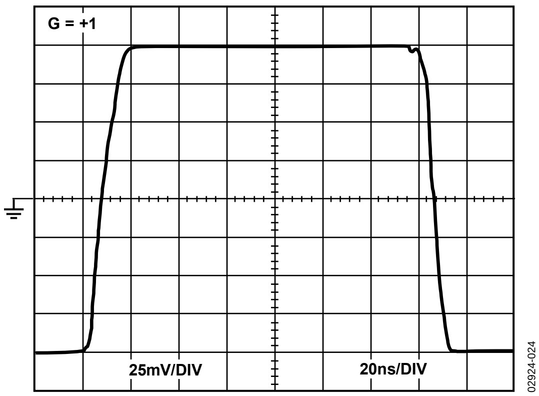


Figure 24. Small Signal Transient Response 5 V (See Figure 44)

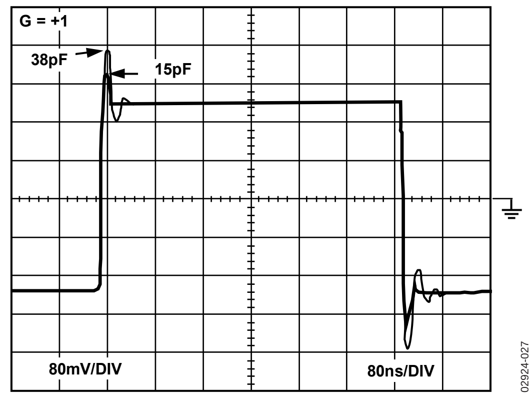


Figure 27. Small Signal Transient Response ±5 V (See Figure 44)

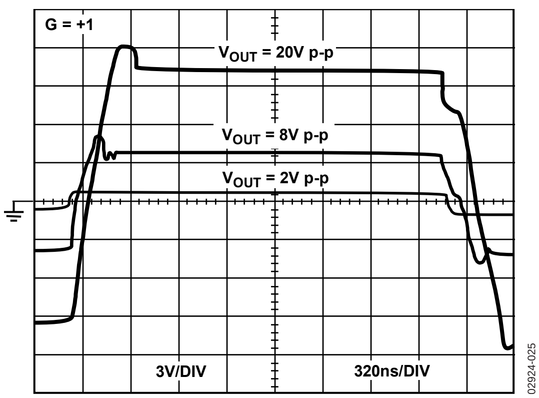


Figure 25. Large Signal Transient Response (See Figure 44)

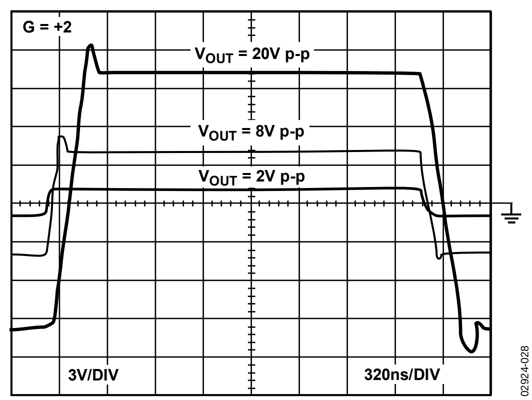


Figure 28. Large Signal Transient Response (See Figure 45)

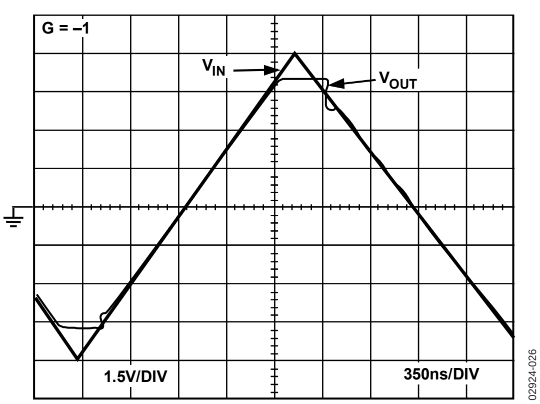


Figure 26. Output Overdrive Recovery (See Figure 46)

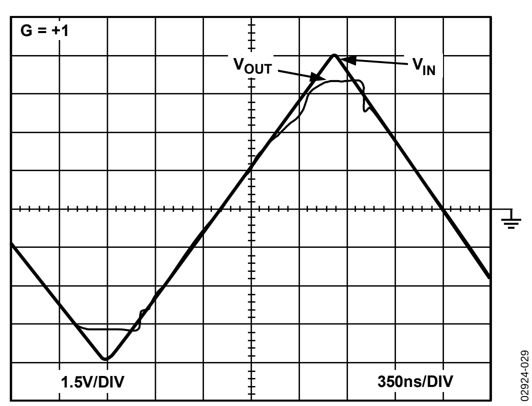


Figure 29. Input Overdrive Recovery (See Figure 44)

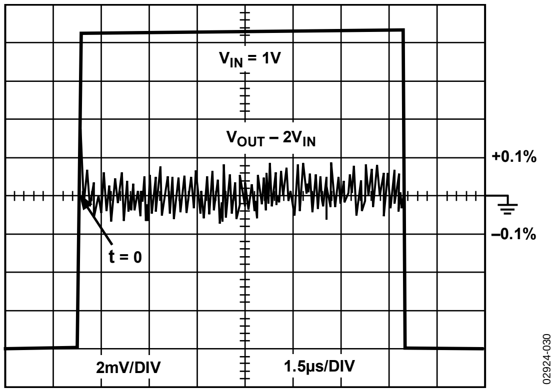


Figure 30. Long-Term Settling Time

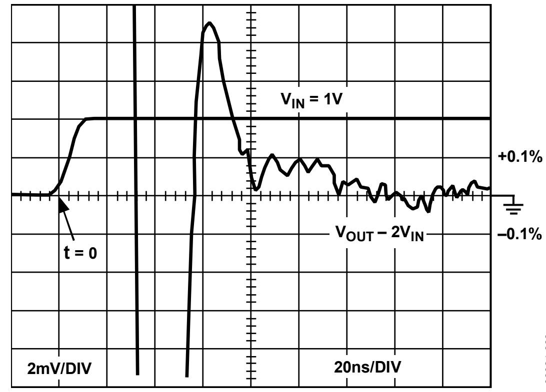


Figure 33. 0.1% Short-Term Settling Time

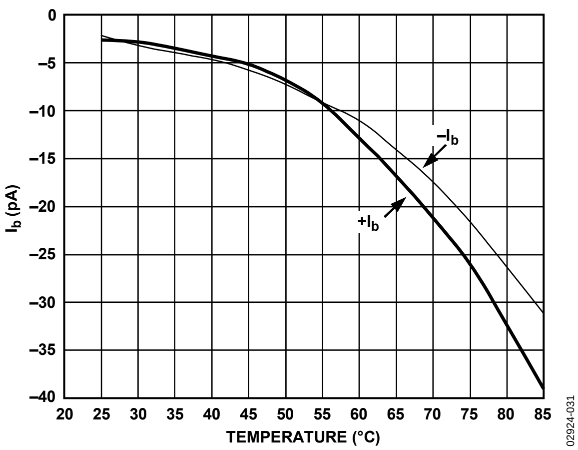


Figure 31. I_b vs. Temperature

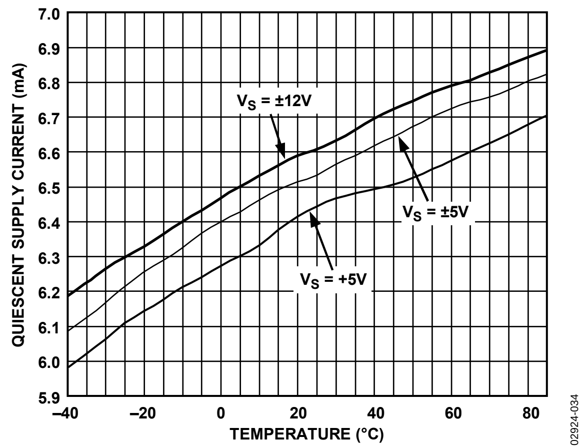


Figure 34. Quiescent Supply Current vs. Temperature for Various Supply Voltages

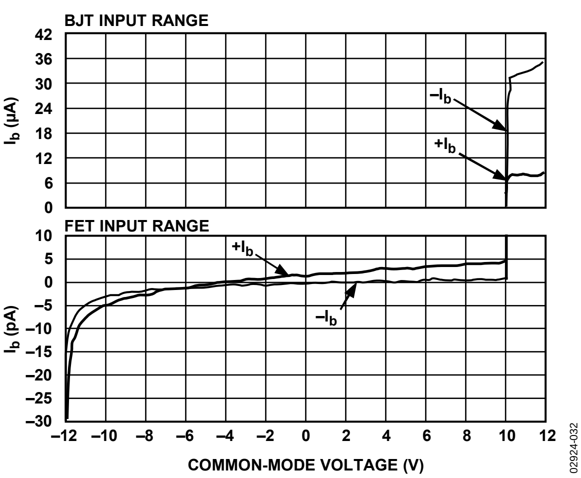


Figure 32. I_b vs. Common-Mode Voltage Range

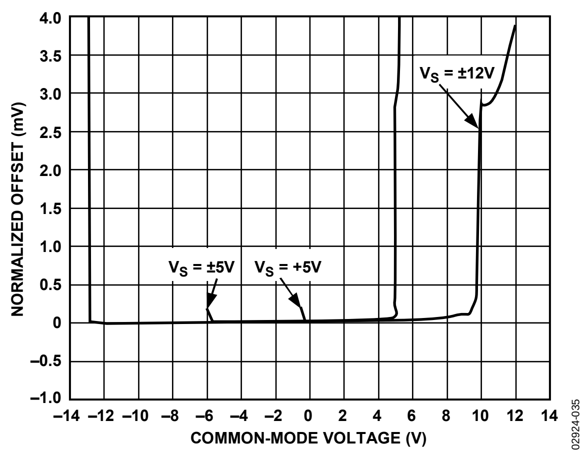


Figure 35. Input Offset Voltage vs. Common-Mode Voltage

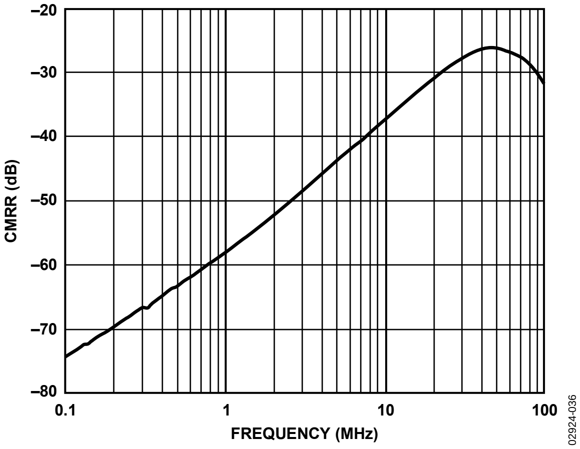


Figure 36. CMRR vs. Frequency (See Figure 50)

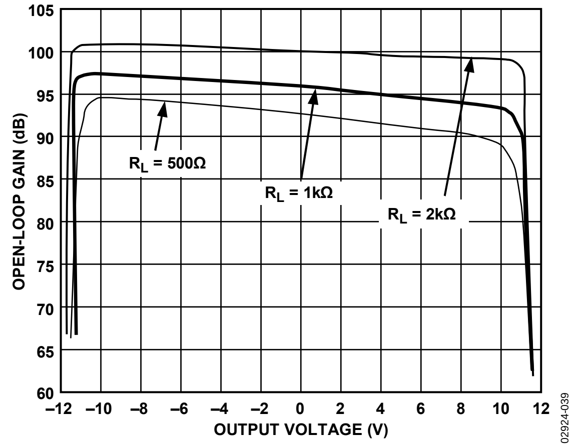


Figure 39. Open-Loop Gain vs. Output Voltage for Various R_L

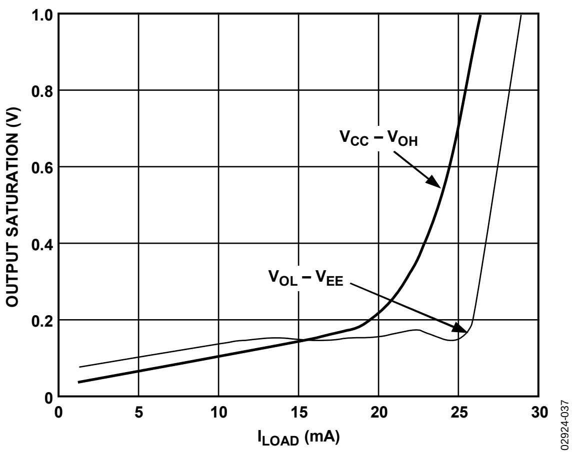


Figure 37. Output Saturation Voltage vs. Load Current

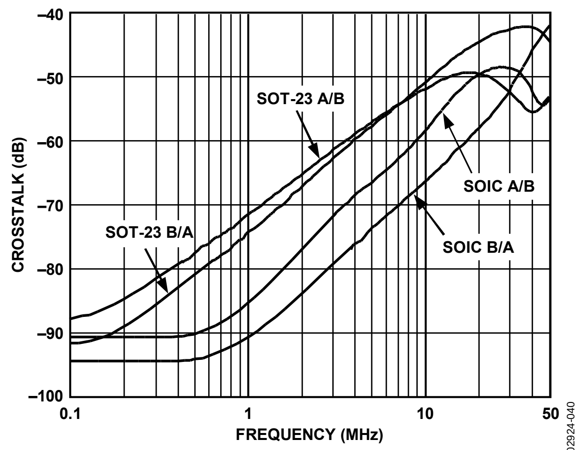


Figure 40. Crosstalk (See Figure 52)

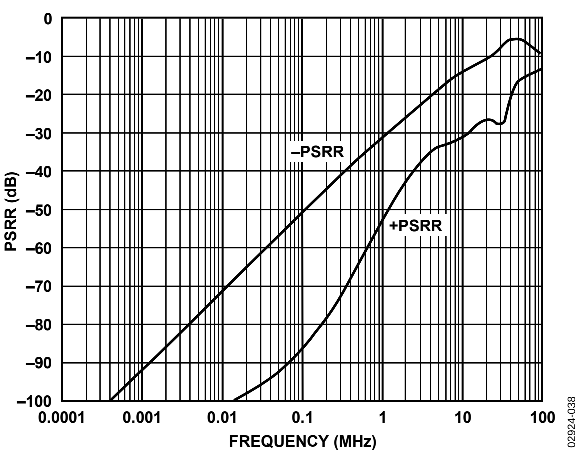


Figure 38. PSRR vs. Frequency (See Figure 49 and Figure 51)

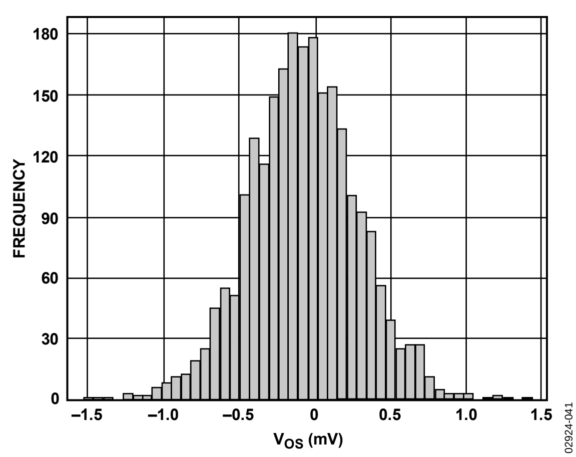


Figure 41. Initial Offset

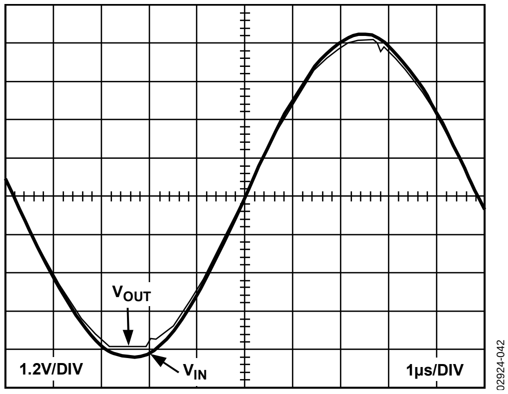


Figure 42. G = +1 Response, V_S = ±5 V

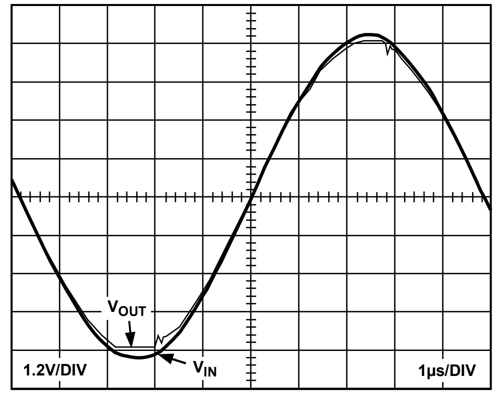


Figure 43. G = +2 Response, V_S = ±5 V

TEST CIRCUITS

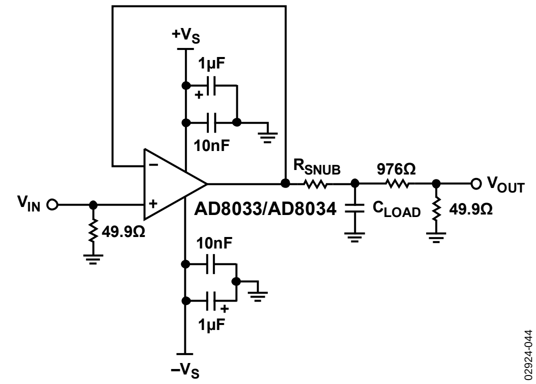


Figure 44. G = +1

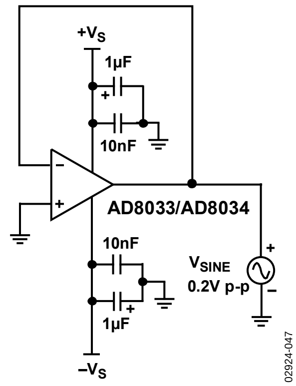


Figure 47. Output Impedance, G = +1

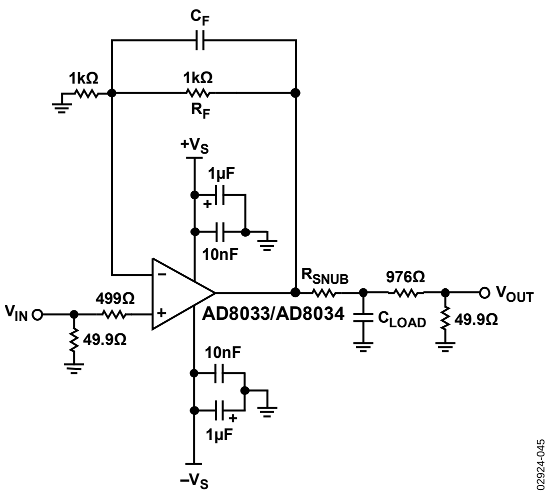


Figure 45. G = +2

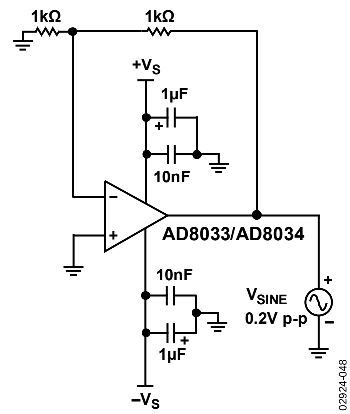


Figure 48. Output Impedance, G = +2

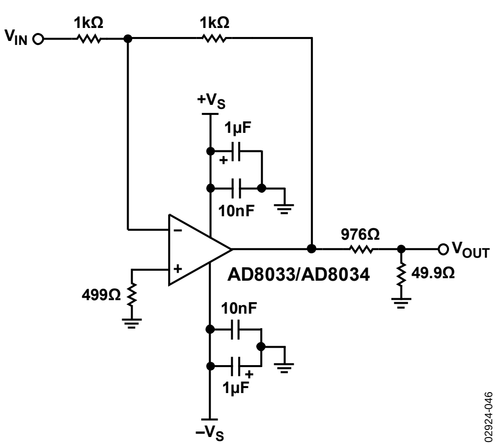


Figure 46. G = −1

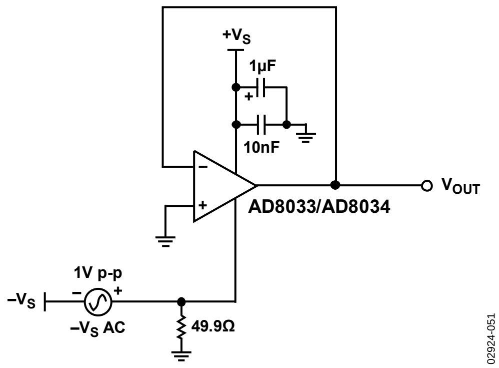


Figure 49. Negative PSRR

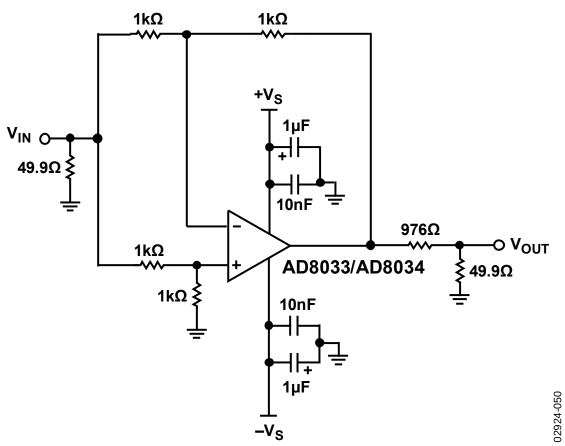


Figure 50. CMRR

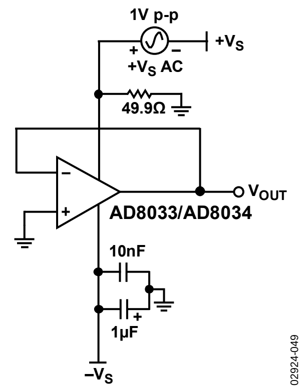


Figure 51. Positive PSRR

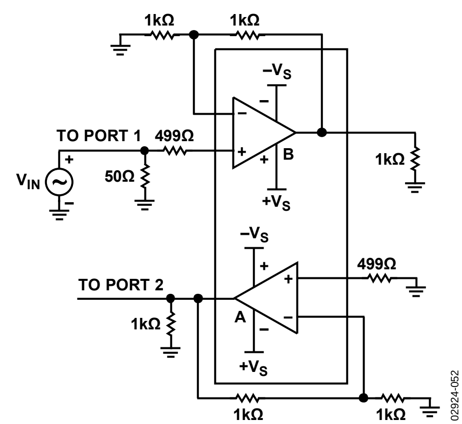


Figure 52. Crosstalk

THEORY OF OPERATION

The incorporation of JFET devices into the Analog Devices high voltage XFCB process has enabled the ability to design the AD8033/AD8034. The AD8033/AD8034 are voltage feedback rail-to-rail output amplifiers with FET inputs and a bipolar-enhanced common-mode input range. The use of JFET devices in high speed amplifiers extends the application space into both the low input bias current and low distortion, high bandwidth areas.

Using N-channel JFETs and a folded cascade input topology, the common-mode input level operates from 0.2 V below the negative rail to within 3.0 V of the positive rail. Cascading of the input stage ensures low input bias current over the entire common-mode range as well as CMRR and PSRR specifications that are above 90 dB. Additionally, long-term settling issues that normally occur with high supply voltages are minimized as a result of the cascading.

OUTPUT STAGE DRIVE AND CAPACITIVE LOAD DRIVE

The common emitter output stage adds rail-to-rail output performance and is compensated to drive 35 pF (30% overshoot at G = +1). Additional capacitance can be driven if a small snub resistor is put in series with the capacitive load, effectively decoupling the load from the output stage, as shown in Figure 12. The output stage can source and sink 20 mA of current within 500 mV of the supply rails and 1 mA within 100 mV of the supply rails.

INPUT OVERDRIVE

An additional feature of the AD8033/AD8034 is a bipolar input pair that adds rail-to-rail common-mode input performance specifically for applications that cannot tolerate phase inversion problems.

Under normal common-mode operation, the bipolar input pair is kept reversed, maintaining I_b at less than 1 pA. When the input common-mode operation comes within 3.0 V of the positive supply rail, I1 turns off and I4 turns on, supplying tail current to the bipolar pair Q25 and Q27. With this configuration, the inputs can be driven beyond the positive supply rail without any phase inversion (see Figure 53).

As a result of entering the bipolar mode of operation, an offset and input bias current shift occurs (see Figure 32 and Figure 35). After re-entering the JFET common-mode range, the amplifier recovers in approximately 100 ns (refer to Figure 29 for input overload behavior). Above and below the supply rails, ESD protection diodes activate, resulting in an exponentially increasing input bias current. If the inputs are driven well beyond the rails, series input resistance should be included to limit the input bias current to <10 mA.

INPUT IMPEDANCE

The input capacitance of the AD8033/AD8034 forms a pole with the feedback network, resulting in peaking and ringing in the overall response. The equivalent impedance of the feedback network should be kept small enough to ensure that the parasitic pole falls well beyond the −3 dB bandwidth of the gain configuration being used. If larger impedance values are desired, the amplifier can be compensated by placing a small capacitor in parallel with the feedback resistor. Figure 13 shows the improvement in frequency response by including a small feedback capacitor with high feedback resistance values.

THERMAL CONSIDERATIONS

Because the AD8034 operates at up to ±12 V supplies in the small 8-lead SOT-23 package (160°C/W), power dissipation can easily exceed package limitations, resulting in permanent shifts in device characteristics and even failure. Likewise, high supply voltages can cause an increase in junction temperature even with light loads, resulting in an input bias current and offset drift penalty. The input bias current doubles for every 10°C shown in Figure 31. Refer to the Maximum Power Dissipation section for an estimation of die temperature based on load and supply voltage.

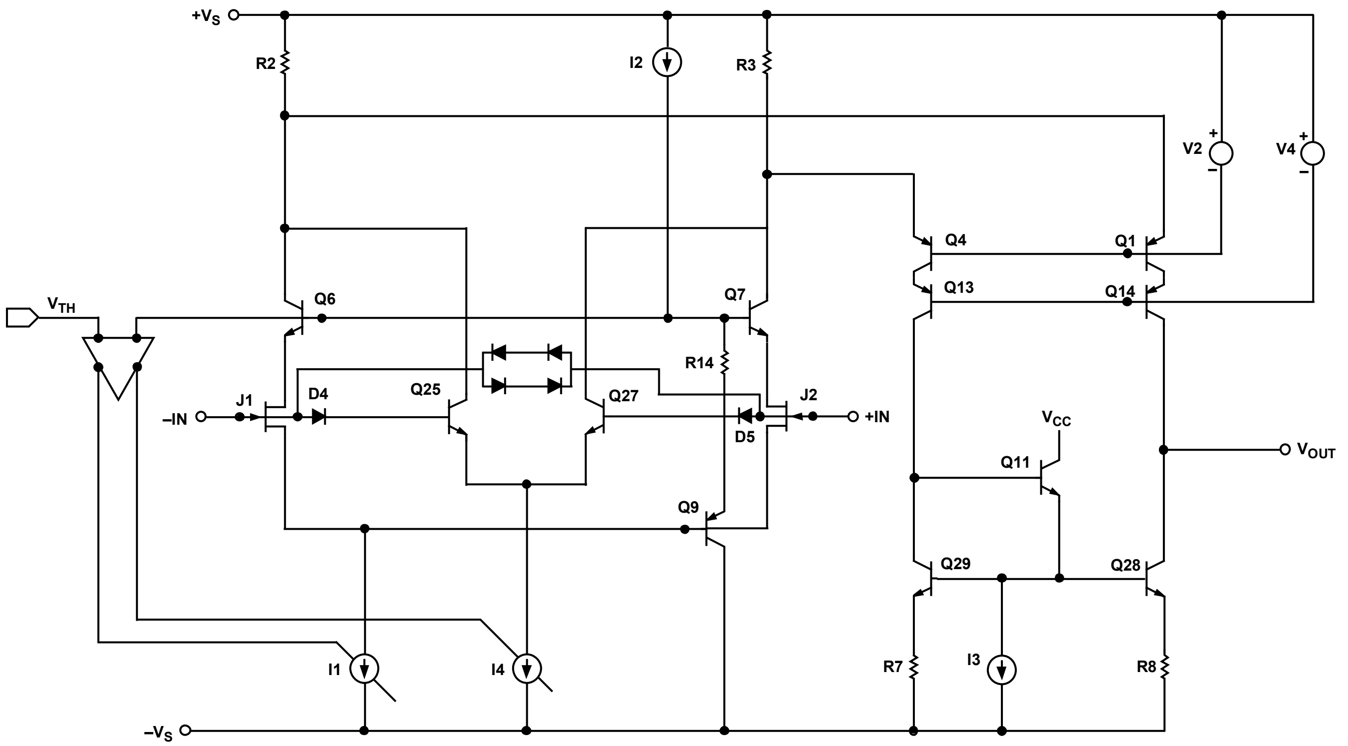


Figure 53. Simplified AD8033/AD8034 Input Stage

LAYOUT, GROUNDING, AND BYPASSING CONSIDERATIONS

BYPASSING

Power supply pins are actually inputs, and care must be taken so that a noise-free stable dc voltage is applied. The purpose of bypass capacitors is to create low impedances from the supply to ground at all frequencies, thereby shunting or filtering a majority of the noise. Decoupling schemes are designed to minimize the bypassing impedance at all frequencies with a parallel combination of capacitors. The chip capacitors, 0.01 μF or 0.001 μF (X7R or NPO), are critical and should be placed as close as possible to the amplifier package. Larger chip capacitors, such as the 0.1 μF capacitor, can be shared among a few closely spaced active components in the same signal path. The 10 μF tantalum capacitor is less critical for high frequency bypassing, and in most cases, only one per board is needed at the supply inputs.

GROUNDING

A ground plane layer is important in densely packed PCBs to spread the current, thereby minimizing parasitic inductances. However, an understanding of where the current flows in a circuit is critical to implementing effective high speed circuit design. The length of the current path is directly proportional to the magnitude of the parasitic inductances and, thus, the high frequency impedance of the path. High speed currents in an inductive ground return create unwanted voltage noise. The length of the high frequency bypass capacitor leads is most critical. A parasitic inductance in the bypass grounding works against the low impedance created by the bypass capacitor. Place the ground leads of the bypass capacitors at the same physical location.

Because load currents flow from the supplies as well, the ground for the load impedance should be at the same physical location as the bypass capacitor grounds. For the larger value capacitors that are intended to be effective at lower frequencies, the current return path distance is less critical.

LEAKAGE CURRENTS

Poor PCB layout, contaminants, and the board insulator material can create leakage currents that are much larger than the input bias currents of the AD8033/AD8034. Any voltage differential between the inputs and nearby runs set up leakage currents through the PCB insulator, for example, 1 V/100 GΩ = 10 pA. Similarly, any contaminants on the board can create significant leakage (skin oils are a common problem). To significantly reduce leakages, put a guard ring (shield) around the inputs and input leads that is driven to the same voltage potential as the inputs. This way there is no voltage potential between the inputs and surrounding area to set up any leakage currents. For the guard ring to be completely effective, it must be driven by a relatively low impedance source and should completely surround the input leads on all sides, above, and below using a multilayer board.

Another effect that can cause leakage currents is the charge absorption of the insulator material itself. Minimizing the amount of material between the input leads and the guard ring helps to reduce the absorption. In addition, low absorption materials such as Teflon® or ceramic may be necessary in some instances.

INPUT CAPACITANCE

Along with bypassing and ground, high speed amplifiers can be sensitive to parasitic capacitance between the inputs and ground. A few pF of capacitance reduces the input impedance at high frequencies, in turn it increases the gain of the amplifier and can cause peaking of the overall frequency response or even oscillations if severe enough. It is recommended that the external passive components that are connected to the input pins be placed as close as possible to the inputs to avoid parasitic capacitance. The ground and power planes must be kept at a distance of at least 0.05 mm from the input pins on all layers of the board.

APPLICATIONS INFORMATION

HIGH SPEED PEAK DETECTOR

The low input bias current and high bandwidth of the AD8033/AD8034 make the parts ideal for a fast settling, low leakage peak detector. The classic fast-low leakage topology with a diode in the output is limited to ~1.4 V p-p maximum in the case of the AD8033/AD8034 because of the protection diodes across the inputs, as shown in Figure 54.

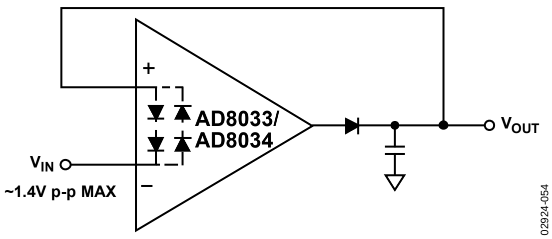


Figure 54. High Speed Peak Detector with Limited Input Range

Using the AD8033/AD8034, a unity gain peak detector can be constructed that captures a 300 ns pulse while still taking advantage of the low input bias current and wide common-mode input range of the AD8033/AD8034, as shown in Figure 55.

Using two amplifiers, the difference between the peak and the current input level is forced across R2 instead of either amplifier's input pins. In the event of a rising pulse, the first amplifier compensates for the drop across D2 and D3, forcing the voltage at Node 3 equal to Node 1. D1 is off and the voltage drop across R2 is zero. Capacitor C3 speeds up the loop by providing the charge required by the input capacitance of the first amplifier, helping to maintain a minimal voltage drop across R2 in the sampling mode. A negative going edge results in D2 and D3 turning off and D1 turning on, closing the loop around the first amplifier and forcing $V_{OUT} - V_{IN}$ across R2. R4 makes the voltage across D2 zero, minimizing leakage current and kickback from D3 from affecting the voltage across C2.

The rate of the incoming edge must be limited so that the output of the first amplifier does not overshoot the peak value of V_{IN} before the output of the second amplifier can provide negative feedback at the summing junction of the first amplifier. This is accomplished with the combination of R1 and C1, which allows the voltage at Node 1 to settle to 0.1% of V_{IN} in 270 ns. The selection of C2 and R3 is made by considering droop rate, settling time, and kickback. R3 prevents overshoot from occurring at Node 3. The time constants of R1, C1 and R3, C2 are roughly equal to achieve the best performance. Slower time constants can be selected by increasing C2 to minimize droop rate and kickback at the cost of increased settling time. R1 and C1 should also be increased to match, reducing the incoming pulse's effect on kickback.

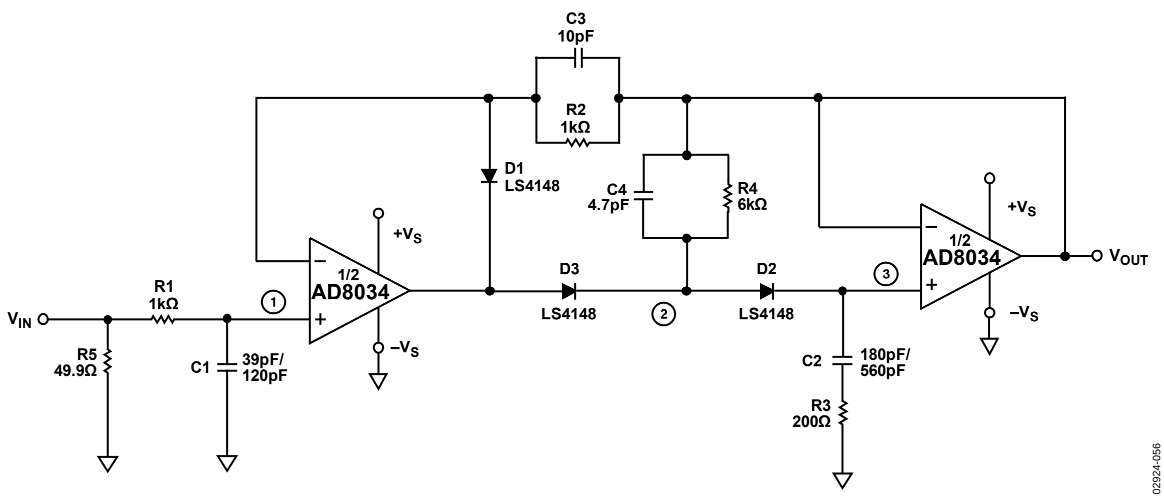


Figure 55. High Speed, Unity Gain Peak Detector Using AD8034

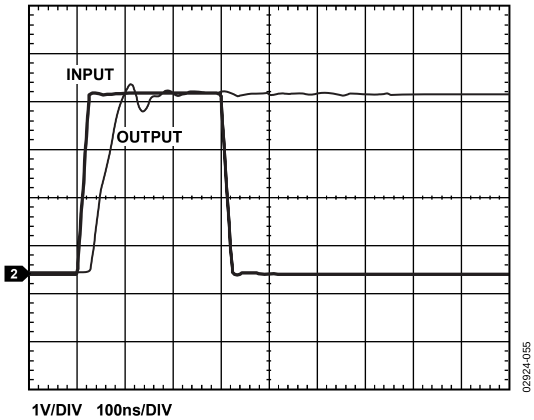


Figure 56. Peak Detector Response 4 V, 300 ns Pulse

Figure 56 shows the peak detector in Figure 55 capturing a 300 ns, 4 V pulse with 10 mV of kickback and a droop rate of 5 V/s. For larger peak-to-peak pulses, increase the time constants of R1, C1 and R3, C3 to reduce overshoot. The best droop rate occurs by isolating parasitic resistances from Node 3, which can be accomplished using a guard band connected to the output of the second amplifier that surrounds its summing junction (Node 3).

Increasing both time constants by a factor of 3 permits a larger peak pulse to be captured and increases the output accuracy.

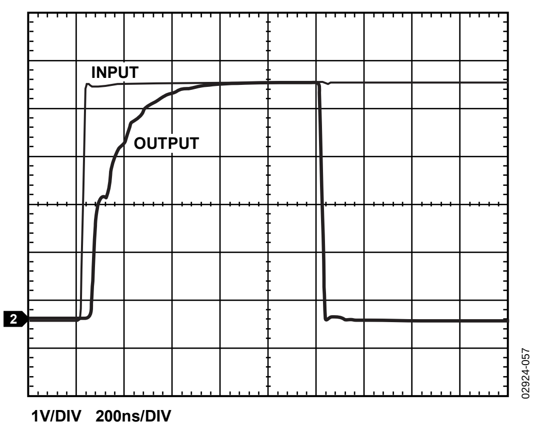


Figure 57. Peak Detector Response 5 V, 1 μs Pulse

Figure 57 shows a 5 V peak pulse being captured in 1 μs with less than 1 mV of kickback. With this selection of time constants, up to a 20 V peak pulse can be captured with no overshoot.

ACTIVE FILTERS

The response of an active filter varies greatly depending on the performance of the active device. Open-loop bandwidth and gain, along with the order of the filter, determines the stop-band attenuation as well as the maximum cutoff frequency, while input capacitance can set a limit on which passive components are used. Topologies for active filters are varied, and some are more dependent on the performance of the active device than others are.

The Sallen-Key topology is the least dependent on the active device, requiring that the bandwidth be flat to beyond the stop-band frequency because it is used simply as a gain block. In the case of high Q filter stages, the peaking must not exceed the open-loop bandwidth and the linear input range of the amplifier.

Using an AD8033/AD8034, a 4-pole cascaded Sallen-Key filter can be constructed with $f_C = 1$ MHz and over 80 dB of stop-band attenuation, as shown in Figure 58.

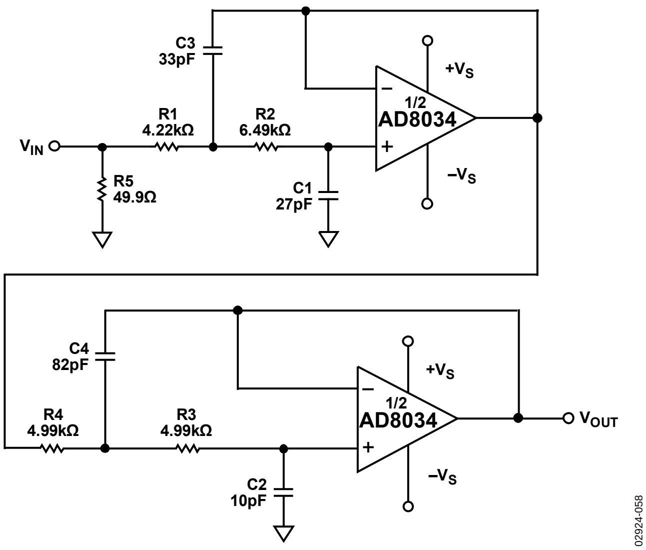


Figure 58. 4-Pole Cascade Sallen-Key Filter

Component values are selected using a normalized cascaded, 2-stage Butterworth filter table and Sallen-Key 2-pole active filter equations. The overall frequency response is shown in Figure 59.

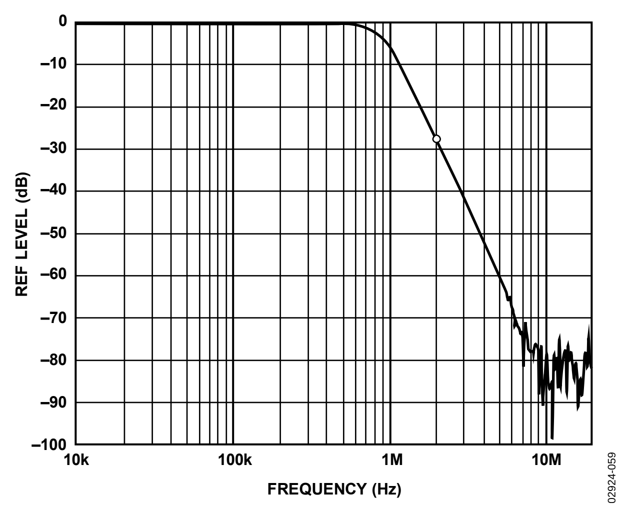


Figure 59. 4-Pole Cascade Sallen-Key Filter Response

When selecting components, the common-mode input capacitance must be taken into consideration.

Filter cutoff frequencies can be increased beyond 1 MHz using the AD8033/AD8034 but limited open-loop gain and input impedance begin to interfere with the higher Q stages. This can cause early roll-off of the overall response.

Additionally, the stop-band attenuation decreases with decreasing open-loop gain.

Keeping these limitations in mind, a 2-pole Sallen-Key Butterworth filter with f_C = 4 MHz can be constructed that has a relatively low Q of 0.707 while still maintaining 15 dB of attenuation an octave above f_C and 35 dB of stop-band attenuation. The filter and response are shown in Figure 60 and Figure 61, respectively.

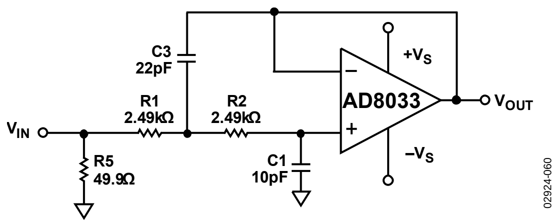


Figure 60. 2-Pole Butterworth Active Filter

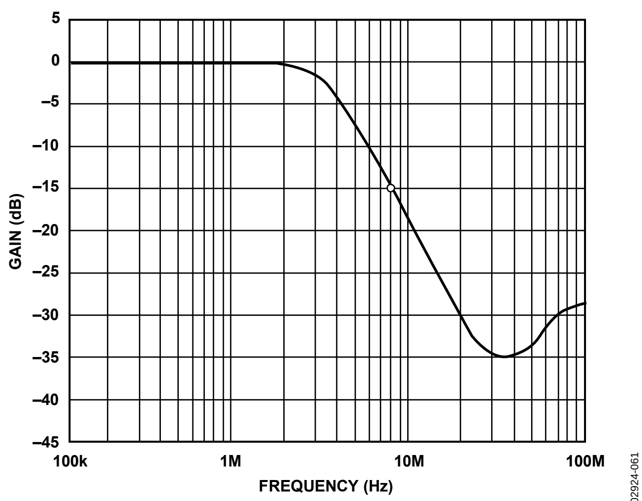


Figure 61. 2-Pole Butterworth Active Filter Response

WIDEBAND PHOTODIODE PREAMP

Figure 62 shows an I/V converter with an electrical model of a photodiode.

The basic transfer function is

$$V_{OUT} = \frac{I_{PHOTO} \times R_F}{1 + sC_F R_F}$$

where I_{PHOTO} is the output current of the photodiode, and the parallel combination of R_F and C_F sets the signal bandwidth.

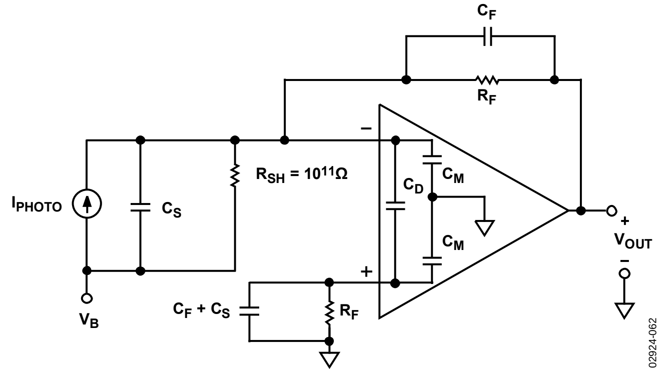


Figure 62. Wideband Photodiode Preamp

The stable bandwidth attainable with this preamp is a function of R_F, the gain bandwidth product of the amplifier, and the total capacitance at the summing junction of the amplifier, including C_S and the amplifier input capacitance. R_F and the total capacitance produce a pole in the loop transmission of the amplifier that can result in peaking and instability. Adding C_F creates a zero in the loop transmission that compensates for the effect of the pole and reduces the signal bandwidth. It can be shown that the signal bandwidth resulting in a 45°phase margin ($f_{(45)}$) is defined by the expression

$$f_{(45)} = \sqrt{\frac{f_{CR}}{2\pi \times R_F \times C_S}}$$

where:
f_{CR} is the amplifier crossover frequency.
R_F is the feedback resistor.
C_S is the total capacitance at the amplifier summing junction (amplifier + photodiode + board parasitics).

The value of C_F that produces $f_{(45)}$ is

$$C_F = \sqrt{\frac{C_S}{2\pi \times R_F \times f_{CR}}}$$

The frequency response in this case shows about 2 dB of peaking and 15% overshoot. Doubling C_F and cutting the bandwidth in half results in a flat frequency response, with about 5% transient overshoot.

The output noise over frequency of the preamp is shown in Figure 63.

The pole in the loop transmission translates to a zero in the noise gain of the amplifier, leading to an amplification of the input voltage noise over frequency. The loop transmission zero introduced by C_F limits the amplification. The bandwidth of the noise gain extends past the preamp signal bandwidth and is eventually rolled off by the decreasing loop gain of the amplifier.

Keeping the input terminal impedances matched is recommended to eliminate common-mode noise peaking effects that add to the output noise.

Integrating the square of the output voltage noise spectral density over frequency and then taking the square root results in the total rms output noise of the preamp.

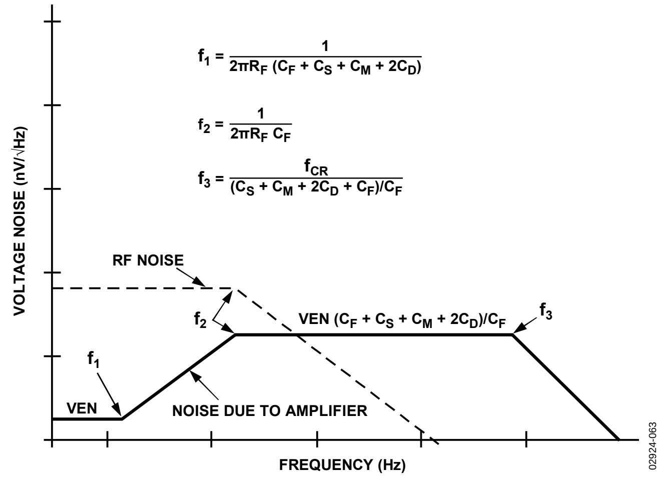


Figure 63. Photodiode Voltage Noise Contributions

OUTLINE DIMENSIONS

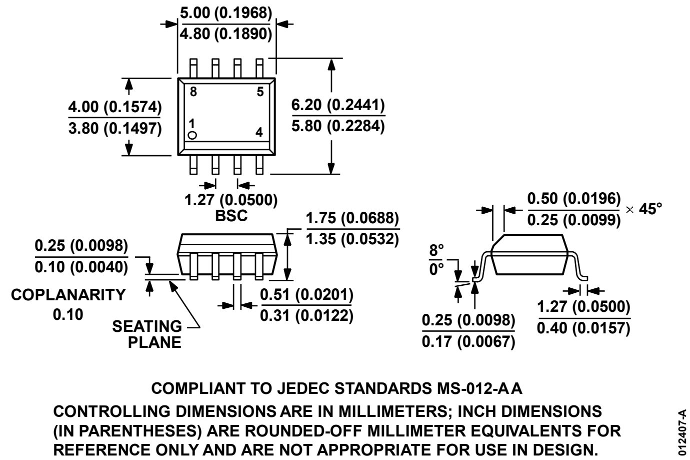


Figure 64. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

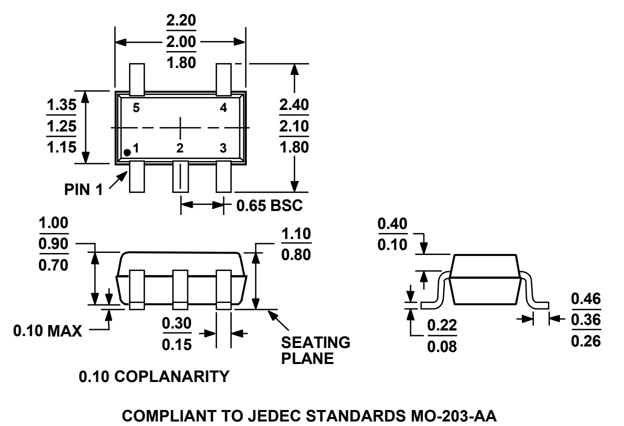


Figure 65. 5-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-5)
Dimensions shown in millimeters

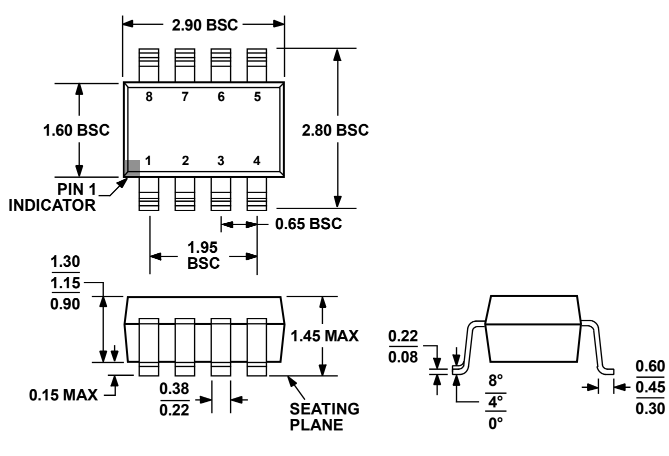


Figure 66. 8-Lead Small Outline Transistor Package [SOT-23]
(RJ-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8033AR	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8033AR-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8033AR-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8033ARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8033ARZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8033ARZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8033AKS-R2	−40°C to +85°C	5-Lead SC70	KS-5	H3B
AD8033AKS-REEL	−40°C to +85°C	5-Lead SC70	KS-5	H3B
AD8033AKS-REEL7	−40°C to +85°C	5-Lead SC70	KS-5	H3B
AD8033AKSZ-R2[1]	−40°C to +85°C	5-Lead SC70	KS-5	H3C
AD8033AKSZ-REEL[1]	−40°C to +85°C	5-Lead SC70	KS-5	H3C
AD8033AKSZ-REEL7[1]	−40°C to +85°C	5-Lead SC70	KS-5	H3C
AD8034AR	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8034AR-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8034AR-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8034ARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8034ARZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8034ARZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8034ART-R2	−40°C to +85°C	8-Lead SOT-23	RJ-8	HZA
AD8034ART-REEL	−40°C to +85°C	8-Lead SOT-23	RJ-8	HZA
AD8034ART-REEL7	−40°C to +85°C	8-Lead SOT-23	RJ-8	HZA
AD8034ARTZ-R2[1]	−40°C to +85°C	8-Lead SOT-23	RJ-8	HZA#
AD8034ARTZ-REEL[1]	−40°C to +85°C	8-Lead SOT-23	RJ-8	HZA#
AD8034ARTZ-REEL7[1]	−40°C to +85°C	8-Lead SOT-23	RJ-8	HZA#
AD8034CHIPS		DIE		

[1] Z = RoHS Compliant Part, # denotes RoHS compliant product may be top or bottom marked.

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