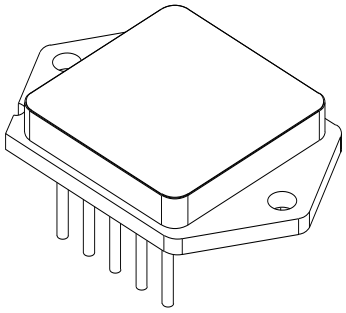
MIL-PRF-38534 AND 38535 CERTIFIED FACILITY

100 VOLT 20 AMP H-BRIDGE PWM MOTOR DRIVER/AMPLIFIER

4206

FEATURES:

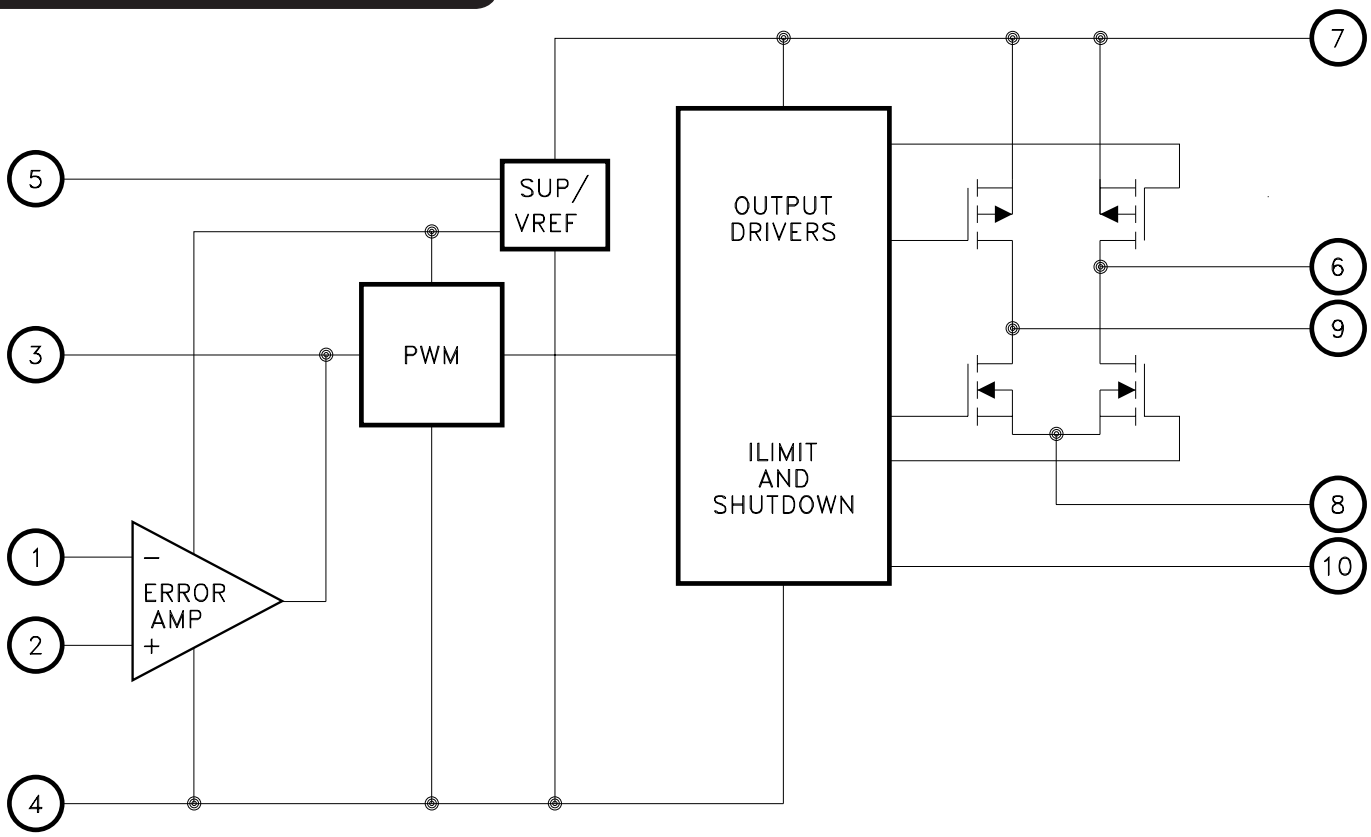
- Replaces APEX SA01 PWM Amplifier
- 100 Volt, 20 Amp Capability
- Self-Contained Smart Lowside/Highside Drive Circuitry
- Internal PWM Generation, Shoot-through Protection
- Isolated Case Allows Direct Heatsinking
- Available Fully Screened To MIL-PRF-38534 Class H
- Contact MSK for MIL-PRF-38534 Qualification Status



DESCRIPTION:

The MSK4206 is a complete H-Bridge microcircuit intended for use in DC brushed motor control applications or Class D switchmode amplification in severe operating conditions. All of the control circuitry, including an error amplifier, is internal to the device. A precision reference output is provided for use in offsetting the error amplifier. Fixed highside current limit is provided internally. Lowside current limit is user controlled with the use of an external resistor network. The design is packaged in a 10 pin bolt down power package.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS

- MOTOR CONTROL
- REACTIVE LOADS
- PIEZO ELEMENTS

PIN-OUT INFORMATION

1	- IN	6	A OUT
2	+IN	7	+VS
3	EA OUT	8	ISENSE
4	GND	9	B OUT
5	REF	10	SHDN/FILTER

8548-139 Rev. D 05/17

ABSOLUTE MAXIMUM RATINGS ⑧

+VS High Voltage Supply.....100V
IOUT Continuous Output Current.....20A
IPK Peak Output Current.....30A
VOUT Output Voltage Range.....GND TO +VS
VIN Input Voltage, +IN and -IN .....0V TO 12V
VL Logic Input Voltage (SHDN/FILTER).....0V TO 10V

TST Storage Temperature Range⑨.....-65°C to +150°C
TLD Lead Temperature Range
(10 Seconds).....300°C
TC Case Operating Temperature Range
MSK4206H.....-55°C to +125°C
MSK4206.....-40°C to +85°C
TJ Junction Temperature.....+150°C
θJc Thermal Resistance
(Output FETS @ 125°C).....1.25°C/W
(Output FETS @ 25°C).....1.0°C/W

ELECTRICAL SPECIFICATIONS

Parameter	Test Conditions	Group A Subgroup	MSK4206H Min.	MSK4206H Typ.	MSK4206H Max.	MSK4206 Min.	MSK4206 Typ.	MSK4206 Max.	Units
OUTPUT CHARACTERISTICS									
VDS(ON) Highside ⑥	ID = 10A	1	-	1.60	2.0	-	1.60	2.2	V
		2	-	2.4	3.0	-	-	-	V
		3	-	1.1	1.5	-	-	-	V
VDS(ON) Lowside ⑥	ID = 10A	1	-	0.75	1.0	-	0.75	1.2	V
		2	-	1.1	1.5	-	-	-	V
		3	-	0.45	0.70	-	-	-	V
VDS(ON) Highside ② ⑥	ID = 20A	1	-	3.5	-	-	3.5	-	V
	ID = 15A	2	-	3.7	-	-	-	-	V
	ID = 20A	3	-	2.1	-	-	-	-	V
VDS(ON) Lowside ② ⑥	ID = 20A	1	-	1.5	-	-	1.5	-	V
		2	-	2.4	-	-	-	-	V
		3	-	0.90	-	-	-	-	V
RDS(ON) each MOSFET ② ⑥ ⑦ ID = 10A	P-CHANNEL	1	-	110	125	-	110	125	mΩ
		2	-	168	250	-	-	-	mΩ
	N-CHANNEL	1	-	22	52	-	22	52	mΩ
		2	-	78	95	-	-	-	mΩ
Leakage Current Highside	+VS = 80V	1	-	0.02	25	-	0.02	25	µA
		2	-	1.0	250	-	-	-	µA
Leakage Current Lowside	A/B out = 80V	1	-	0.02	25	-	0.02	25	µA
		2	-	1.0	250	-	-	-	µA
OUTPUT FREQUENCY and DUTY CYCLE									
Switching Frequency		4	35	42	49	32	42	52	KHz
Duty Cycle	EA OUT = 5V	4	40	50	60	40	50	60	%
	EA OUT = 8V, Output A = 100%, Output B = 0%	7	-	Verify	-	-	Verify	-	P/F
	EA OUT = 2V, Output A = 0%, Output B = 100%	7	-	Verify	-	-	Verify	-	P/F
SUPPLY CURRENT CHARACTERISTICS									
+VS ②		1, 2, 3	16	50	100	16	50	100	V
+VS Current	IREF = 5mA, RL = 10KΩ SHDN/FILTER = <180mV	1	-	60	93	-	60	93	mA
+VS Current	IREF = 5mA, RL = 10KΩ SHDN/FILTER = <180mV	1	-	20	25	-	-	25	mA
REFERENCE									
Output Voltage	IOUT = 5mA	1	7.46	7.50	7.54	7.42	7.50	7.58	V
		2, 3	7.42	-	7.58	-	-	-	V
Load Regulation		-	-	20	-	-	20	-	PPM/mA
Line Regulation		-	-	1	-	-	1	-	PPM/V
Error Amp									
Offset Voltage		1	-10	-	+10	-15	-	+15	mV
		2, 3	-15	-	+15	-	-	-	mV
Input Bias Current		1	-	0.5	5	-	0.5	8	µA
		2, 3	-	0.7	13	-	-	-	µA
Offset Current		1	-	0.01	1	-	0.01	2	µA
		2, 3	-	0.01	8	-	-	-	µA
Common Mode Voltage range ②		1, 2, 3	2	-	8	2	0.01	8	V
Common Mode Rejection, DC ②		1, 2, 3	75	-	-	75		-	dB
Slew Rate		-	-	15	-	-	15	-	V/µS
Open loop gain ②		4, 5, 6	75	-	-	75	-	-	dB
Gain Bandwidth Product		-	-	2	-	-		-	MHz
SHDN/FILTER									
Trip Point		1	180	200	220	170	200	230	mV
Input Current		1	-	0.8	10	-	0.8	10	µA

NOTES:

① +VS = 28V, I SENSE = Ground, SHDN/FILTER = 0V unless otherwise specified.
② Guaranteed by design but not tested. Typical parameters are representative of actual device performance but are for reference only.
③ Class H devices are 100% tested to subgroups 1, 2, 3, 4 and 7. Subgroup 5 and 6 testing available upon request.
④ Subgroup 1, 4, 7 TA = +25°C
2, 5 TA = +125°C
3, 6 TA = -55°C
⑤ Industrial grade devices shall be 100% tested at 25°C only.
⑥ Tested with a low duty cycle pulse to minimize junction heating.
⑦ The typical internal reading is for the die only. This should be used for thermal calculations only.
⑧ Continuous operation at or above absolute maximum ratings may adversly effect the device performance and/or life cycle.
⑨ Internal solder reflow temperature is 180°C, do not exceed.

APPLICATION NOTES

MSK4206 PIN DESCRIPTION

+VS - Is the voltage supply for powering internal logic and drivers as well as H-bridge supply pin. The MOSFETS obtain the drive current from this supply pin. The MOSFETs are rated at 100 volts. Proper bypassing to GND with sufficient capacitance to suppress any voltage transients, and ensure removal of any drooping during switching, should be done as close to the pin on the hybrid as possible.

AOUT - Is the output pin for one half of the bridge. As EA OUT goes more positive the duty cycles increases at this output.

BOUT - Is the output pin for one half of the bridge. As EA OUT goes more positive the duty cycles decreases at this output.

ISENSE - Is the connection for the bottom of the half bridge. This can have a sense resistor connection to the +Vs return ground for current limit sensing, or can be connected directly to ground. The maximum voltage on this pin is ±5V with respect to GND.

GND - Is the return connection for +VS.

+IN - Is the non-inverting input to the internal error amplifier. This pin requires a level between 2 and 8V for proper operation.

-IN - Is the inverting input to the internal error amplifier.

EA OUT - Is the output of the internal error amplifier. The error amplifier output is connected internally to the PWM. An error amp output voltage higher than 5V will produce greater than 50% duty cycle pulses out of A OUT. An error amp voltage lower than 5V will produce greater than 50% duty cycle pulses out of B OUT.

REF - Is the output of the internal precision reference. The internal reference will provide 7.5V with load current up to 5mA.

SHDN/FILTER - Is the connection for disabling all 4 output switches. SHUTDOWN high overrides all other inputs. When taken low, everything functions normally. This pin should be grounded if not used.

CURRENT LIMIT

The current limit function sets the peak limit on current flow in pin 8. This circuit can trip at anytime during the conduction period and will hold the output transistors off for the remainder of that conduction period. It is recommended that RLIMIT resistor be non-inductive. Load current flows in the ISENSE pin. To avoid errors due to lead length connect the SHDN/FILTER pin directly to the RLIMIT resistor (through the filter network and shutdown divider resistor) and connect the RLIMIT resistor directly to the +VS return. Switching noise spikes will invariably be found at the ISENSE pin. The noise spikes could trip the current limit threshold which is only 200mV. RFILTER and CFILTER should be adjusted so as to reduce the switching noise well below 200mV to prevent false current limiting. The sum of the DC level plus the noise peak will determine the current limiting value. As in most switching circuits it may be difficult to determine the true noise amplitude without careful attention to grounding of the oscilloscope probe. Use the shortest possible ground lead for the probe and connect exactly at the GND pin of the amplifier. Suggested starting values are CFILTER=0.01µF, RFILTER=5K. The required value of RLIMIT in voltage mode may be calculated by:

RLIMIT=0.2V/ILIMIT where RLIMIT is the required resistor value and ILIMIT is the maximum desired current. If RSHDN is used it will further divide down the sense voltage. The shutdown divider network will also have an effect on the filtering circuit.

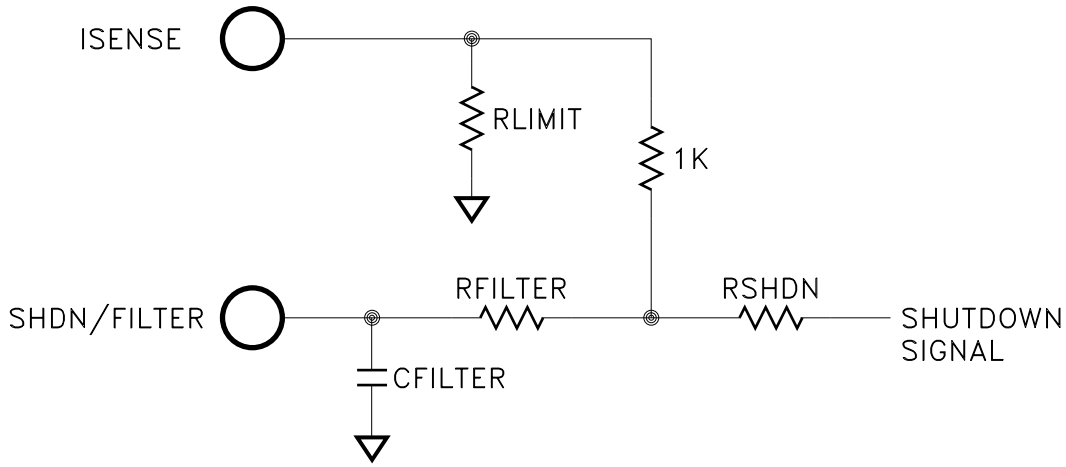


FIGURE 1

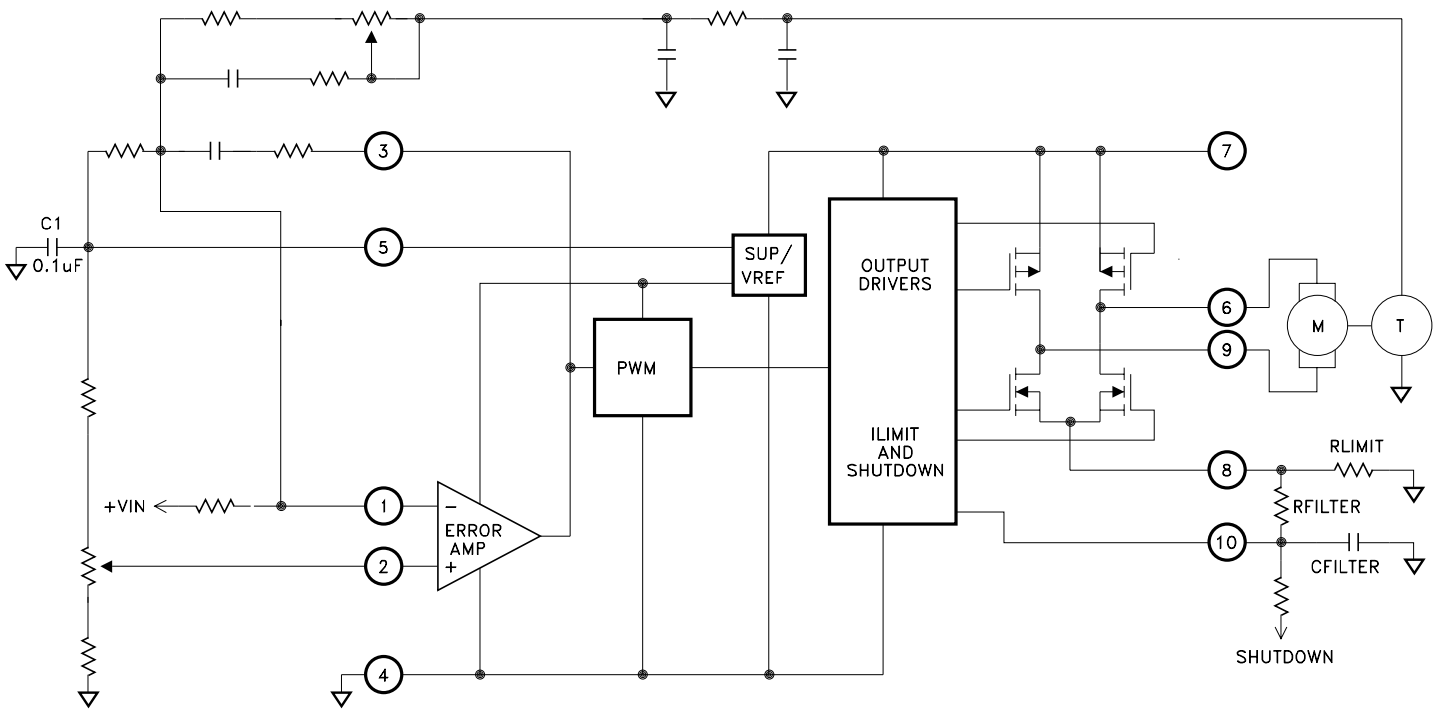
ERROR AMPLIFIER

The internal amplifier can be used to integrate the difference between command signals and feedback signals. For highest loop accurancy it is best to configure the error amplifier as an integrator. Poles and zeros must be selected to provide circuit stability while maximizing system respones. Specific component values will vary from system to system. The 7.5V reference output can be used to bias the non-inverting input of the error amplifier to the middle of its 2 to 8V common mode voltage range. (See typical application circuit).

PROTECTION CIRCUITS

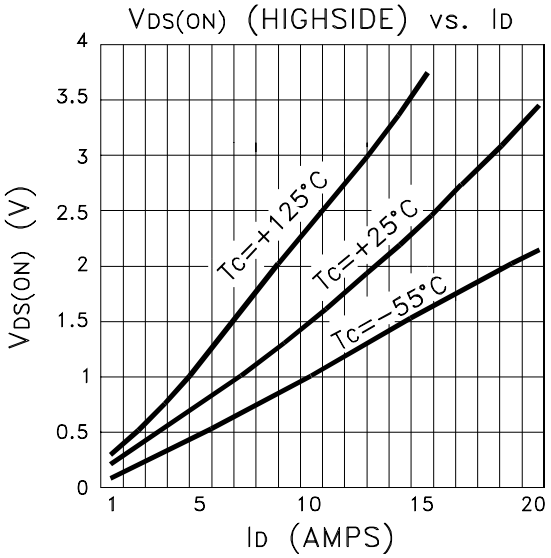
In addition to the externally programmable current limit there is also a fixed internal current limit which senses only the highside current. The DC trip level is approximately 35A. Should either of the outputs be shorted to ground the highside current limit will latch off the output transistors. It will be necessary to remove the fault condition and recycle power to +VS to restart the circuit.

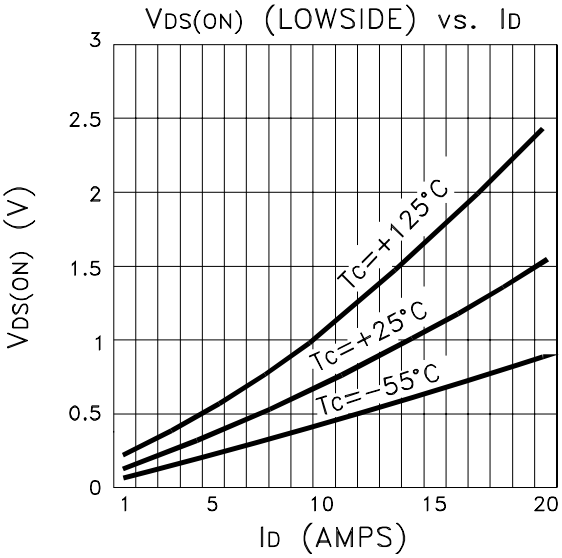
TYPICAL APPLICATION CIRCUIT

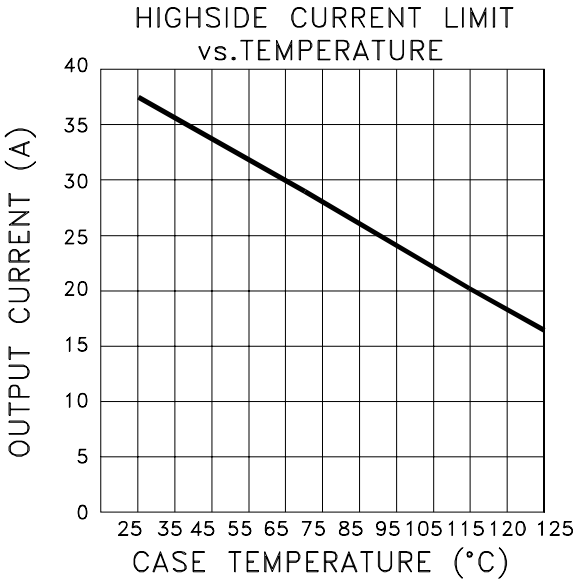


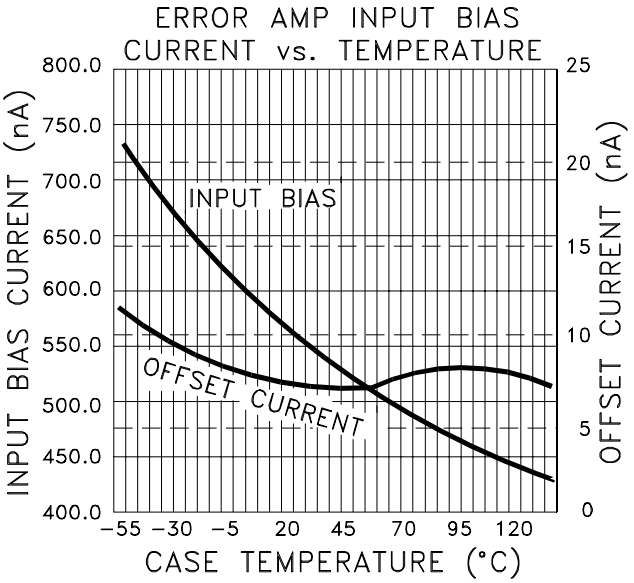
MOTOR DRIVER WITH TACH FEEDBACK

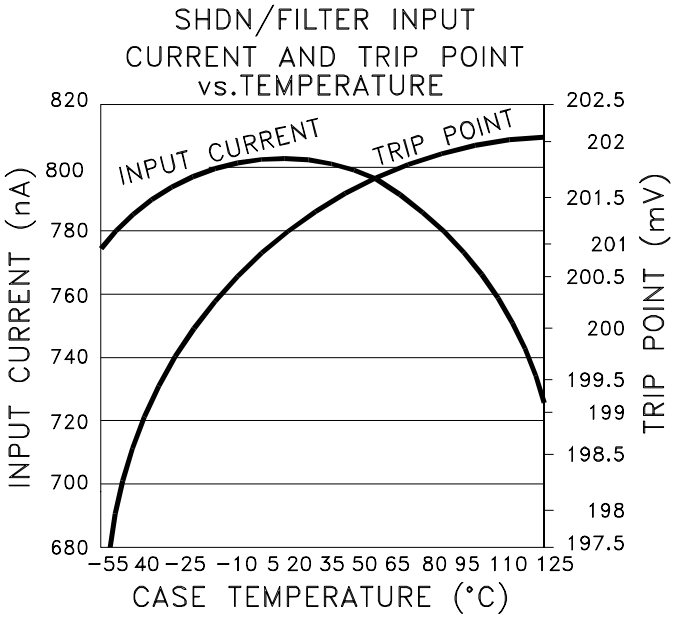
PERFORMANCE CURVES

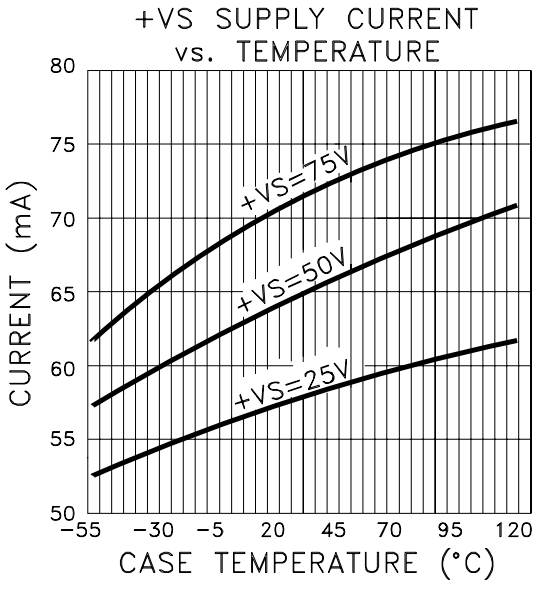




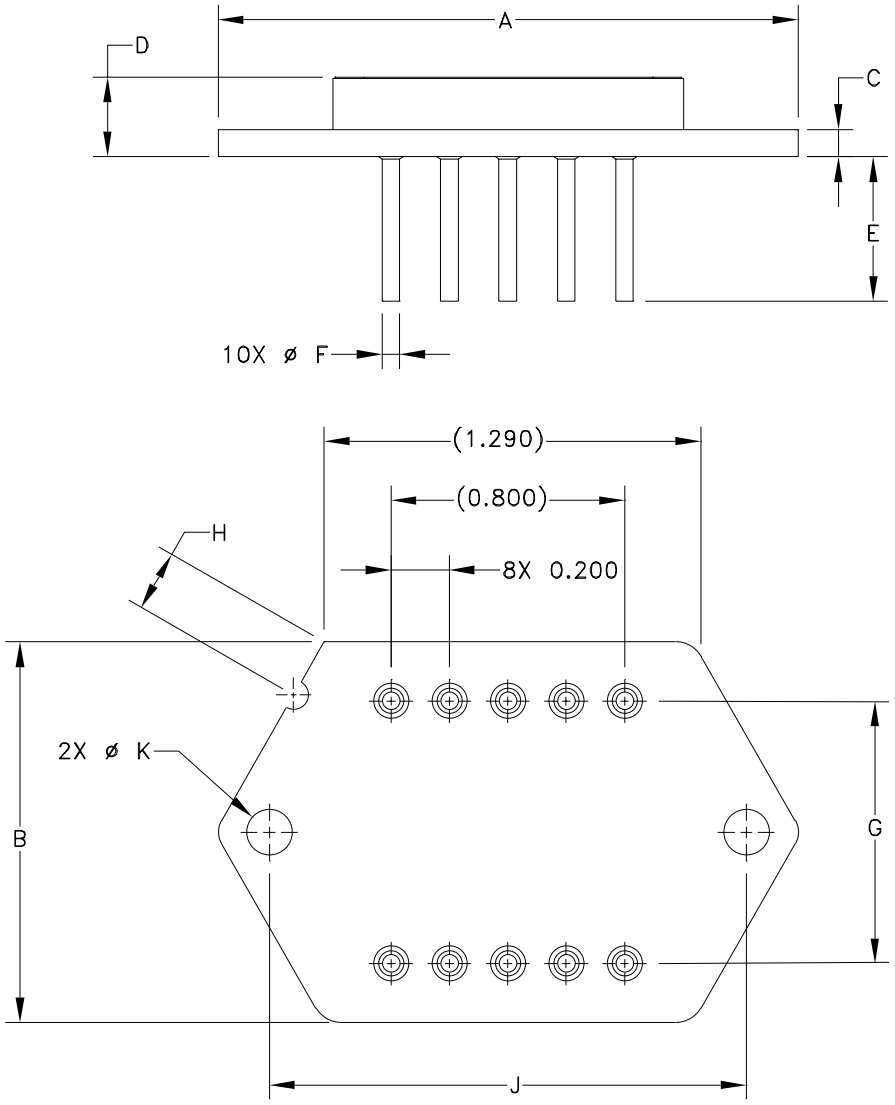








MECHANICAL SPECIFICATIONS



REF	MIN	MAX
A	1.977	1.997
B	1.295	1.315
C	0.088	0.098
D	———	0.290
E	0.450	0.500
F	0.058	0.062
G	0.895	0.905
H	0.200	0.220
J	1.629	1.639
K	0.154	0.158

WEIGHT= 35 GRAMS TYPICAL
TORQUE SPEC: 8-10 IN-LBS

ALL DIMENSIONS ARE SPECIFIED IN INCHES

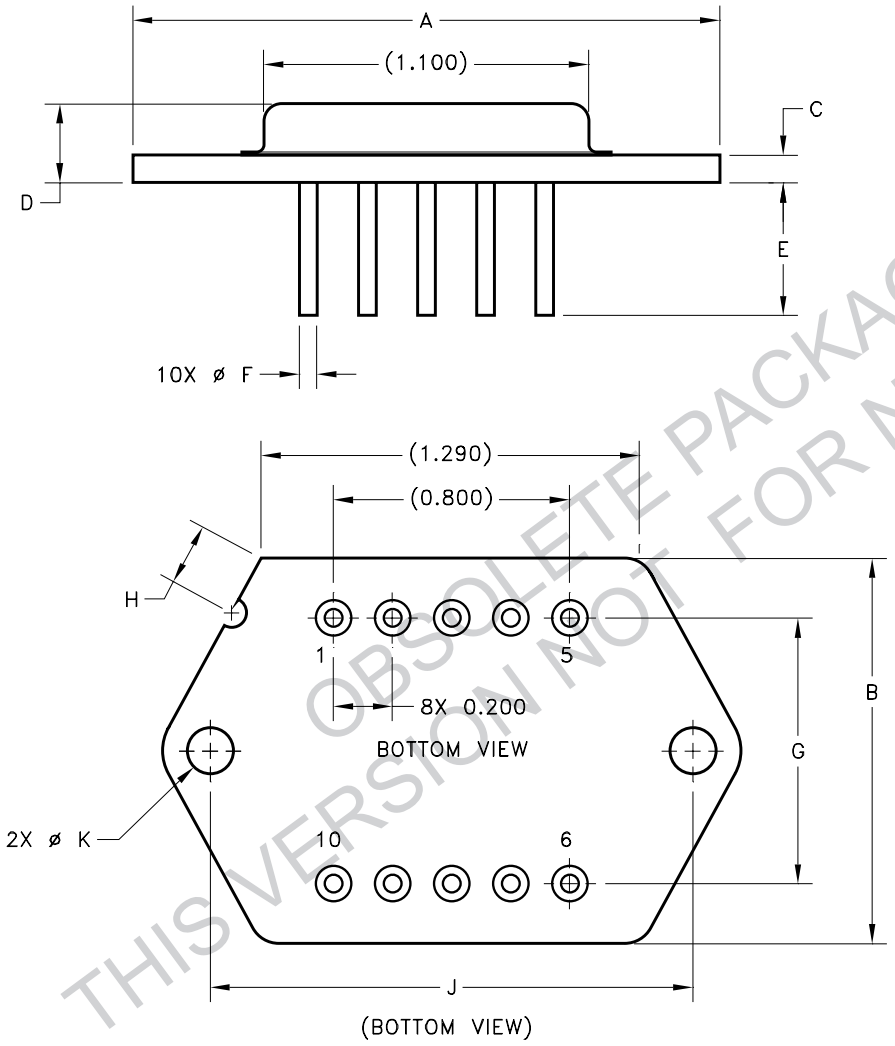
ORDERING INFORMATION

MSK4206H

SCREENING
BLANK= INDUSTRIAL
H=MIL-PRF-38534 CLASS H

GENERAL PART NUMBER

The above example is a Military grade class H hybrid.



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REVISION HISTORY

REV	STATUS	DATE	DESCRIPTION
B	Released	10/14	Format update, add internal note and clarify mechanical specifications.
C	Released	05/17	Package update

MSK
www.anaren.com/MSK