

FAN7530

Critical Conduction Mode PFC Controller

Features

- Low Total Harmonic Distortion (THD)
- Precise Adjustable Output Over-Voltage Protection
- Open-Feedback Protection and Disable Function
- Zero Current Detector
- 150µs Internal Start-up Timer
- MOSFET Over-Current Protection
- Under-Voltage Lockout with 3.5V Hysteresis
- Low Start-up (40µA) and Operating Current (1.5mA)
- Totem Pole Output with High State Clamp
- +500/-800mA Peak Gate Drive Current
- 8-Pin DIP or 8-Pin SOP

Applications

- Adapter
- Ballast
- LCD TV, CRT TV
- SMPS

Related Application Notes

- **AN-6027** - *Design of Power Factor Correction Circuit Using FAN7530*

Description

The FAN7530 is an active power factor correction (PFC) controller for boost PFC applications that operates in critical conduction mode (CRM). It uses the voltage mode PWM that compares an internal ramp signal with the error amplifier output to generate MOSFET turn-off signal. Since the voltage mode CRM PFC controller does not need rectified AC line voltage information, it saves the power loss of the input voltage sensing network necessary for the current mode CRM PFC controller.

FAN7530 provides many protection functions, such as over voltage protection, open-feedback protection, over-current protection, and under-voltage lockout protection. The FAN7530 can be disabled if the INV pin voltage is lower than 0.45V and the operating current decreases to 65µA. Using a new variable on-time control method, THD is lower than the conventional CRM boost PFC ICs.

Ordering Information

| Part Number | Operating Temp. Range | Pb-Free | Package | Packing Method | Marking Code |
|-------------|-----------------------|---------|---------|----------------|--------------|
| FAN7530N | -40°C to +125°C | Yes | 8-DIP | Rail | FAN7530 |
| FAN7530M | -40°C to +125°C | Yes | 8-SOP | Rail | FAN7530 |
| FAN7530MX | -40°C to +125°C | Yes | 8-SOP | Tape & Reel | FAN7530 |

Typical Application Diagrams

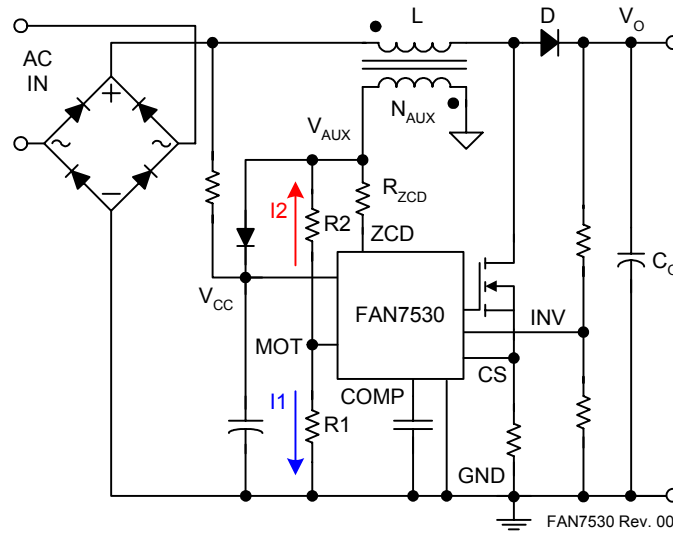


Figure 1. Typical Boost PFC Application

Internal Block Diagram

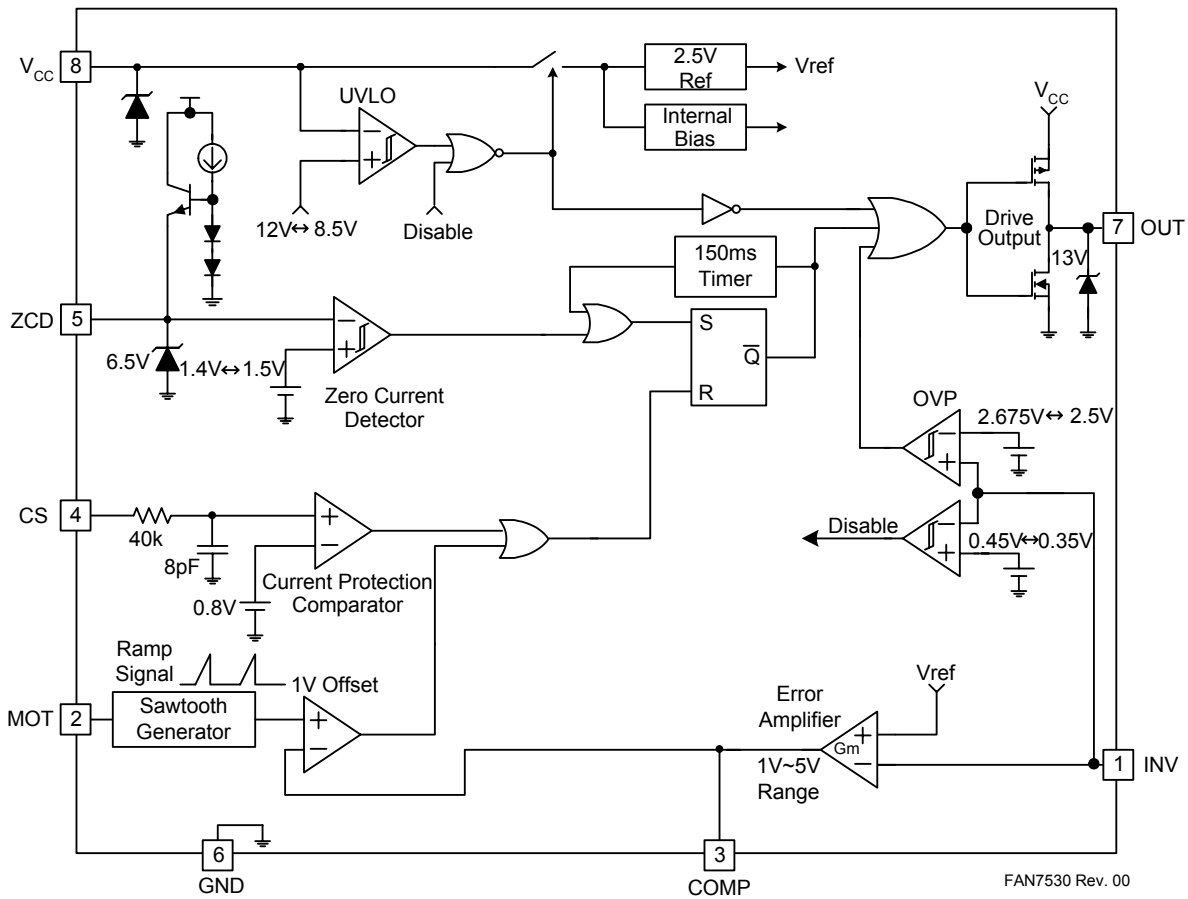


Figure 2. Functional Block Diagram of FAN7530

Pin Assignments

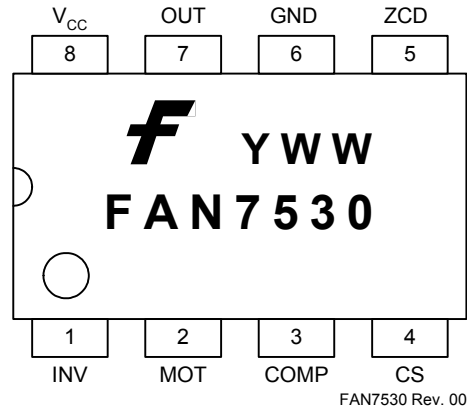


Figure 3. Pin Configuration (Top View)

Pin Definitions

| Pin # | Name | Description |
|-------|------|--|
| 1 | INV | This pin is the inverting input of the error amplifier. The output voltage of the boost PFC converter should resistively divided to 2.5V. |
| 2 | MOT | This pin is used to set the slope of the internal ramp. The voltage of this pin is maintained at 2.9V. If a resistor is connected between this pin and GND, current flows out of the pin and the slope of the internal ramp is proportional to this current. |
| 3 | COMP | This pin is the output of the transconductance error amplifier. Components for the output voltage compensation should be connected between this pin and GND. |
| 4 | CS | This pin is the input of the over-current protection comparator. The MOSFET current is sensed using a sensing resistor and the resulting voltage is applied to this pin. An internal RC filter is included to filter switching noise. |
| 5 | ZCD | This pin is the input of the zero current detection block. If the voltage of this pin goes higher than 1.5V, then goes lower than 1.4V, the MOSFET is turned on. |
| 6 | GND | This pin is used for the ground potential of all the pins. For proper operation, the signal ground and the power ground should be separated. |
| 7 | OUT | This pin is the gate drive output. The peak sourcing and sinking current levels are +500mA and -800mA respectively. For proper operation, the stray inductance in the gate driving path must be minimized. |
| 8 | Vcc | This pin is the IC supply pin. IC current and MOSFET drive current are supplied using this pin. |

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. $T_A=25^{\circ}\text{C}$, unless otherwise specified.

| Symbol | Parameter | Value | Unit |
|------------------|--|------------|--------------------|
| V_{CC} | Supply Voltage | V_Z | V |
| I_{OH}, I_{OL} | Peak Drive Output Current | +500/-800 | mA |
| I_{clamp} | Driver Output Clamping Diodes $V_O > V_{CC}$ or $V_O < -0.3\text{V}$ | ± 10 | mA |
| I_{det} | Detector Clamping Diodes | ± 10 | mA |
| V_{IN} | Error Amplifier, MOT, CS Input Voltages | -0.3 to 6 | V |
| T_J | Operating Junction Temperature | 150 | $^{\circ}\text{C}$ |
| T_A | Operating Temperature Range | -40 to 125 | $^{\circ}\text{C}$ |
| T_{STG} | Storage Temperature Range | -65 to 150 | $^{\circ}\text{C}$ |
| V_{ESD_HBM} | ESD Capability, Human Body Model | 2.0 | kV |
| V_{ESD_MM} | ESD Capability, Machine Model | 300 | V |
| V_{ESD_CDM} | ESD Capability, Charged Device Model | 500 | V |

Thermal Impedance⁽¹⁾

| Symbol | Parameter | Value | Unit | |
|---------------|---|-------|------|-----------------------------|
| θ_{JA} | Thermal Resistance, Junction-to-Ambient | 8-DIP | 110 | $^{\circ}\text{C}/\text{W}$ |
| | | 8-SOP | 150 | $^{\circ}\text{C}/\text{W}$ |

Note:

- Regarding the test environment and PCB type, please refer to JESD51-2 and JESD51-10.

Electrical Characteristics

$V_{CC} = 14V$ and $T_A = -40^{\circ}C \sim 125^{\circ}C$ unless otherwise specified.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|--------------------------------------|--|--|-------|-------|-------|-----------|
| UNDER-VOLTAGE LOCKOUT SECTION | | | | | | |
| $V_{th(start)}$ | Start Threshold Voltage | V_{CC} increasing | 11 | 12 | 13 | V |
| $V_{th(stop)}$ | Stop Threshold Voltage | V_{CC} decreasing | 7.5 | 8.5 | 9.5 | V |
| $HY_{(uvlo)}$ | UVLO Hysteresis | | 3.0 | 3.5 | 4.0 | V |
| V_Z | Zener Voltage | $I_{CC} = 20mA$ | | 22 | | V |
| SUPPLY CURRENT SECTION | | | | | | |
| I_{st} | Start-up Supply Current | $V_{CC} = V_{th(start)} - 0.2V$ | | 40 | 70 | μA |
| I_{CC} | Operating Supply Current | Output no switching | | 1.5 | 3.0 | mA |
| I_{dCC} | Dynamic Operating Supply Current | 50kHz, $C_L = 1nF$ | | 2.5 | 4.0 | mA |
| $I_{CC(dis)}$ | Operating Current at Disable | $V_{inv} = 0V$ | 20 | 65 | 95 | μA |
| ERROR AMPLIFIER SECTION | | | | | | |
| V_{ref1} | Voltage Feedback Input Threshold 1 | $T_A = 25^{\circ}C$ | 2.465 | 2.500 | 2.535 | V |
| ΔV_{ref1} | Line Regulation | $V_{CC} = 14V \sim 20V$ | | 0.1 | 10.0 | mV |
| ΔV_{ref2} | Temperature Stability of $V_{ref1}^{(2)}$ | | | 20 | | mV |
| $I_{b(ea)}$ | Input Bias Current | $V_{inv} = 1V \sim 4V$ | -0.5 | | 0.5 | μA |
| I_{source} | Output Source Current | $V_{inv} = V_{ref1} - 0.1V$ | | -12 | | μA |
| I_{sink} | Output Sink Current | $V_{inv} = V_{ref1} + 0.1V$ | | 12 | | μA |
| $V_{eao(H)}$ | Output Upper Clamp Voltage | $V_{inv} = V_{ref1} - 0.1V$ | 5.4 | 6.0 | 6.6 | V |
| $V_{eao(Z)}$ | Zero Duty Cycle Output Voltage | | 0.9 | 1.0 | 1.1 | V |
| g_m | Transconductance ⁽²⁾ | | 90 | 115 | 140 | μmho |
| MAXIMUM ON-TIME SECTION | | | | | | |
| V_{mot} | Maximum On-Time Voltage | $R_{mot} = 40.5k\Omega$ | 2.784 | 2.900 | 3.016 | V |
| $t_{on(max)}$ | Maximum On-Time Programming | $R_{mot} = 40.5k\Omega, T_A = 25^{\circ}C$ | 19 | 24 | 29 | μsec |
| CURRENT SENSE SECTION | | | | | | |
| $V_{CS(limit)}$ | Current Sense Input Threshold Voltage Limit | | 0.7 | 0.8 | 0.9 | V |
| $I_{b(cs)}$ | Input Bias Current | $V_{CS} = 0V \sim 1V$ | -1.0 | -0.1 | 1.0 | μA |
| $t_{d(cs)}$ | Current Sense Delay to Output ⁽²⁾ | $dV/dt = 1V/100ns,$ from 0V to 5V | | 350 | 500 | nsec |

Note:

2. These parameters, although guaranteed by design, are not tested in production.

Electrical Characteristics (Continued)

$V_{CC} = 14V$ and $T_A = -40^{\circ}C \sim 125^{\circ}C$ unless otherwise specified.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|--|---|--|-------|-------|-------|-----------|
| ZERO CURRENT DETECT SECTION | | | | | | |
| $V_{th(ZCD)}$ | Input Voltage Threshold ⁽³⁾ | | 1.35 | 1.50 | 1.65 | V |
| $HY_{(ZCD)}$ | Detect Hysteresis ⁽³⁾ | | 0.05 | 0.10 | 0.15 | V |
| $V_{clamp(H)}$ | Input High Clamp Voltage | $I_{det} = 3mA$ | 6.0 | 6.7 | 7.4 | V |
| $V_{clamp(L)}$ | Input Low Clamp Voltage | $I_{det} = -3mA$ | 0 | 0.65 | 1.00 | V |
| $I_{b(ZCD)}$ | Input Bias Current | $V_{ZCD} = 1V \sim 5V$ | -1.0 | -0.1 | 1.0 | μA |
| $I_{source(zcd)}$ | Source Current Capability ⁽³⁾ | $T_A = 25^{\circ}C$ | | | -10 | mA |
| $I_{sink(zcd)}$ | Sink Current Capability ⁽³⁾ | $T_A = 25^{\circ}C$ | | | 10 | mA |
| t_{dead} | Maximum Delay from ZCD to Output Turn-on ⁽³⁾ | $dV/dt = -1V/100ns$, from 5V to 0V | 100 | | 200 | nsec |
| OUTPUT SECTION | | | | | | |
| V_{OH} | Output Voltage High | $I_O = -100mA$, $T_A = 25^{\circ}C$ | 9.2 | 11.0 | 12.8 | V |
| V_{OL} | Output Voltage Low | $I_O = 200mA$, $T_A = 25^{\circ}C$ | | 1.0 | 2.5 | V |
| t_r | Rising Time ⁽³⁾ | $Cl = 1nF$ | | 50 | 100 | nsec |
| t_f | Falling Time ⁽³⁾ | $Cl = 1nF$ | | 50 | 100 | nsec |
| $V_{O(max)}$ | Maximum Output Voltage | $V_{CC} = 20V$, $I_O = 100\mu A$ | 11.5 | 13.0 | 14.5 | V |
| $V_{O(UVLO)}$ | Output Voltage with UVLO Activated | $V_{CC} = 5V$, $I_O = 100\mu A$ | | | 1 | V |
| RESTART TIMER SECTION | | | | | | |
| $t_{d(rst)}$ | Restart Timer Delay | | 50 | 150 | 300 | μsec |
| OVER-VOLTAGE PROTECTION SECTION | | | | | | |
| V_{ovp} | OVP Threshold Voltage | $T_A = 25^{\circ}C$ | 2.620 | 2.675 | 2.730 | V |
| $HY_{(ovp)}$ | OVP Hysteresis | $T_A = 25^{\circ}C$ | 0.120 | 0.175 | 0.230 | V |
| ENABLE SECTION | | | | | | |
| $V_{th(en)}$ | Enable Threshold Voltage | | 0.40 | 0.45 | 0.50 | V |
| $HY_{(en)}$ | Enable Hysteresis | | 0.05 | 0.10 | 0.15 | V |

Note:

3. These parameters, although guaranteed by design, are not tested in production.

Typical Characteristics

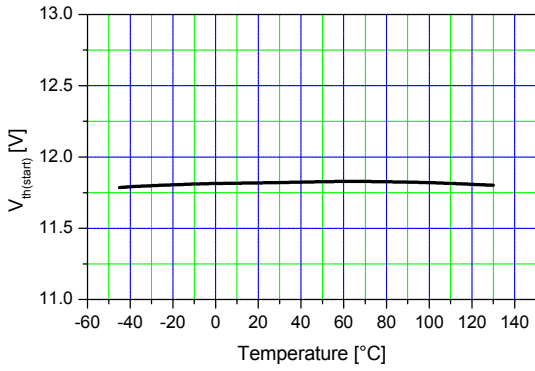


Figure 4. Start Threshold Voltage vs. Temp.

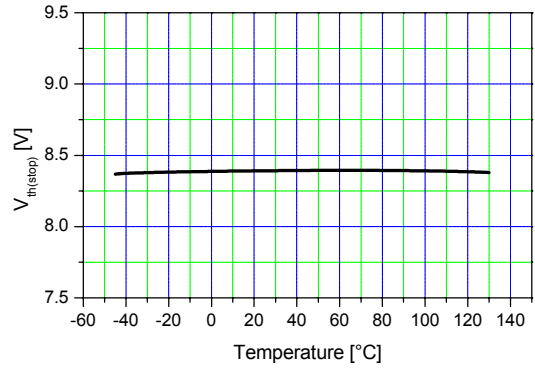


Figure 5. Stop Threshold Voltage vs. Temp.

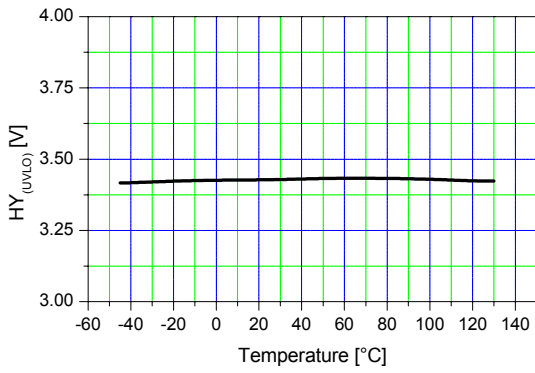


Figure 6. UVLO Hysteresis vs. Temp.

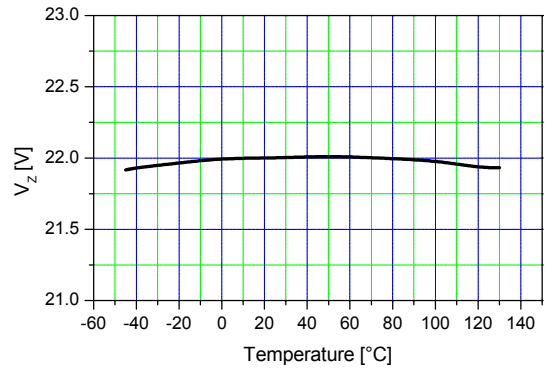


Figure 7. Zener Voltage vs. Temp.

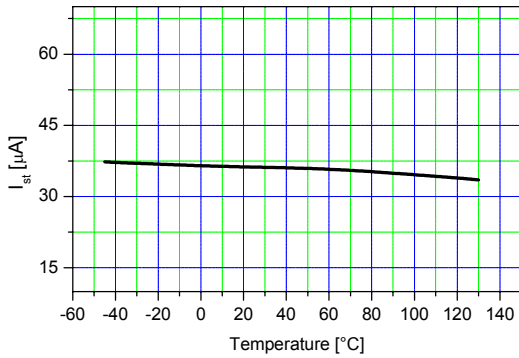


Figure 8. Start-up Supply Current vs. Temp.

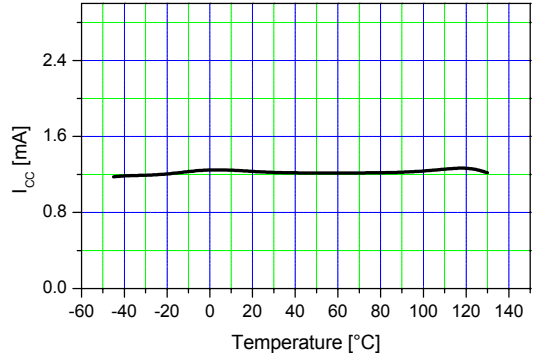


Figure 9. Operating Supply Current vs. Temp.

Typical Characteristics (Continued)

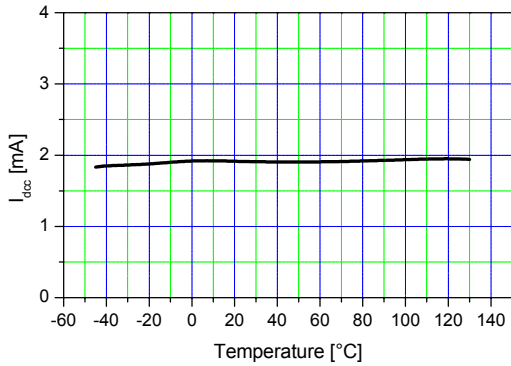


Figure 10. Dynamic Operating Supply Current vs. Temp.

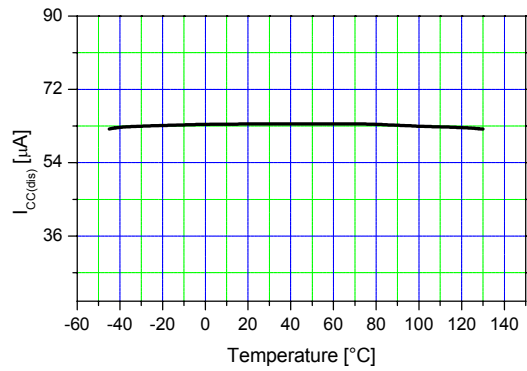


Figure 11. Operating Current at Disable vs. Temp.

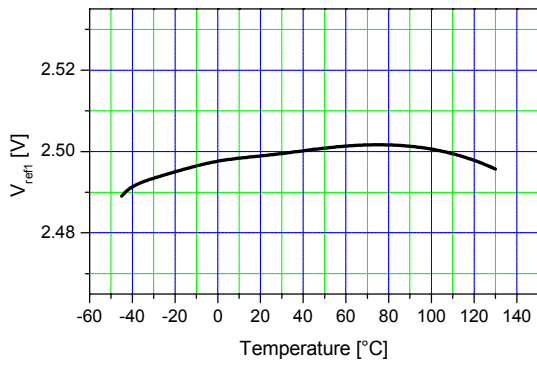


Figure 12. V_{ref1} vs. Temp.

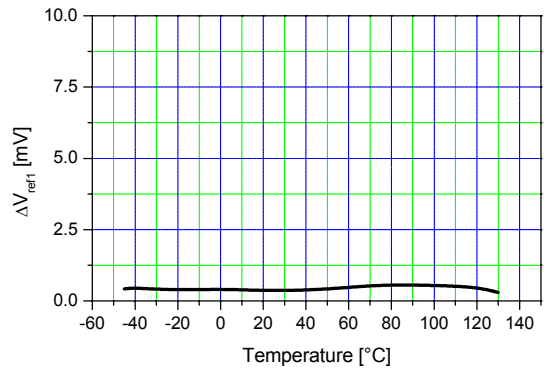


Figure 13. ΔV_{ref1} vs. Temp.

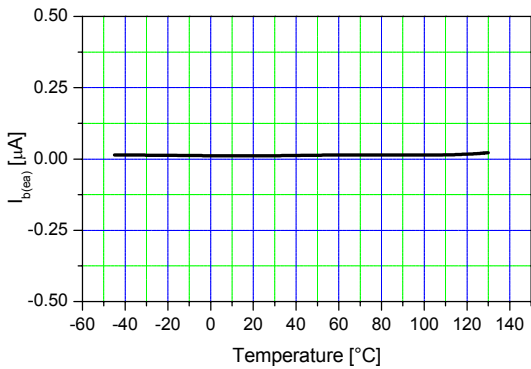


Figure 14. Input Bias Current vs. Temp.

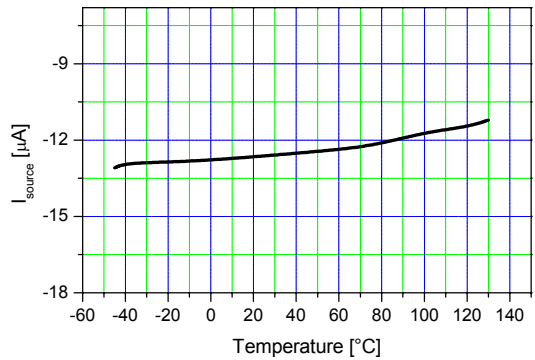


Figure 15. Output Source Current vs. Temp.

Typical Characteristics (Continued)

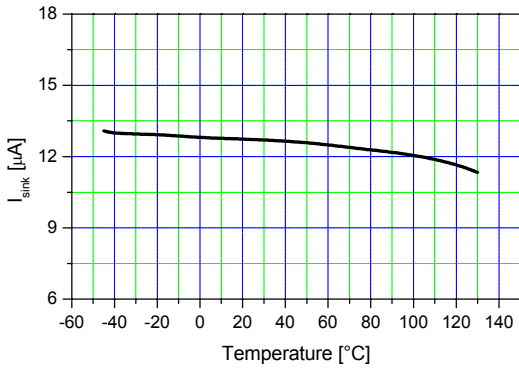


Figure 16. Output Sink Current vs. Temp.

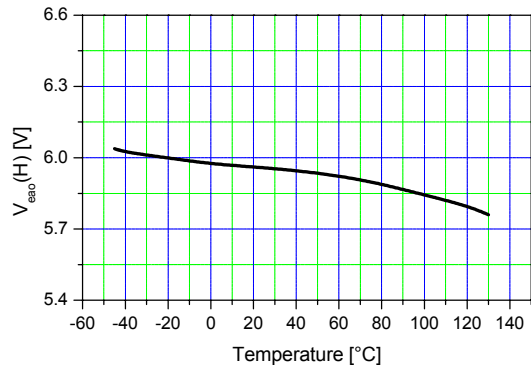


Figure 17. Output Upper Clamp Voltage vs. Temp.

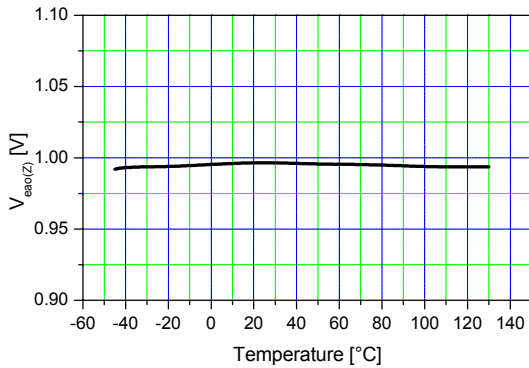


Figure 18. Zero Duty Cycle Output Voltage vs. Temp.

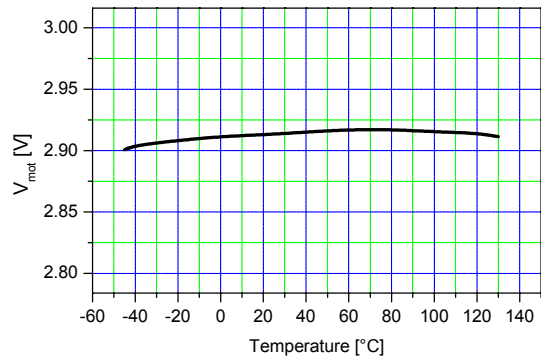


Figure 19. Maximum On-Time Voltage vs. Temp.

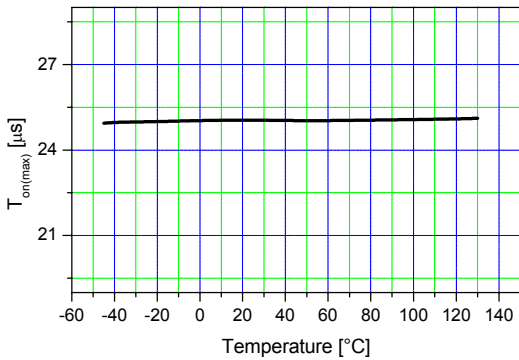


Figure 20. Maximum On-Time vs. Temp.

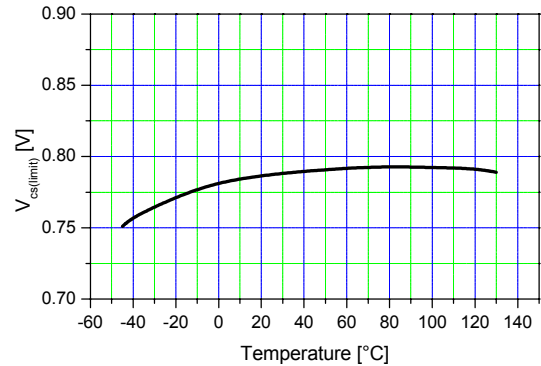


Figure 21. Current Sense Input Threshold Voltage vs. Temp.

Typical Characteristics (Continued)

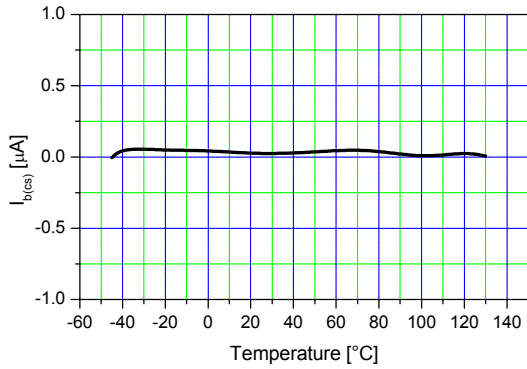


Figure 22. Input Bias Current vs. Temp.

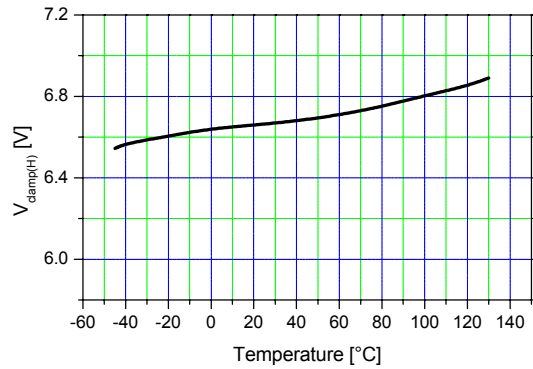


Figure 23. Input High Clamp Voltage vs. Temp.

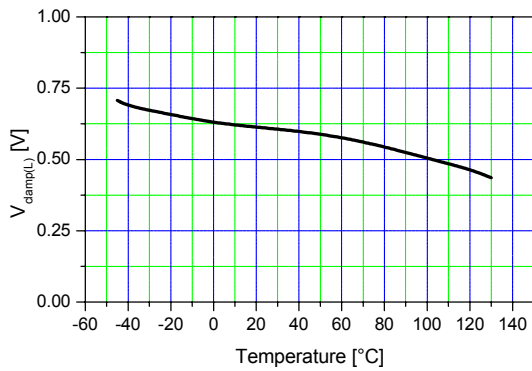


Figure 24. Input Low Clamp Voltage vs. Temp.

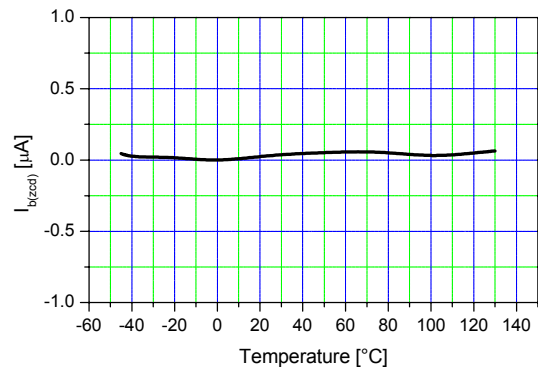


Figure 25. Input Bias Current vs. Temp.

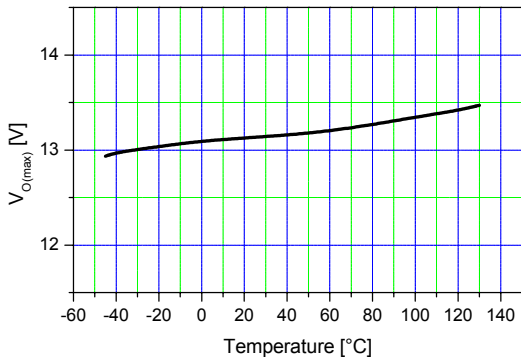


Figure 26. Maximum Output Voltage vs. Temp.

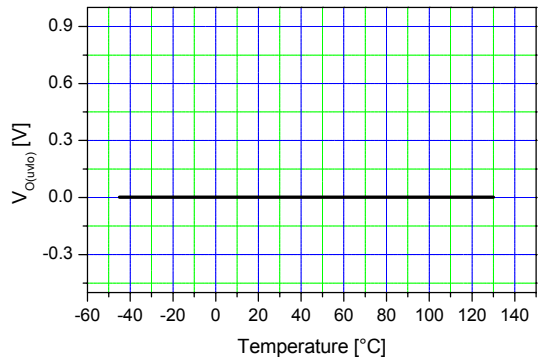


Figure 27. Output Voltage with UVLO Activated vs. Temp.

Typical Characteristics (Continued)

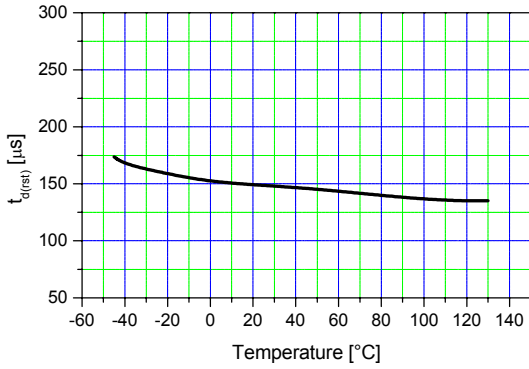


Figure 28. Restart Delay Time vs. Temp.

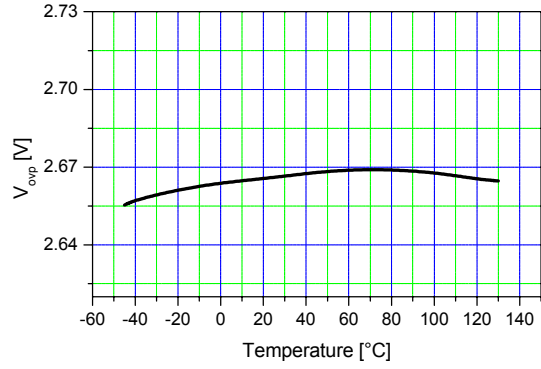


Figure 29. OVP Threshold Voltage vs. Temp.

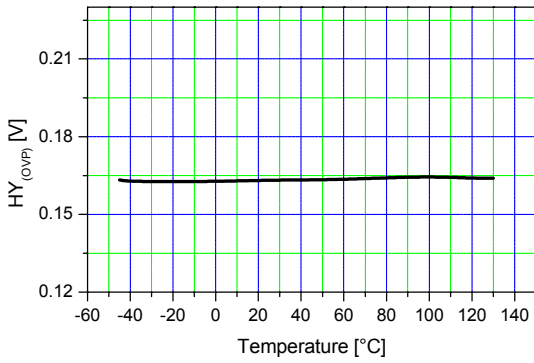


Figure 30. OVP Hysteresis vs. Temp.

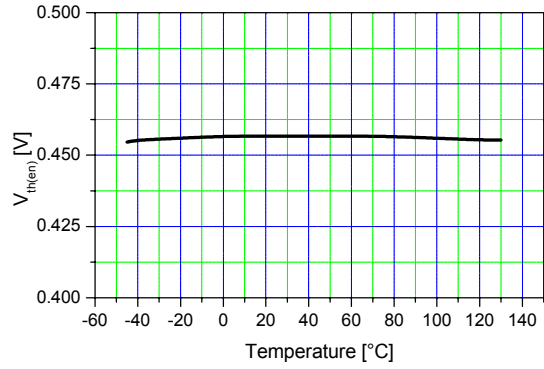


Figure 31. Enable Threshold Voltage vs. Temp.

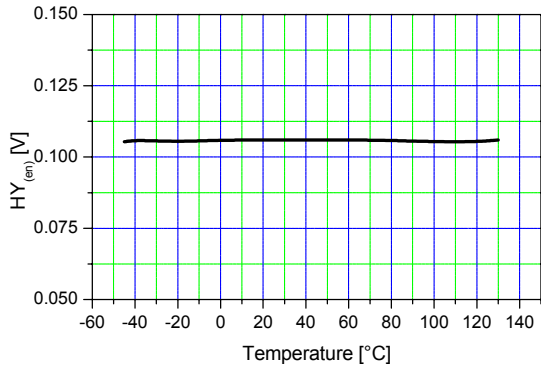


Figure 32. Enable Hysteresis vs. Temp.

Applications Information

1. Error Amplifier Block

The error amplifier block consists of a transconductance amplifier, output OVP comparator, and disable comparator. For the output voltage control, a transconductance amplifier is used instead of the conventional voltage amplifier. The transconductance amplifier (voltage controlled current source) aids the implementation of OVP and disable function. The output current of the amplifier changes according to the voltage difference of the inverting and non-inverting input of the amplifier. The output voltage of the amplifier is compared with the internal ramp signal to generate the switch turn-off signal. The OVP comparator shuts down the output drive block when the voltage of the INV pin is higher than 2.675V and there is 0.175V hysteresis. The disable comparator disables the operation of the FAN7530 when the voltage of the inverting input is lower than 0.45V and there is 100mV hysteresis. An external small signal MOSFET can be used to disable the IC, as shown in Figure 33. The IC operating current decreases below 65μA to reduce power consumption if the IC is disabled.

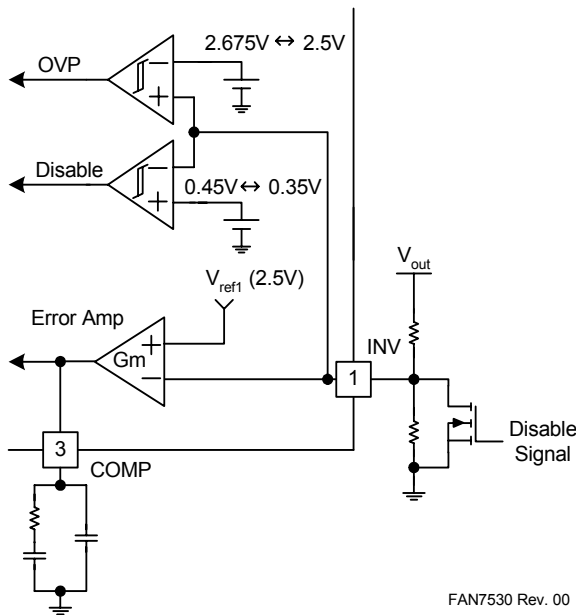


Figure 33. Error Amplifier Block

2. Zero Current Detection Block

The zero current detector (ZCD) generates the turn-on signal of the MOSFET when the boost inductor current reaches zero using an auxiliary winding coupled with the inductor. If the voltage of the ZCD pin goes higher than 1.5V, the ZCD comparator waits until the voltage goes below 1.4V. If the voltage goes below 1.4V, the zero cur-

rent detector turns on the MOSFET. The ZCD pin is protected internally by two clamps, 6.7V-high clamp and 0.65V-low clamp. The 150μs timer generates a MOSFET turn-on signal if the drive output has been low for more than 150μs from the falling edge of the drive output.

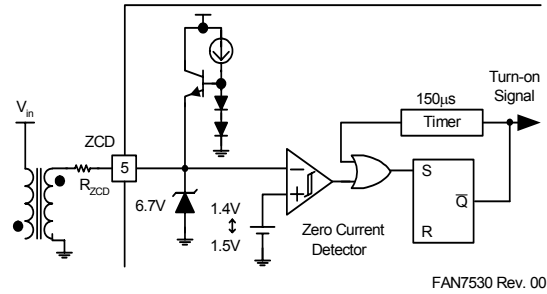


Figure 34. Zero Current Detector Block

3. Sawtooth Generator Block

The output of the error amplifier and the output of the sawtooth generator are compared to determine the MOSFET turn-off instance. The slope of the sawtooth is determined by an external resistor connected to the MOT pin. The voltage of the MOT pin is 2.9V and the slope is proportional to the current flowing out of the MOT pin. The internal ramp signal has a 1V offset; therefore, the drive output is shut down if the voltage of the COMP pin is lower than 1V. The MOSFET on-time is maximum when the COMP pin voltage is 5V. According to the slope of the internal ramp, the maximum on-time can be programmed. The necessary maximum on-time depends on the boost inductor, lowest AC line voltage, and maximum output power. The resistor value should be designed properly.

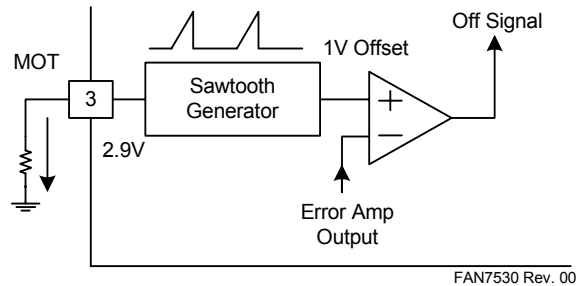


Figure 35. Sawtooth Generator Block

4. Over-Current Protection Block

The MOSFET current is sensed using an external sensing resistor for the over-current protection. If the CS pin voltage is higher than 0.8V, the over-current protection comparator generates a protection signal. An internal RC filter is included to filter switching noise.

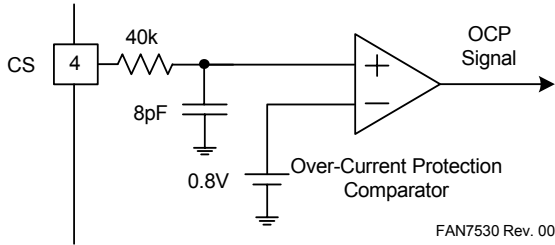


Figure 36. Over-Current Protection Block

5. Switch Drive Block

The FAN7530 contains a single totem-pole output stage designed for direct drive of the power MOSFET. The drive output is capable of up to +500/-800mA peak current with a typical rise and fall time of 50ns with 1nF load. The output voltage is clamped to 13V to protect the MOSFET gate if the V_{CC} voltage is higher than 13V.

6. Under-Voltage Lockout Block

If the V_{CC} voltage reaches 12V, the IC's internal blocks are enabled and start operation. If the V_{CC} voltage drops below 8.5V, most of the internal blocks are disabled to reduce the operating current. V_{CC} voltage should be higher than 8.5V under normal conditions.

Typical Application Circuit

| Application | Output Power | Input Voltage | Output Voltage |
|-------------|--------------|--|----------------|
| Ballast | 100W | Universal input (85~265V _{AC}) | 400V |

Features

- High efficiency (>90% at 85V_{AC} input)
- Low total harmonic distortion (THD) (<10% at 265V_{AC} input, 25W load)

Key Design Notes

- R1, R2, R5, C11 should be optimized for best THD characteristic.

1. Schematic

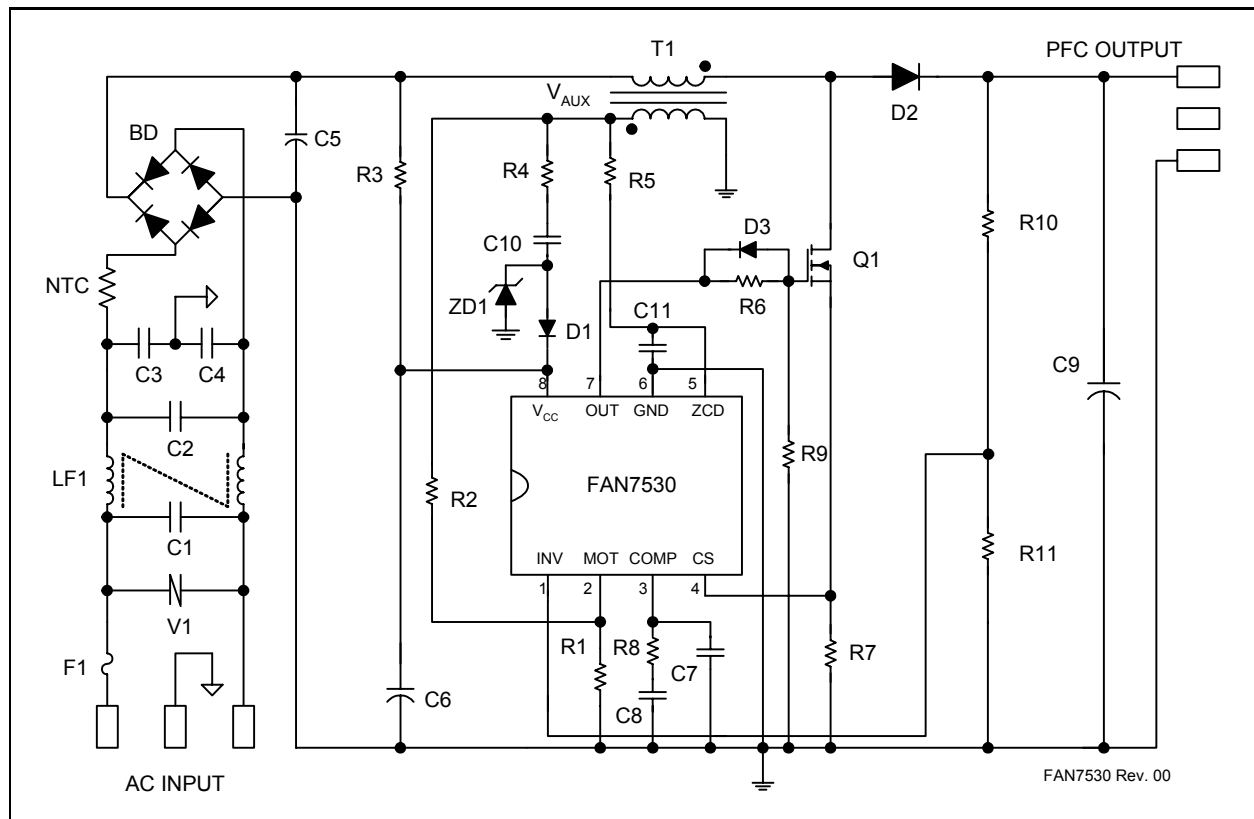


Figure 37. Schematic

2. Inductor Schematic Diagram

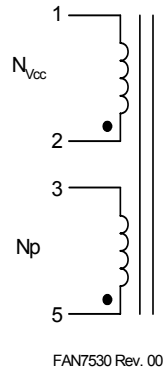


Figure 38. Inductor Schematic Diagram

3. Winding Specification

| No | Pin (s→f) | Wire | Turns | Winding Method |
|--|-----------|----------------------|-------|------------------|
| N_{Vcc} | 2 → 1 | $0.2^\phi \times 1$ | 8 | Solenoid Winding |
| Insulation: Polyester Tape $t = 0.050\text{mm}$, 4 Layers | | | | |
| N_p | 5 → 3 | $0.2^\phi \times 10$ | 58 | Solenoid Winding |
| Outer Insulation: Polyester Tape $t = 0.050\text{mm}$, 4 Layers | | | | |
| Air Gap: 0.6mm for each leg | | | | |

4. Electrical Characteristics

| | Pin | Specification | Remarks |
|------------|-------|---------------------------|------------|
| Inductance | 3 - 5 | $600\mu\text{H} \pm 10\%$ | 100kHz, 1V |

5. Core & Bobbin

- Core: EI 3026
- Bobbin: EI3026
- $A_e(\text{mm}^2)$: 111

6. Demo Circuit Part List

| Part | Value | Note | Part | Value | Note |
|------------------|------------------|------------------------------|---------------------|-------------|------------|
| Fuse | | | Inductor | | |
| F1 | 3A/250V | | T1 | 600 μ H | EI3026 |
| NTC | | | | | |
| NTC | 10D-9 | | MOSFET | | |
| Resistor | | | Q1 | FQPF13N50C | Fairchild |
| R1 | 56k Ω | 1/4W | | | |
| R2 | 820k Ω | 1/4W | Diode | | |
| R3 | 330k Ω | 1/2W | D1 | 1N4148 | Fairchild |
| R4 | 150 Ω | 1/2W | D2 | BYV26C | 600V, 1A |
| R5 | 20k Ω | 1/4W | D3 | SB140 | Fairchild |
| R6 | 10 Ω | 1/4W | ZD1 | 1N4746 | 18V |
| R7 | 0.2 Ω | 1/2W | | | |
| R8 | 10k Ω | 1/4W | | | |
| R9 | 10k Ω | 1/4W | Bridge Diode | | |
| R10 | 2M Ω | 1/4W | BD | KBL06 | 600V/4A |
| R11 | 12.9k Ω | 1/4W | | | |
| | | | Line Filter | | |
| Capacitor | | | LF1 | 40mH | Wire 0.4mm |
| C1 | 150nF/275VAC | Box Capacitor | | | |
| C2 | 470nF/275VAC | Box Capacitor | IC | | |
| C3 | 2.2nF/3kV | Ceramic Capacitor | IC1 | FAN7530 | Fairchild |
| C4 | 2.2nF/3kV | Ceramic Capacitor | | | |
| C5 | | | TNR | | |
| C6 | 47 μ F/25V | Electrolytic Capacitor | V1 | 471 | 470V |
| C7 | 47nF/50V | Ceramic Capacitor | | | |
| C8 | 220nF/50V | Multilayer Ceramic Capacitor | | | |
| C9 | 100 μ F/450V | Electrolytic Capacitor | | | |
| C10 | 12nF/100V | Film Capacitor | | | |
| C11 | 56pF/50V | Ceramic Capacitor | | | |

7. Layout

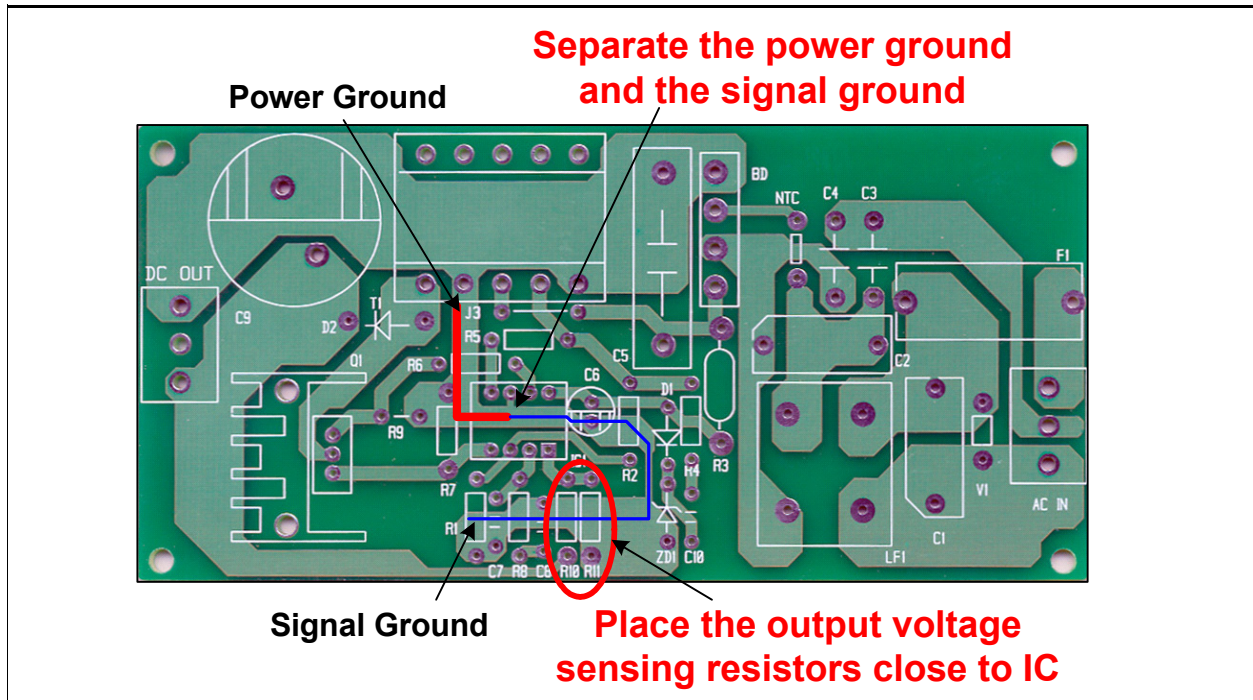


Figure 39. PCB Layout Considerations for FAN7530

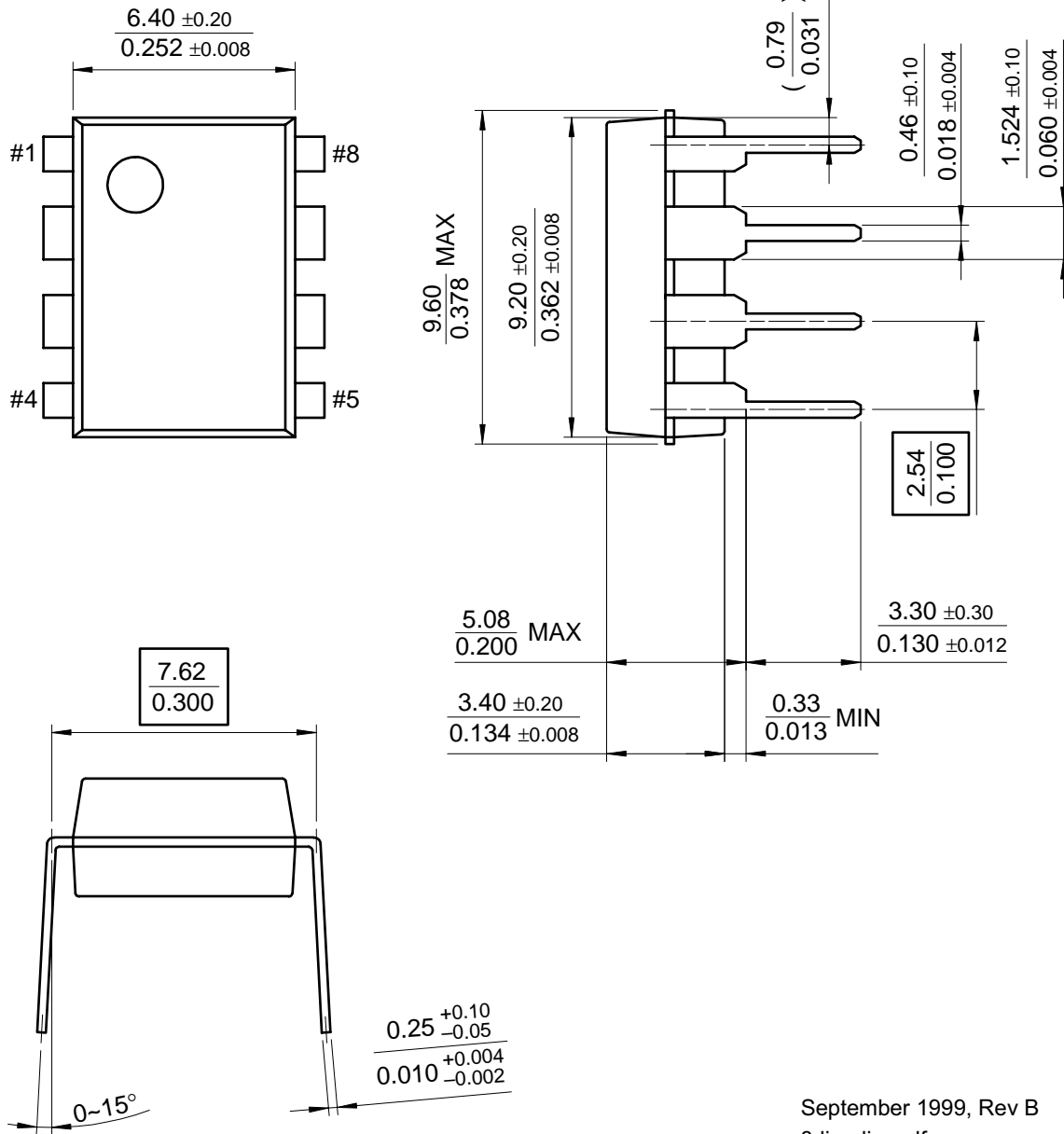
8. Performance Data

| P_{OUT} | | 85V _{AC} | 115V _{AC} | 230V _{AC} | 265V _{AC} |
|-----------|------------|-------------------|--------------------|--------------------|--------------------|
| 100W | PF | 0.998 | 0.998 | 0.991 | 0.984 |
| | THD | 5.1% | 3.6% | 5.2% | 6.2% |
| | Efficiency | 90.9% | 93.7% | 95.6% | 96% |
| 75W | PF | 0.999 | 0.998 | 0.986 | 0.975 |
| | THD | 4.1% | 3.6% | 5.0% | 5.7% |
| | Efficiency | 91.6% | 93.3% | 94.6% | 95.3% |
| 50W | PF | 0.998 | 0.997 | 0.974 | 0.956 |
| | THD | 4.4% | 5.0% | 5.7% | 6.2% |
| | Efficiency | 91.3% | 91.9% | 92.7% | 93.4% |
| 25W | PF | 0.995 | 0.991 | 0.923 | 0.876 |
| | THD | 7.9% | 8.6% | 8.3% | 8.7% |
| | Efficiency | 86.4% | 87.1% | 87.3% | 88.1% |

Mechanical Dimensions

8-DIP

Dimensions are in millimeters (inches) unless otherwise noted.

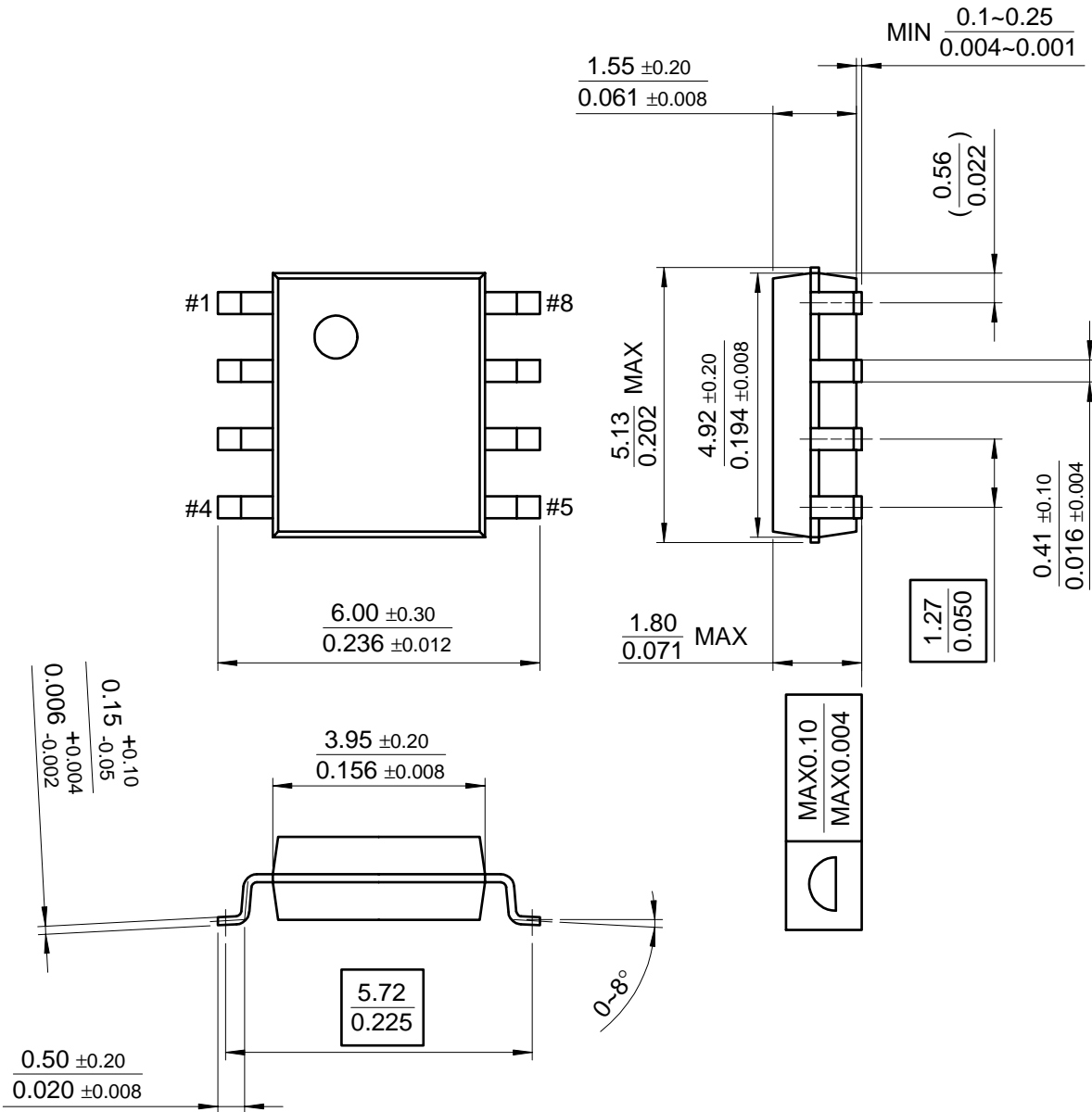


September 1999, Rev B
8dip_dim.pdf

Mechanical Dimensions (Continued)

8-SOP

Dimensions are in millimeters (inches) unless otherwise noted.



September 2001, Rev B1
sop8_dim.pdf

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