



Not Recommended for New Designs

Use MCP2515 or MCP25625

MCP2502X/5X

CAN I/O Expander Family

Features

- Implements CAN V2.0B
 - Programmable bit rate up to 1 Mb/s
 - One programmable mask
 - Two programmable filters
 - Three auto-transmit buffers
 - Two message reception buffers
 - Does not require synchronization or configuration messages
- Hardware Features
 - Non-volatile memory for user configuration
 - User configuration automatically loaded on Power-up
 - Eight general-purpose I/O lines individually selectable as inputs or outputs
 - Individually selectable transmit-on-pin-change for each input
 - Four 10-bit, analog input channels with programmable conversion clock and VREF sources (MCP2505X devices only)
 - Message scheduling capability
 - Two 10-bit PWM outputs with independently programmable frequencies
 - Device configuration can be modified via CAN bus messages
 - In-Circuit Serial Programming™ (ICSP™) of default Configuration memory
 - Optional 1-wire CAN bus operation
- Low-power CMOS technology
 - Operates from 2.7V to 5.5V
 - 10 mA active current, typical
 - 30 µA standby current (CAN Sleep mode)
- 14-pin PDIP (300 mil) and SOIC (150 mil) packages
- Available temperature ranges:
 - Industrial (I): -40°C to +85°C
 - Extended (E): -40°C to +125°C

Description

The MCP2502X/5X devices operate as I/O expanders for a Controller Area Network (CAN) system, supporting CAN v2.0B active, with bus rates up to 1 Mb/s. The MCP2502X/5X allows a simple CAN node to be implemented without the need for a microcontroller.

The devices are identical, with the following exceptions:

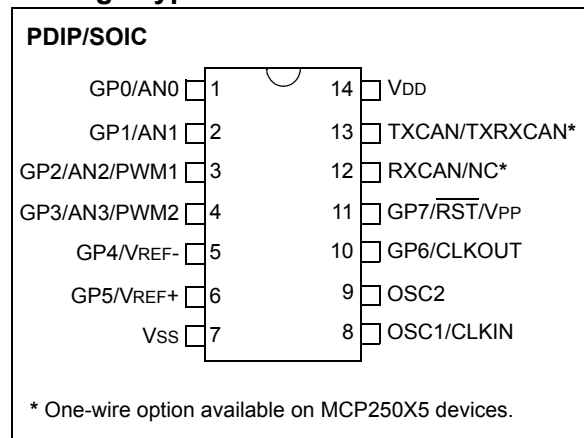
| Device | A/D | One Wire Digital CANbus |
|----------|-----|-------------------------|
| MCP25020 | No | No |
| MCP25025 | No | Yes |
| MCP25050 | Yes | No |
| MCP25055 | Yes | Yes |

The MCP2502X/5X devices feature a number of peripherals, including digital I/Os, four-channel 10-bit A/D (MCP2505X), and PWM outputs with automatic message transmission on change-of-input state. This includes an analog input exceeding a preset threshold.

One mask and two acceptance filters are provided to give maximum flexibility during system design with respect to identifiers that the device will respond to. The device can also be configured to automatically transmit a unique message whenever any of several error conditions occur.

The device is pre-programmed in non-volatile memory so that the part defaults to a specific configuration at Power-up.

Package Types



MCP2502X/5X

Definition of Terms

The following terms are used throughout this document:

I/O Expander – refers to the integrated circuit (IC) device being described (MCP2502X/5X).

Input Message – term given to messages that are received by the MCP2502X/5X and cause the internal registers to be modified. Once the register modification has been performed, the MCP2502X/5X transmits a Command Acknowledge message to indicate that the command was received and processed.

Command Acknowledge Message – term given to the message that is automatically transmitted by the MCP2502X/5X after receiving and processing an input message.

Information Request Message – term given to the Remote Request messages that are received by the MCP2502X/5X that subsequently generate an output message (data frame) in response.

Output Message – term given to the message that the MCP2502X/5X sends in response to an Information Request message.

On Bus Message – term given to the message that the MCP2502X/5X transmits after completing the Power-On and/or Self-Configuration sequences at timed intervals, if enabled.

Self-Configuration – term used to describe the process of transferring the contents of the EPROM memory array to the SRAM memory array.

On Bus – term used to describe the condition when the MCP2502X/5X is fully-configured and ready to transmit or receive on the bus. This is the only state in which the MCP2502X/5X can transmit on the bus.

Edge Detection – refers to the MCP2502X/5X's ability to automatically transmit a message based on the occurrence of a predefined edge on any digital input.

Threshold Detection – refers to the MCP2502X/5X's ability to automatically transmit a message when a predefined analog threshold is reached.

1.0 DEVICE OVERVIEW

This document contains device-specific information on the MCP2502X/5X family of CAN I/O expanders. The CAN protocol is not discussed in depth in this document. Additional information on the CAN protocol can be found in the CAN specification, as defined by Robert Bosch GmbH.

Figure 1-1 is the block diagram of the MCP2502X/5X and Table 1-1 is the pinout description.

FIGURE 1-1: MCP2502X/5X BLOCK DIAGRAM

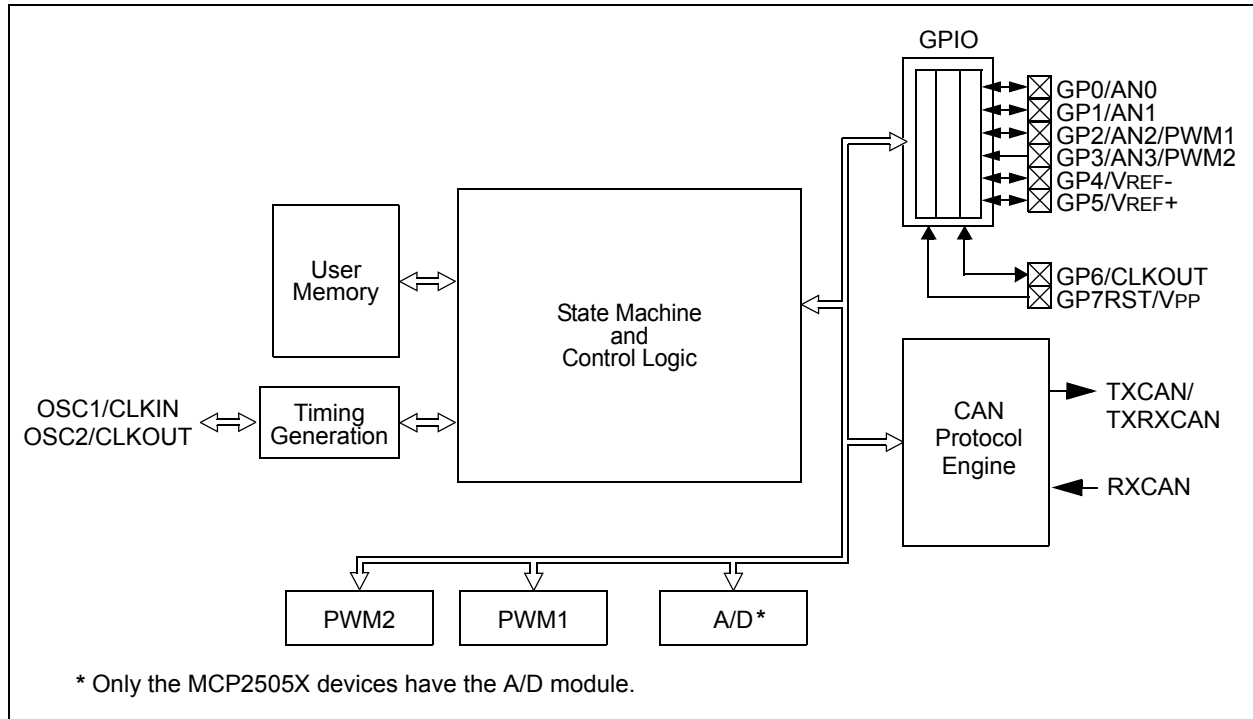


TABLE 1-1: PINOUT DESCRIPTION

| Pin Name | Pin Number | Standard Function | Alternate Function | Programming Mode Function |
|----------------|------------|---|---|---------------------------|
| GP0/AN0 * | 1 | Bidirectional I/O pin, TTL input buffer | Analog input channel | None |
| GP1/AN1 * | 2 | Bidirectional I/O pin, TTL input buffer | Analog input channel | None |
| GP2/AN2/PWM2 * | 3 | Bidirectional I/O pin, TTL input buffer | Analog input/PWM output | None |
| GP3/AN3/PWM3 * | 4 | Bidirectional I/O pin, TTL input buffer | Analog input/PWM output | None |
| GP4/VREF- | 5 | Bidirectional I/O pin, TTL input buffer | External VREF- | Data |
| GP5/VREF+ | 6 | Bidirectional I/O pin, TTL input buffer | External VREF+ input | Clock |
| Vss | 7 | Ground | None | Ground |
| OSC1/CLKIN | 8 | External oscillator input | External clock input | None |
| OSC2 | 9 | External oscillator output | None | None |
| GP6/CLKOUT | 10 | Bidirectional I/O pin, TTL input buffer | CLKOUT output | None |
| GP7RST/VPP | 11 | Input pin, TTL input buffer | External Reset input | VPP |
| RXCAN | 12 | CAN data receive input | Not connected for 1-wire operation | None |
| TXCAN/TXRXCAN | 13 | CAN data transmit output | CAN TX and RX for 1-wire operation (MCP250X5) | None |
| VDD | 14 | Power | None | Power |

* Only the MCP2505X devices have the A/D module.

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NOTES:

2.0 CAN MODULE

The CAN module is a protocol controller that converts between raw digital data and CAN message packets. The main functional block of the CAN module is shown in [Figure 2-1](#) and consists of:

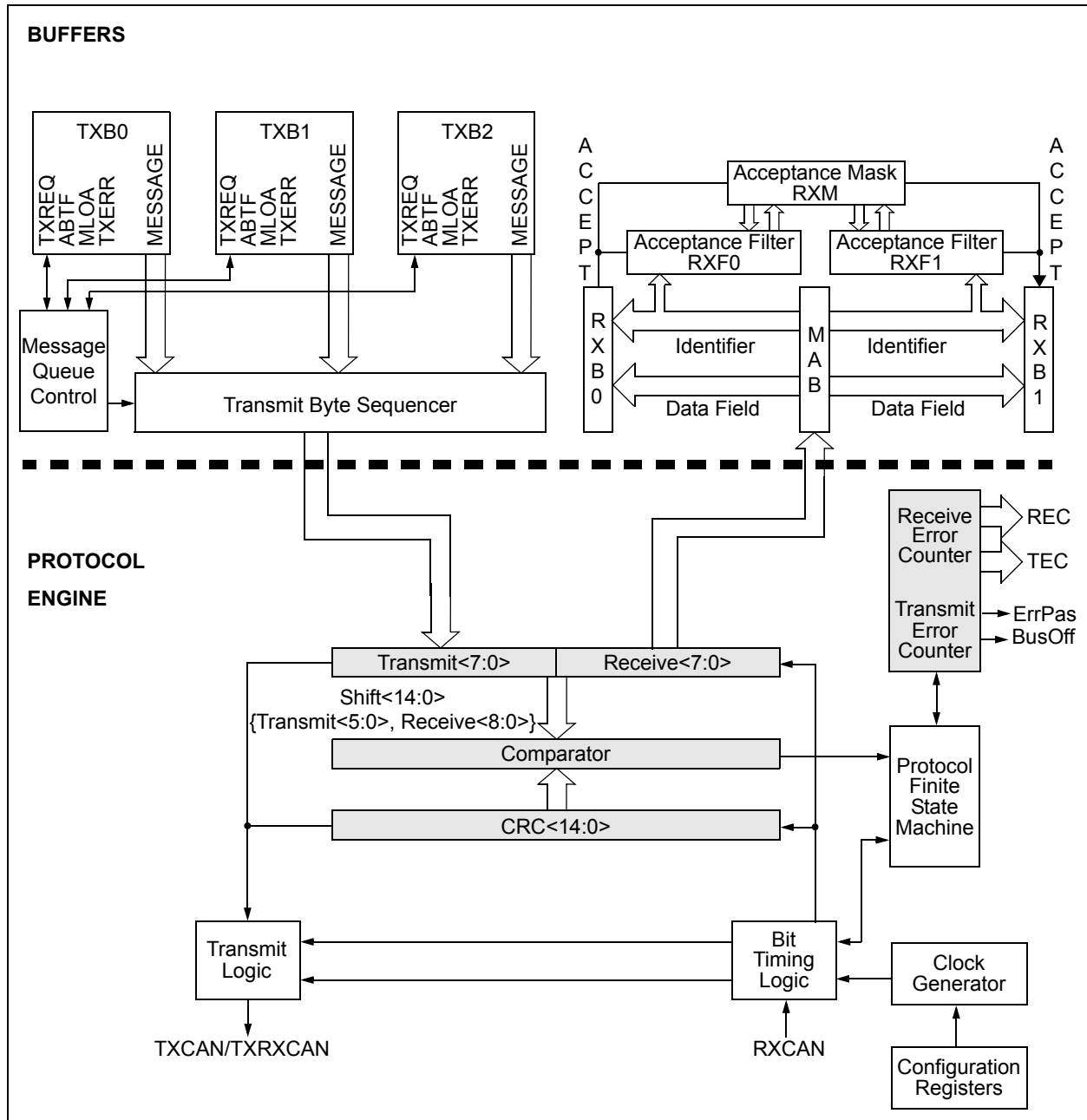
- CAN protocol engine
- Buffers, masks and filters

The module features include:

- Implementation of the CAN protocol
- Double-buffered receiver with two separate receive buffers

- One full-acceptance mask (standard and extended)
- Two full-acceptance filters (standard and extended)
- One filter for each receive buffer
- Three prioritized transmit buffers for transmitting predefined message types
- Automatic wake-up on bus traffic function
- Error management logic for transmit and receive error states
- Low-power SLEEP mode

FIGURE 2-1: CAN MODULE



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2.1 CAN Protocol Finite State Machine

The heart of the engine is the Finite State Machine (FSM). This state machine sequences through messages on a bit-by-bit basis, changing states as the fields of the various frame types are transmitted or received. The FSM is a sequencer controlling the sequential data stream between the TX/RX Shift register, the CRC register and the bus line. The FSM also controls the Error Management Logic (EML) and the parallel data stream between the TX/RX Shift registers and the buffers. The FSM ensures that the processes of reception, arbitration, transmission and error signaling are performed according to the CAN protocol. The automatic retransmission of messages on the bus line is also handled.

2.2 Cyclic Redundancy Check (CRC)

The CRC register generates the CRC code that is transmitted after either the Control field (for messages with 0 data bytes) or the Data field, and is used to check the CRC field of incoming messages.

2.3 Error Management Logic

The error management logic is responsible for the fault confinement of the CAN device. Its two counters, the Receive Error Counter (REC) and the Transmit Error Counter (TEC), are incremented and decremented by commands from the bit stream processor. According to the values of the error counters, the MCP2502X/5X is set into one of the following states: Error-Active, Error-Passive, or Bus-Off.

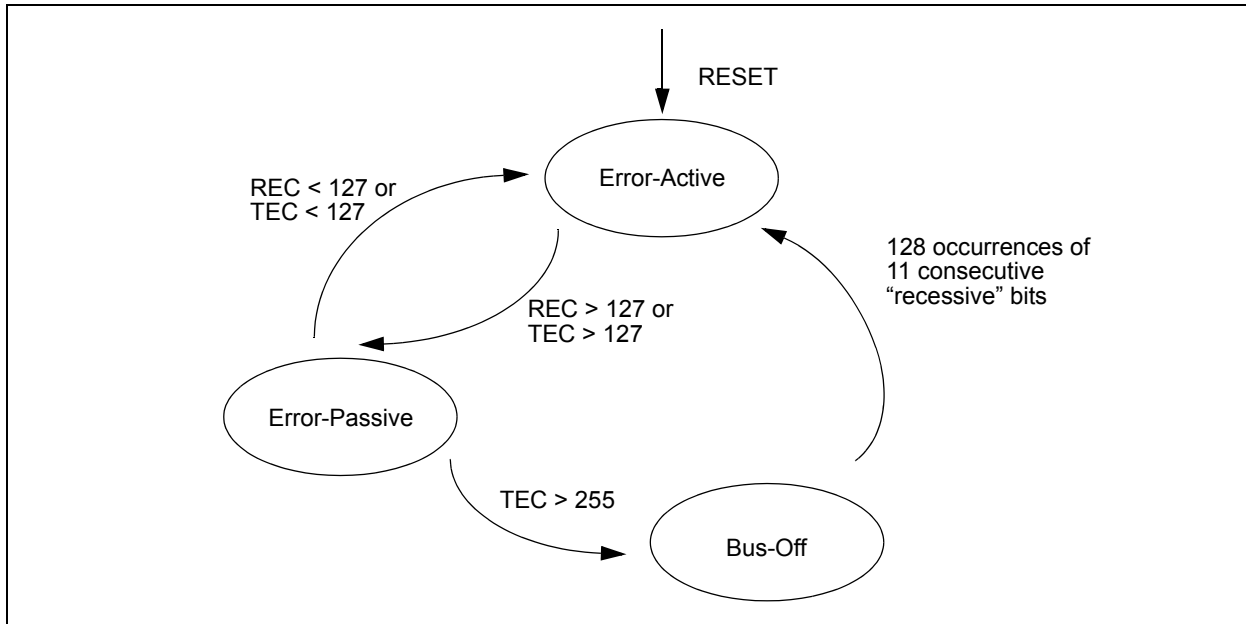
Error-Active: both error counters are below the error-passive limit of 128.

Error-Passive: at least one of the error counters (TEC or REC) equals or exceeds 128.

Bus-Off: the transmit error counter (TEC) equals or exceeds the bus-off limit of 256. The device remains in this state until the bus-off recovery sequence is received. The bus-off recovery sequence consists of 128 occurrences of 11 consecutive recessive bits.

Note: The MCP2502X/5X, after going bus-off, will recover to error-active automatically if the bus remains idle for 128 x 11 bits. OPTREG2.ERRE must be set to force the MCP2502X/5X to enter Listen-Only mode, instead of Normal mode, during bus recovery. The current error mode (except for bus-off) of the MCP2502X/5X can be determined by reading the EFLG register via the Read CAN error message.

FIGURE 2-2: ERROR MODES STATE DIAGRAM



REGISTER 2-1: TEC - TRANSMITTER ERROR COUNTER

| | | | | | | | |
|-------|------|------|------|-------|------|------|------|
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| TEC7 | TEC6 | TEC5 | TEC4 | TEC3 | TEC2 | TEC1 | TEC0 |
| bit 7 | | | | bit 0 | | | |

bit 7-0 **TEC7:TEC0:** Transmit Error Counter bits

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 2-2: REC - RECEIVER ERROR COUNTER

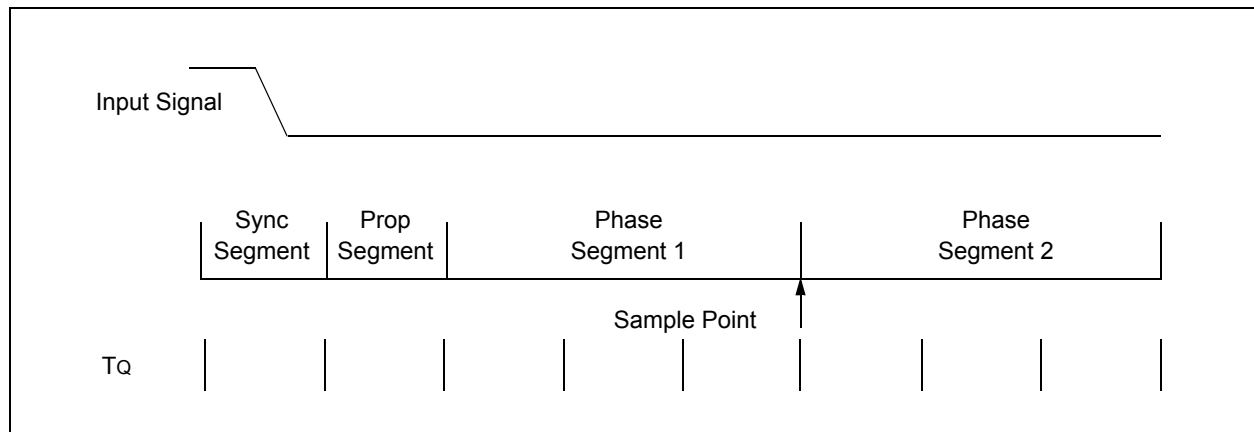
| | | | | | | | |
|-------|------|------|------|-------|------|------|------|
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| REC7 | REC6 | REC5 | REC4 | REC3 | REC2 | REC1 | REC0 |
| bit 7 | | | | bit 0 | | | |

bit 7-0 **REC7:REC0:** Receive Error Counter bits

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

FIGURE 2-3: BIT TIME PARTITIONING



2.4 Bit Timing Logic

The Bit Timing Logic (BTL) monitors the bus line input and handles the bus-related bit timing, based on the CAN protocol. The BTL synchronizes on a recessive-to-dominant bus transition at Start-of-Frame (hard synchronization) and on any further recessive-to-dominant bus line transition if the CAN controller itself does not transmit a dominant bit (resynchronization). The BTL also provides programmable time segments to compensate for the propagation delay time, phase shifts, and to define the position of the sample point within the bit time. These programmable segments are made up of integer units called Time Quanta (T_Q).

The nominal bit time is calculated by programming the T_Q length and the number of T_Q in each time segment, as discussed below.

2.4.1 TIME QUANTUM (T_Q)

T_Q is a fixed unit of time derived from the oscillator period. There is a programmable baud rate prescaler (BRP) (with integral values ranging from 1 to 64), as well as a fixed division by two for clock generation.

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The base T_Q is defined as twice the oscillator period. Adding the BRP into the equation yields:

$$T_Q = 2 * T_{OSC} * (BRP + 1)$$

where BRP = binary value represented by CNF1.BRP<5:0>

By definition, the nominal bit time is programmable from a minimum of 8 T_Q to 25 T_Q . Also, the minimum nominal bit time is 1 μ s, which corresponds to 1 Mbps.

2.4.2 TIME SEGMENTS

Time segments make up the nominal bit time. The nominal bit time can be thought of as being divided into separate non-overlapping time segments. These segments are shown in [Figure 2-3](#).

- Synchronization Segment (SyncSeg)
- Propagation Segment (PropSeg)
- Phase Buffer Segment 1 (PS1)
- Phase Buffer Segment 2 (PS2)

$$\text{Nominal Bit Time} = T_Q * (\text{Sync_Seg} + \text{PropSeg} + \text{Phase_Seg1} + \text{Phase_Seg2})$$

Rules for Programming the Segments

There are a few rules to follow when programming the time segments:

- PropSeg + PS1 \geq PS2
- PS2 > Sync Jump Width
- PS2 \geq Information Processing Time

2.4.2.1 Synchronization Segment

The Synchronization Segment (SyncSeg) of the bit time is used to synchronize the various CAN nodes on the bus. The edge of the input signal is expected to occur during the SyncSeg. The duration is fixed at 1 T_Q .

2.4.2.2 Propagation Segment

This part of the bit time is used to compensate for physical delay times within the network. These delay times consist of the signal propagation time on the bus line and the internal delay time of the nodes. The delay is calculated as being the round-trip time from transmitter to receiver (twice the signal's propagation time on the bus line), the input comparator delay and the output driver delay. The length of the Propagation Segment can be programmed from 1 T_Q to 8 T_Q by setting the PRSEG2:PRSEG0 bits of the CNF2 register.

2.4.2.3 Phase Buffer Segments

The Phase Buffer Segments are used to optimally locate the sampling point of the received bit within the nominal bit time. The sampling point occurs between PS1 and PS2. These segments can be automatically lengthened or shortened by the resynchronization process. Thus, the variation of the values of the phase buffer segments represent the DPLL functionality.

PS1: the end of PS1 determines the sampling point within a bit time. PS1 is programmable from 1 T_Q to 8 T_Q in duration.

PS2: PS2 provides delay before the next transmitted data transition and is also programmable from 1 T_Q to 8 T_Q in duration. However, due to Information Processing Time (IPT) requirements, the actual minimum length of PS2 is 2 T_Q . It can also be defined as equal to the greater of PS1 or the IPT.

2.4.3 SAMPLE POINT

The sample point is the point of time at which the bus level is read and the value of the received bit is determined. The sampling point occurs at the end of PS1. If desired, it is possible to specify multiple sampling of the bus line at the sample point. The value of the received bit is determined to be the value of the majority decision of three values. The three samples are taken at the sample point, and twice before, with a time of $T_Q/2$ between each sample.

2.4.4 INFORMATION PROCESSING TIME

IPT is the time segment (starting at the sample point) that is reserved for calculation of the subsequent bit level. The CAN specification defines this time to be less than or equal to 2 T_Q . The MCP2502X/5X defines this time to be 2 T_Q . Thus, PS2 must be at least 2 T_Q long.

2.4.5 SYNCHRONIZATION JUMP WIDTH (SJW)

To compensate for phase shifts and oscillator tolerances between the nodes in the system, each CAN controller must be able to synchronize to the relevant signal edge of the incoming signal. When a recessive-to-dominant edge in the transmitted data is detected, the logic will compare the location of the edge to the expected time (SyncSeg). The circuit will then adjust the values of PS1 and PS2, as necessary, using the programmed SJW. This adjustment is made for resynchronization during a message and not hard synchronization, which occurs only at the message Start-of-Frame (SOF).

As a result of resynchronization, PS1 may be lengthened or PS2 may be shortened. The amount of lengthening or shortening of the phase buffer segments has an upper-boundary given by the SJW. The SJW is programmable between 1 T_Q and 4 T_Q. The value of the SJW will be added to PS1 (or subtracted from PS2) depending on the phase error (e) of the edge in relation to the receiver's SyncSeg. The phase error is defined as follows:

- e = 0 if the edge lies within SYNCSESEG
No resynchronization is required.
- e > 0 if the edge lies before the sample point
PS1 will be lengthened by the amount of the SJW.
- e < 0 if the edge lies after the sample point of the previous bit and before the SyncSeg of the current bit
PS2 will be shortened by the amount of the SJW.

2.4.6 CONFIGURATION REGISTERS

There are three registers (in the Configuration register module) associated with the CAN bit timing logic that controls the bit timing for the CAN bus interface.

2.4.6.1 CNF1

The BRP<5:0> bits control the baud rate prescaler. These bits set the length of T_Q relative to the OSC1 input frequency, with the minimum length of T_Q being 2 T_{osc} in length (when BRP<5:0> are set to 000000). The SJW<1:0> bits select the synchronization jump width in terms of number of T_Q's.

2.4.6.2 CNF2

The PRSEG<2:0> bits set the length (in T_Q's) of the propagation segment. The PS1<2:0> bits set the length (in T_Q's) of phase segment 1. The SAM bit controls how many times the RXCAN pin is sampled. Setting this bit to a '1' causes the bus to be sampled three times. Twice at T_Q/2 before the sample point and once at the normal sample point (which is at the end of PS1). The value of the bus is determined to be the value read during at least two of the samples. If the SAM bit is set to a '0', the RXCAN pin is sampled only once at the sample point. The BTLMODE bit controls how the length of PS2 is determined. If this bit is set to a '1', the length of PS2 is determined by the PS2<2:0> bits of CNF3. If the BTLMODE bit is set to a '0', then the length of PS2 is the greater of PS1 and the information processing time (which is fixed at 2 T_Q for the MCP2502X/5X).

2.4.6.3 CNF3

The PS2<2:0> bits set the length, in T_Q's, of PS2, if the CNF2.BTLMODE bit is set to a '1'. If the BTLMODE bit is set to a '0', the PS2<2:0> bits have no effect.

Additionally, the wake-up filter (CNF3.WAKFIL) is implemented in the CNF3 register. This filter is a low-pass filter that can be used to prevent the MCP2502X/5X from waking up due to short glitches on the CAN bus.

REGISTER 2-3: CNF1 - CAN CONFIGURATION REGISTER 1

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| SJW1 | SJW0 | BRP5 | BRP4 | BRP3 | BRP2 | BRP1 | BRP0 |
| bit 7 | | | | | | | bit 0 |

bit 7-6 **SJW1:SJW0:** Synchronized Jump Width bits

11 = Length = 4 x T_Q
 10 = Length = 3 x T_Q
 01 = Length = 2 x T_Q
 00 = Length = 1 x T_Q

bit 5-0 **BRP5:BRP0:** Baud Rate Prescaler bits

111111 = T_Q = 64 x 1/Fosc
 -
 -
 000000 = T_Q = 64 x 1/Fosc

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

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REGISTER 2-4: CNF2 - CAN CONFIGURATION REGISTER 2

| | | | | | | | | |
|---------|-------|---------|---------|---------|--------|--------|--------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | |
| BTLMODE | SAM | PHSEG12 | PHSEG11 | PHSEG10 | PRSEG2 | PRSEG1 | PRSEG0 | |
| bit 7 | | | | | | | | bit 0 |

- bit 7 **BTL MODE:** Length determination of PHSEG2 bit
 1 = Length of Phase_Seg2 determined by bits 2:0 of CNF3
 0 = Length of Phase_Seg2 is the greater of Phase_Seg1 or IPT(2T_Q)
- bit 6 **SAM:** Sample of the CAN bus line bit
 1 = Bus line is sampled three times at the sample point
 0 = Bus line is sampled once at the sample point
- bit 5-3 **PHSEG12:PHSEG10:** Phase Buffer Segment1 bits
 111 = Length = 8 x T_Q
 -
 -
 -
 000 = Length = 1 x T_Q
- bit 2-0 **PRSEG2:PRSEG0:** Propagation Time Segment bits
 111 = Length = 8 x T_Q
 -
 -
 -
 000 = Length = 1 x T_Q

| | | | |
|--------------------|------------------|------------------------------------|--------------------|
| Legend: | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

REGISTER 2-5: CNF3 - CAN CONFIGURATION REGISTER 3

| | | | | | | | | |
|-------|--------|-----|-----|-----|---------|---------|---------|-------|
| U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | |
| — | WAKFIL | — | — | — | PHSEG22 | PHSEG21 | PHSEG20 | |
| bit 7 | | | | | | | | bit 0 |

- bit 7 **Unimplemented:** (Reads as 0)
- bit 6 **WAKFIL:** Wake-up filter bit
 1 = Wake-up filter enabled
 0 = Wake-up filter disabled
- bit 5-3 **Unimplemented:** (Reads as 0)
- bit 2-0 **PHSEG22:PHSEG20:** Phase Buffer Segment2 bits
 111 = Length = 8 x T_Q
 -
 -
 -
 001 = Length = 2 x T_Q
 000 = Invalid

| | | | |
|--------------------|------------------|------------------------------------|--------------------|
| Legend: | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

2.5 Buffers, Masks, and Filters

This part of the CAN module supports the transmitting, receiving and acceptance of CAN messages.

Three transmit buffers are used for the three transmit message IDs, as discussed later in this section. Two receive buffers store the CAN message's arbitration field, control field and the data field.

One mask defines which bits are to be applied to either filter. The mask can be regarded as defining "don't care" bits for the filter.

Each of the two filters define a bit pattern that will be compared to all incoming messages. All filter bits that have not been defined as "don't care" by the mask are applied to the message.

2.5.1 TRANSMIT MESSAGE IDs

The MCP2502X/5X device contains three separate transmit message IDs: TXID0, TXID1 and TXID2. The data length code is predefined for each of the various output messages, with the data that is transmitted coming directly from the contents of the device's peripheral registers.

2.5.1.1 Transmit Message ID0 (TXID0)

TXID0 contains the identifier that is used when transmitting the On Bus message. If enabled (STCON.STEN = 1), the On Bus message will be transmitted at predefined intervals. Depending on the message-select bit (STCON.STMS = 1), the CAN message will send GPIO and A/D data.

Transmit Message ID0 will not be sent automatically when the device is brought out of sleep.

2.5.1.2 Transmit Message ID1 (TXID1)

TXID1 contains the identifier that is used when the MCP2502X/5X sends the Command Acknowledge message, the Receive Overflow message and/or the Error Condition message. All message types use the same identifier.

The CAEN bit, in the OPTREG2 register, selects between the Command Acknowledge and Receive Overflow operation. These message types have a DLC of 0 and do not contain any data. The Error Condition message can occur anytime, has a DLC of 3 and contains the EFLG, TEC and REC data values.

Note: A zero-data-length On Bus message will be transmitted once after Power-up, regardless of the scheduled transmission-enable status.

Command Acknowledge: TXID1 sends a Command Acknowledge message when the MCP2502X/5X receives an Input Message and processes the instruction (and OPTREG2.CAEN = 1). This message is used as a hand shake for the node requesting the modification of the MCP2502X/5X. There is no data associated with this message.

Receive Overflow: TXID1 sends a Receive Overflow message if there is a Receive Overflow condition (and OPTREG2.CAEN = 0). This only occurs if the device has received a valid message before processing the previous valid message from the same receive buffer. There is no data associated with this message.

Error Condition: An Error Condition message is transmitted if the TEC or REC counters reach error warning (> 95) or error passive (> 127). This message contains the TXID1 identifier and the TEC, REC and EFLG counters.

A hysteresis is implemented in hardware that prevents messages from repeatedly being transmitted due to error counts changing by one or two bits. When a message is sent for an error warning (TEC or REC > 95), the message will not trigger again until the error counter ≤ 79 and back to > 95 (hysteresis = 17 counts). Similarly, an error passive message is sent at TEC or REC > 127 and is not sent again until the error counter ≤ 111 and back to >127 (hysteresis = 17 counts).

2.5.1.3 Transmit Message ID2 (TXID2)

Transmit ID2 contains the identifier that is used when transmitting auto-conversion-initiated messages, including digital input edge detection and/or analog input exceeding a threshold. This message will also be sent when the device wakes up from sleep due to a digital input change-of-state condition (i.e., change-of-state occurs on input configured to transmit on change-of-state).

2.6 Receive Buffers

The MCP2505X contains two receive buffers, each with their own filter. There is also a Message Assembly Buffer (MAB) that acts as a third receive buffer (see [Figure 2-1](#)).

The two receive buffers, combined with the MAB help, ensure that received messages will be processed while minimizing the chances of receive buffer overrun due to maximum bus loading of messages destined for the MCP2502X/5X.

Note: The receive buffers are used by the MCP2502X/5X to implement the command messages. They are not externally accessible.

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2.7 Acceptance Mask

The acceptance mask is used to define which bits in the CAN ID are to be compared against the programmable filters. Individual bits within the mask correspond to bits in the CAN ID that, in turn, correspond to bits in the acceptance filters. Any bit in the mask that is set to a '1' will cause the corresponding CAN ID bit to be compared against the associated filter bit. Any bit in the mask that is set to a '0' is not compared and effectively sets the associated CAN ID bit to 'don't care'.

2.7.1 MASKS AND STANDARD/EXTENDED IDS

To insure proper operation of the information request and input messages, some mask bits (as configured in the mask registers) may be ignored as explained:

Message with a standard ID - the three least significant bits of a standard identifier (RXMSIDL.SID2:SID0) are 'don't care' for the mask registers and effectively become '0'.

Message with an extended ID - the three least significant bits of the standard identifier (RXMSIDL.SID2:SID0) are configurable and the three least significant bits of the extended identifier (RXMEID0.EID2:EID0) are always 'don't cares' and effectively becomes '0'.

Note: The EXIDE bit in the Mask register (RXMSIDL) can be used to mask the IDE bit in the corresponding Receive buffer register (RXBnSIDL).

2.8 Acceptance Filters

There are two separate acceptance filters defined for the MCP2502X/5X: RXF0 and RXF1. RXF0 is used for Information Request messages and RXF1 is used for input messages (see [Table 4-2](#) and [Table 4-3](#)). Each bit in the filters corresponds to a bit in the CAN ID. Every bit in the CAN ID, for which the corresponding Mask bit is set, must match the associated filter bit in order for the message to be accepted. Messages that fail to meet the mask/filter criteria are ignored.

REGISTER 2-6: TXIDNSIDH - TRANSMIT IDENTIFIER N STANDARD IDENTIFIER HIGH

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 |

bit 7 bit 0

bit 7-0 **SID10:SID3:** Standard Identifier bits

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
- n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 2-7: TXIDNSIDL - TRANSMIT IDENTIFIER N STANDARD IDENTIFIER LOW

| R/W-x | R/W-x | R/W-x | U-0 | R/W-x | U-0 | R/W-x | R/W-x |
|-------|-------|-------|-----|-------|-----|-------|-------|
| SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 |
| bit 7 | | | | | | bit 0 | |

- bit 7-5 **SID2:SID0**: Standard Identifier bits
- bit 4 **Unimplemented**: Read as '0'
- bit 3 **EXIDE**: Extended Identifier Enable bit
1 = Message will transmit extended identifier
0 = Message will transmit standard identifier
- bit 2 **Unimplemented**: Read as '0'
- bit 1-0 **EID17:EID16**: Extended Identifier bits

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 2-8: TXIDNEID8 - TRANSMIT IDENTIFIER N EXTENDED IDENTIFIER HIGH

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EID15 | EID14 | EID13 | EID12 | EID11 | EID10 | EID9 | EID8 |
| bit 7 | | | | | | bit 0 | |

- bit 7-0 **EID15:EID8**: Extended Identifier bits

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 2-9: TXIDNEID0 - TRANSMIT IDENTIFIER N EXTENDED IDENTIFIER LOW

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EID7 | EID6 | EID5 | EID4 | EID3 | EID2 | EID1 | EID0 |
| bit 7 | | | | | | bit 0 | |

- bit 7-0 **EID7:EID0**: Extended Identifier bits

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

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REGISTER 2-10: RXMSIDH - ACCEPTANCE FILTER MASK STANDARD IDENTIFIER HIGH

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3* | |
| bit 7 | | | | | | | | bit 0 |

bit 7-0 **SID10:SID3:** Standard Identifier bits

* If OPTREG2.MTYPE = 1, then SID3 is forced to zero

| Legend: | | | |
|--------------------|------------------|------------------------------------|--------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

REGISTER 2-11: RXMSIDL - ACCEPTANCE FILTER MASK STANDARD IDENTIFIER LOW

| R/W-x | R/W-x | R/W-x | U-0 | R/W-x | U-0 | R/W-x | R/W-x | |
|-------|-------|-------|-----|-------|-----|-------|-------|-------|
| SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | |
| bit 7 | | | | | | | | bit 0 |

bit 7-5 **SID2:SID0:** Standard Identifier bits
Standard messages, bits = b'000'
Extended messages, bits = SID2:SID0

bit 4 **Unimplemented:** Read as '0'

bit 3 **EXIDE:** Extended Identifier Enable bit
1 = Apply filter to RXFnSIDL.EXIDE (filter applies to standard **or** extended message frames, depending on filter bit)
0 = Do not apply filter to RXFnSIDL.EXIDE (filter will be applied to both standard **and** extended message frames)

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **EID17:EID16:** Extended Identifier bits

| Legend: | | | |
|--------------------|------------------|------------------------------------|--------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

REGISTER 2-12: RXMEID8 - ACCEPTANCE FILTER MASK EXTENDED IDENTIFIER MID

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| EID15 | EID14 | EID13 | EID12 | EID11 | EID10 | EID9 | EID8 | |
| bit 7 | | | | | | | | bit 0 |

bit 7-0 **EID15:EID8:** Extended Identifier bits

| Legend: | | | |
|--------------------|------------------|------------------------------------|--------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

REGISTER 2-13: RXMEID0 - ACCEPTANCE FILTER MASK EXTENDED IDENTIFIER LOW

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EID7 | EID6 | EID5 | EID4 | EID3 | EID2 | EID1 | EID0 |
| bit 7 | | | | bit 0 | | | |

- bit 7-3 **EID7:EID3**: Extended Identifier bits
- bit 2-0 **EID2:EID0**: Extended Identifier bits (always reads as '0')

| | | |
|--------------------|------------------|--|
| Legend: | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

REGISTER 2-14: RXFN SIDH - ACCEPTANCE FILTER N STANDARD IDENTIFIER HIGH

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3* |
| bit 7 | | | | bit 0 | | | |

- bit 7-0 **SID10:SID3**: Standard Identifier bits
- * If OPTREG2.MTYPE = 1, then SID3 = X

| | | |
|--------------------|------------------|--|
| Legend: | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

REGISTER 2-15: RXFN SIDL - ACCEPTANCE FILTER N STANDARD IDENTIFIER LOW

| R/W-x | R/W-x | R/W-x | U-0 | R/W-x | U-0 | R/W-x | R/W-x |
|-------|-------|-------|-----|-------|-----|-------|-------|
| SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 |
| bit 7 | | | | bit 0 | | | |

- bit 7-5 **SID2:SID0**: Standard Identifier bits
 - 1 = When EXIDE = 1, SID2:SID0 = b'xxx'
 - 0 = When EXIDE = 0, SID2:SID0 = as configured
- bit 4 **Unimplemented**: Read as '0'
- bit 3 **EXIDE**: Extended Identifier Enable bit
 - 1 = Filter will apply to extended identifier
 - 0 = Filter will apply to standard identifier
- bit 2 **Unimplemented**: Read as '0'
- bit 1-0 **EID17:EID16**: Extended Identifier bits

| | | |
|--------------------|------------------|--|
| Legend: | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

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REGISTER 2-16: RXFNEID8 - ACCEPTANCE FILTER N EXTENDED IDENTIFIER MID

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EID15 | EID14 | EID13 | EID12 | EID11 | EID10 | EID9 | EID8 |

bit 7 bit 0

bit 7-0 **EID15:EID8:** Extended Identifier bits

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
- n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 2-17: RXFNEID0 - ACCEPTANCE FILTER N EXTENDED IDENTIFIER LOW

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EID7 | EID6 | EID5 | EID4 | EID3 | EID2 | EID1 | EID0 |

bit 7 bit 0

bit 7-0 **EID7:EID0:** Extended Identifier bits (always = b'xxxx')

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
- n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 2-18: EFLG - ERROR FLAG REGISTER

| | | | | | | | |
|-------|-----|------|------|------|-------|-------|-------|
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| ESCF | RBO | TXBO | TXEP | RXEP | TXWAR | RXWAR | EWARN |
| bit 7 | | | | | | | bit 0 |

- bit 7 **ESCF**: Error State Change bit (for sending Error state message)
 1 = An error state change occurred
 0 = No error state change
- bit 6 **RBO**: Receive Buffer Overflow bit
 1 = Overflow occurred
 0 = No overflow occurred
- bit 5 **TXBO**: Transmitter in Bus Off Error State bit
 1 = TEC reaches 256
 0 = Indicates a successful bus recovery sequence
- bit 4 **TXEP**: Transmitter in Error Passive State bit
 1 = TEC is equal to or greater than 128
 0 = TEC is less than 128
- bit 3 **RXEP**: Receiver in Error Passive State bit
 1 = REC is equal to or greater than 128
 0 = REC is less than 128
- bit 2 **TXWAR**: Transmitter in Error Warning State bit
 1 = TEC is equal to or greater than 96
 0 = TEC is less than 96
- bit 1 **RXWAR**: Receiver in Error Warning State bit
 1 = REC is equal to or greater than 96
 0 = REC is less than 96
- bit 0 **EWARN**: Either the Receive Error counter or Transmit Error counter has reached or exceeded 96 errors
 1 = TEC or REC is equal to or greater than 96 (TXWAR or RXWAR = 1)
 0 = Both REC and TEC are less than 96

Legend:

| | | |
|--------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

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NOTES:

3.0 USER REGISTERS

3.1 Description

The MCP2502X/5X allows the user to pre-program registers pertaining to CAN module and device configuration into non-volatile EPROM memory. In this way, the device is initialized to a default state after Power-up. The user registers are transferred to SRAM during the Power-up sequence. Many of the registers are able to be accessed via the CAN bus, once the device establishes a connection with the bus. Additionally, there are 16 user-defined registers that can be used to store information about the part (e.g., serial number, node identifier, etc.). The registers are summarized in [Table 3-1](#).

Note 1: When transferred to RAM, the register addresses are offset by 1Ch. Accessing individual registers using the “Write Register” or “Read Register command requires use of the offset address. Also, see [Table 3-2](#) for information on accessible registers not contained in user EPROM.

2: Do not address locations outside of the user memory map or unexpected results may occur.

TABLE 3-1: USER MEMORY MAP

| Address | Name | Description | Address | Name | Description |
|---------|-------------------|---|---------|-----------|---|
| 00h | IOINTEN | Enable inputs for Transmit-On-Change feature | 1Bh | RXF0EID0 | Acceptance Filter 0, Extended ID LSB |
| 01h | IOINTPO | Defines polarity for I/O, or greater-than/less-than operator for A/D Transmit-On-Change inputs | 1Ch | RXF1SIDH | Acceptance Filter 1, Standard ID MSB |
| 02h | GPLAT | General Purpose I/O (GPIO) Register | 1Dh | RXF1SIDL | Acceptance Filter 1, Standard ID LSB, Extended ID USB, Extended ID enable |
| 03h | 0xFF | Reserved | 1Eh | RXF1EID8 | Acceptance Filter 1, Extended ID MSB |
| 04h | OPTREG1 | Configuration options, including GPIO pull-up enable, clockout enable and prescaler | 1Fh | RXF1EID0 | Acceptance Filter 1, Extended ID LSB |
| 05h | T1CON | PWM1 Timer Control Register; contains enable bit, clock prescale and DC LSBs | 20h | TXID0SIDH | Transmit Buffer 0, Standard ID MSB |
| 06h | T2CON | PWM2 Timer Control Register; contains enable bits, clock prescale and DC LSBs | 21h | TXID0SIDL | Transmit Buffer 0, Standard ID LSB, Extended ID USB, Extended ID enable |
| 07h | PR1 | PWM1 Period Register | 22h | TXID0EID8 | Transmit Buffer 0, Extended ID MSB |
| 08h | PR2 | PWM2 Period Register | 23h | TXID0EID0 | Transmit Buffer 0, Extended ID LSB |
| 09h | PWM1DCH | PWM1 Duty Cycle (DC) MSBs | 24h | TXID1SIDH | Transmit Buffer 1, Standard ID MSB |
| 0Ah | PWM2DCH | PWM2 Duty Cycle (DC) MSBs | 25h | TXID1SIDL | Transmit Buffer 1, Standard ID LSB, Extended ID USB, Extended ID enable |
| 0Bh | CNF1 ³ | CAN module register configures synchronization jump width and baud rate prescaler | 26h | TXID1EID8 | Transmit Buffer 1, Extended ID MSB |
| 0Ch | CNF2 ³ | CAN module register configures propagation segment, phase segment 1, and determines number of sample points | 27h | TXID1EID0 | Transmit Buffer 1, Extended ID LSB |

Note 1: GPDDR is mapped to 1Fh is SRAM and not offset by 1Ch.

2: User memory (35h–44h) is not transferred to RAM on Power-up and can only be accessed via “Read User Mem” commands.

3: Cannot be modified from initial programmed values.

4: Unimplemented on MCP2502X devices and read 0x00 (exception, ADCON1 = 0x0F).

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TABLE 3-1: USER MEMORY MAP (CONTINUED)

| Address | Name | Description | Address | Name | Description |
|---------|---------------------|--|---------|------------------------|---|
| 0Dh | CNF3 ³ | CAN module register configures phase buffer segment 2, Sleep mode | 28h | TXID2SIDH | Transmit Buffer 2, Standard ID MSB |
| 0Eh | ADCON0 ⁴ | A/D Control Register; contains enable, conversion rate, channel select bits | 29h | TXID2SIDL | Transmit Buffer 2, Standard ID LSB, Extended ID USB, Extended ID enable |
| 0Fh | ADCON1 ⁴ | A/D Control Register; contains voltage reference source, conversion rate and A/D input enable bits | 2Ah | TXID2EID8 | Transmit Buffer 2, Extended ID MSB |
| 10h | STCON | Scheduled Transmission Control Register | 2Bh | TXID2EID0 | Transmit Buffer 2, Extended ID LSB |
| 11h | OPTREG2 | Configuration options, including Sleep mode, RTR message and error recovery enables | 2Ch | ADCMP3H ⁴ | Analog Channel 3 Compare Value MSB |
| 12h | — | Reserved | 2Dh | ADCMP3L ⁴ | Analog Channel 3 Compare Value LSb's |
| 13h | — | Reserved | 2Eh | ADCMP2H ⁴ | Analog Channel 2 Compare Value MSB |
| 14h | RXMSIDH | Acceptance Filter Mask, Standard ID MSB | 2Fh | ADCMP2L ⁴ | Analog Channel 2 Compare Value LSb's |
| 15h | RXMSIDL | Acceptance Filter Mask, Standard ID LSB, Extended ID USB | 30h | ADCMP1H ⁴ | Analog Channel 1 Compare Value MSB |
| 16h | RXMEID8 | Acceptance Filter Mask, Extended ID MSB | 31h | ADCMP1L ⁴ | Analog Channel 1 Compare Value LSb's |
| 17h | RXMEID0 | Acceptance Filter Mask, Extended ID LSB | 32h | ADCMP0H ⁴ | Analog Channel 0 Compare Value MSB |
| 18h | RXF0SIDH | Acceptance Filter 0, Standard ID MSB | 33h | ADCMP0L ⁴ | Analog Channel 0 Compare Value LSb's |
| 19h | RXF0SIDL | Acceptance Filter 0, Standard ID LSB, Extended ID USB, Extended ID enable | 34h | GPDDR ¹ | General Purpose I/O Data Direction Register |
| 1Ah | RXF0EID8 | Acceptance Filter 0, Extended ID MSB | 35-44h | USER[0:F] ² | User Defined Bytes (0-15) |

- Note 1:** GPDDR is mapped to 1Fh in SRAM and not offset by 1Ch.
Note 2: User memory (35h-44h) is not transferred to RAM on Power-up and can only be accessed via "Read User Mem" commands.
Note 3: Cannot be modified from initial programmed values.
Note 4: Unimplemented on MCP2502X devices and read 0x00 (exception, ADCON1 = 0x0F).

TABLE 3-2: ACCESSIBLE RAM REGISTERS NOT IN THE EPROM MAP

| Addr* | Name | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Value on POR | Value on RST |
|-------|---------|-------------------------|-------|-------|-------|-------|-------|-------|-------|--------------|--------------|
| 1Fh** | GPDDR | — | DDR6 | DDR4 | DDR4 | DDR3 | DDR2 | DDR1 | DDR0 | -111 1111 | -111 1111 |
| 18h | EFLG | ESCF | RBO | TXEP | TXEP | RXEP | TXWAR | RXWAR | EWARN | 0000 0000 | 0000 0000 |
| 19h | TEC | Transmit Error Counters | | | | | | | | 0000 0000 | 0000 0000 |
| 1Ah | REC | Receive Error Counters | | | | | | | | 0000 0000 | 0000 0000 |
| 50h | ADRES3H | AN3.9 | AN3.8 | AN3.6 | AN3.6 | AN3.5 | AN3.4 | AN3.3 | AN3.2 | xxxx xxxx | uuuu uuuu |
| 51h | ADRES3L | AN3.1 | AN3.0 | — | — | — | — | — | — | xx-- ---- | uu-- ---- |
| 52h | ADRES2H | AN2.9 | AN2.8 | AN2.6 | AN2.6 | AN2.5 | AN2.4 | AN2.3 | AN2.2 | xxxx xxxx | uuuu uuuu |
| 53h | ADRES2L | AN2.1 | AN2.0 | — | — | — | — | — | — | xx-- ---- | uu-- ---- |
| 54h | ADRES1H | AN1.9 | AN1.8 | AN1.6 | AN1.6 | AN1.5 | AN1.4 | AN1.3 | AN1.2 | xxxx xxxx | uuuu uuuu |
| 55h | ADRES1L | AN1.1 | AN1.0 | — | — | — | — | — | — | xx-- ---- | uu-- ---- |
| 56h | ADRES0H | AN0.9 | AN0.8 | AN0.6 | AN0.6 | AN0.5 | AN0.4 | AN0.3 | AN0.2 | xxxx xxxx | uuuu uuuu |
| 57h | ADRES0L | AN0.1 | AN0.0 | — | — | — | — | — | — | xx-- ---- | uu-- ---- |

* These addresses are used when using the "Write Register" or "Read Register" command

** The GPDDR register is not offset to RAM the same as the other registers in the EPROM

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NOTES:

4.0 DEVICE OPERATION

4.1 Power-Up Sequence

The following sections describe the events/actions of the MCP2502X/5X during normal Power-up and operation.

4.1.1 POWER-ON RESET

The MCP2502X/5X goes through a sequence of events at Power-on Reset (POR) to load the programmed configuration and insure that errors are not introduced on the bus. During this time, the device is prevented from generating a low condition on the TXCAN pin. The TXCAN pin must remain high from Power-on until the device goes on bus.

Operational Mode at Power-On

The MCP2502X/5X initially powers up in Configuration mode. While in this mode, the MCP2502X/5X will be prevented from sending or receiving messages via the CAN interface. The ADC and PWM peripherals are disabled while in this mode.

Self-Configuration

Once the MCP2502X/5X is out of Reset, it will perform a self-configuration. This is accomplished by transferring the contents of the EPROM array to the corresponding locations within the SRAM array. In addition, the checksum of the data written to SRAM will be compared to a pre-programmed value as a test of valid data.

Going On Bus

Once the self-configuration cycle has successfully completed, the MCP2502X/5X switches to Listen-only mode. It will remain in this mode until an error-free CAN message is detected. This is done to ensure that the device is at the correct bus rate for the system.

Once the device detects an error-free message, it waits for CAN bus idle before switching to Normal mode. This prevents it from going on bus in the middle of another node's transmission and generating an error frame.

Alternately, the MCP2505X may directly enter Normal mode, without first entering Listen-only Mode, after completing its self-configuration. This is configured by the user via a control bit (OPTREG2.PUNRM).

Once the MCP2502X/5X enters Normal mode, it is ready to send/receive messages via the CAN interface. At this point the ADC and PWM peripherals are operational, if enabled.

Scheduled Transmissions

When the MCP2502X/5X has gone on bus it will transmit the On Bus message once, regardless of whether it is enabled or not. This message notifies the network of the MCP2502X/5X's presence. The On Bus message will (if enabled, STCON.STEN) repeat at a frequency determined by the STCON register ([Register 4-1](#)).

This message can also be configured to send the "Read A/D Register" data bytes with the predefined identifier in TXID2 by setting STCON.STMS = 1.

Notes: The first On Bus message sent after Power-up will NOT send the "Read A/D Register" data bytes, regardless of the STCON.STMS value.

If the MCP2502X/5X enters SLEEP mode, the scheduled transmissions will cease until the device wakes up again. This implies that SLEEP mode has priority over scheduled transmissions.

4.2 Message Functions

The MCP2502X/5X uses the global mask (RXMASK), two filters (RXF0 and RXF1), and two receive buffers (RB0 and RB1) to determine if a received message should be acted on. There are 16 functions that can be performed by the MCP2502X/5X, based on received messages (see [Table 4-1](#)). These functions allow the device to be accessed for Information Request/Input/Output operations, but also to be reconfigured via the CAN bus, if necessary.

4.3 Message Types

There are three types of messages that are used to implement the functions of [Table 4-1](#).

- Information Request Messages (IRMs):
Received by the MCP2502X/5X
- Output Messages:
Transmitted from the MCP2502X/5X as a response to IRMs
- Input Messages:
Received by the MCP2502X/5X and used to modify registers

Notes: IRMs and Input messages are both input messages to the MCP2502X/5X.

IRMs are received into receive buffer 0
Input Messages are received into receive buffer 1.

This must be taken into account while configuring the acceptance filters.

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4.3.1 INFORMATION REQUEST MESSAGES

IRMs are messages that are received by the the MCP2502X/5X into the Receive Buffer 0 (matches Filter 0); and then, responded to by transmitting a message (output message) containing the requested data.

IRMs can be implemented as either a Remote Transfer Request (RTR) or a Data Frame message by configuring the MTYPE bit in the OPTREG2 register.

TABLE 4-1: MESSAGE FUNCTION

| Name | Description |
|-----------------------------------|--|
| Read A/D Registers | Transmits a single message containing the current state of the analog and I/O registers, including the configuration |
| Read Control Registers | Transmits several control registers not included in other messages |
| Read Configuration Registers | Transmits the contents of many of the Configuration registers |
| Read CAN error states | Transmits the error flag register and the error counts |
| Read PWM Configuration | Transmits the registers associated with the PWM modules |
| Read User Registers 1 | Transmits the values in bytes 0 - 7 of the user memory |
| Read User Registers 2 | Transmits the values in bytes 8 -15 of the user memory |
| Read Register* | Transmits a single byte containing the value in an addressed user memory register |
| Write Register | Uses a mask to write a value to an addressed register |
| Write TX Message ID0 (TXID0) | Writes the identifiers to a specified value |
| Write TX Message ID1 (TXID1) | Writes the identifiers to a specified value |
| Write TX Message ID2 (TXID2) | Writes the identifiers to a specified value |
| Write I/O Configuration Registers | Writes specified values to the three IOCON registers |
| Write RX Mask | Changes the receive mask to the specified value |
| Write RX Filter0 | Changes the specified filter to the specified value |
| Write RX Filter1 | Changes the specified filter to the specified value |

* The Read Register command is available when using extended message format only. Not available with standard message format.

4.3.1.1 RTR Message Type

When RTR message types are selected (OPTREG2.MTYPE) and a node in the system wants information from the MCP2502X/5X, it has to send a remote frame on the bus. The identifier for the remote frame must be such that it will be accepted through the MCP2502X/5X's mask/filter process (using RXF0). The RTR message type (remote frames) is the default configuration (MTYPE bit = 0).

Information Request "RTR" messages must not only meet the RXMASK/RXF0 criteria but must also have the RTR bit of the CAN ID set (since the filter registers do not contain an explicit RTR bit). If a message passes the mask/filter process and the RTR bit is a '0', that message will be ignored.

Once the MCP2502X/5X has received a remote frame, it will determine the function to be performed based upon the three LSB's (RXB0SIDL.SID2:SID0 for standard messages and RXB0EID0.EID2:EID0 for extended messages) of the received remote frame.

Additionally, a predefined Data Length Code (DLC) must be sent to signify the number of data bytes that the MCP2502X/5X must return in the output message (see Table 4-2 and Table 4-3).

4.3.1.2 Data Frame Message Type

When a non-RTR (or data frame) message type is selected and a node in the system wants information from the MCP2502X/5X, it sends an Information Request in the form of a data frame. The identifier for this request must be such that it will be accepted through the MCP2502X/5X's mask/filter process (using RXF0).

Information request messages in the data frame format must not only meet the RXMASK/RXF0 criteria, but must also have the RTR bit of the CAN ID cleared (since the filter registers do not contain an explicit RTR bit). If a message passes the mask/filter process and the RTR bit is a '1', that message will be ignored.

Once the MCP2502X/5X has received a data frame information request, it will determine the function to be performed based upon the three LSB's (RXB0SIDL.SID2:SID0 for standard messages and RXB0EID0.EID2:EID0 for extended messages) of the received data frame. Also, Bit 3 of the received message ID must be set to a '1'.

In addition, the data length code (DLC) must be set to a zero. Refer to Table 4-2 and Table 4-3 for more information.

Regardless of the message format, all messages (except the Read Register message) can use either standard or extended identifiers.

The Read Register message has one additional requirement; it must be an extended identifier. This is discussed in more detail in Table 4-1 and Table 4-3.

4.3.2 OUTPUT MESSAGES

The data frame sent in response to the information request message is defined as an output message.

If the data frame is in response to a remote frame, it has the same identifier (standard or extended) and contains the same number of data bytes specified by the DLC of the remote frame (per the CAN 2.0B specification).

Note: If the DLC of the incoming remote frame differs from the message definitions summarized in [Table 4-2](#) and [Table 4-3](#), the resulting output message will limit itself to the erroneous DLC that was received (to maintain compliance with the Bosch CAN specification). The output message will concatenate the number of data bytes for an erroneous DLC that is less than the defined number. For an erroneous DLC that is greater than the defined number, the MCP2502X/5X will extend the number of data bytes, with the data value of the last defined data byte being repeated in the extra bytes in the data field.

If the output message is in response to a data frame, the lower-three LSB's of the identifier (standard or extended) must be the same as the received message, as well as the upper-seven MSb's in the case of a standard identifier, or the upper 25 MSb's in the case of an extended identifier. Bit 3 of a standard or extended identifier of the output message will differ from the received information request message in that the value equals '1' for an IRM and equals '0' for the resulting output message.

Output messages contain the requested data (in the data field). **Example:** The information request message Read CAN error is a remote transmit request received by the MCP2502X/5X with a DLC of 3. The responding output message will return a data frame that contains the same identifier (standard or extended) as the receive message. The accompanying data bytes will contain the values of the predefined GPIO registers and related control/status registers, as shown in [Table 4-2](#) and [Table 4-3](#).

4.3.3 INPUT MESSAGES

Input messages are received into receive buffer 1 and are used to change the values of the pre-defined groups of registers. There is also an input message that can change a single register's contents. The primary purpose of input messages are to reconfigure MCP2502X/5X parameters (if needed) while in an operating CAN system and are, therefore, optional in system implementation. These messages are in the form of standard (or extended) data frames (per the CAN 2.0B specification) that have identifiers which pass the MCP2502X/5X's mask/filter process (using RXF1).

After passing the mask and filter, the lower-three bits of the standard identifier (RXF1SIDL.SID2:SID0) will indicate which register(s) are to be written. The values for the register(s) are contained in the data byte registers as defined in [Table 4-2](#).

Note: If using more than one controlling node, the MCP2502X/5X must be set up to accept input messages with different identifiers in order to avoid possible message collisions in the DLC or data bytes if transmitted at the same time.

Notes: IRMs can theoretically be sent by more than one controlling node because the message is a predefined constant and destructive collisions will not occur.

The number of data bytes in an input message must match the DLC number as defined in [Table 4-2](#) and [Table 4-3](#). If the user specifies and transmits an input message with a DLC that is less than the required number of data bytes, the MCP25020 will operate on corrupted data for the bytes that it did not receive and unknown results will occur.

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4.4 Dynamic Message Handling

The design insures that transmit and receive messages are handled properly for variable bus-loading conditions and different transmit/receive combinations.

4.4.1 MESSAGE ACCEPTANCE/ REJECTION

Messages received that meet the Mask/RXFn criteria are then compared to the requirements for input messages or IRMs, as determined by the filter used to accept the message. If the message meets the requirements of one of the associated input or information request messages, the appropriate actions for that message function are taken.

4.4.2 RECEIVING MULTIPLE MESSAGES

The MCP2502X/5X can only receive and process one message at a time. While the MCP2502X/5X should have ample time to process any received message before another is completely received, a second message received before the first message is finished processing will be lost.

However, the MCP2502X/5X has the ability to notify the network if a message is lost. TXID1 can be configured to transmit a message if a receive overflow occurs (OPTREG2.CAEN = 0).

4.4.3 TRANSMIT MESSAGE PRIORITY

There is a priority for all transmit messages, including TXIDn and all "Output" messages.

The transmit message priority is as follows:

1. Output messages have the highest priority. Prioritization of the individual output message types is determined by the three bits that determine message type, with the lowest value having the highest priority (e.g., Read A/D Regs is a higher priority than Read Control Regs).
2. TXID2 (Transmit auto-converted messages) has the second-highest priority.
3. TXID1 (Command acknowledge) has the third-highest priority.
4. TXID0 (On Bus message) has the lowest priority.

In the event two or more messages are pending transmission, transmit-message prioritization will occur and the highest message type will be sent first. Messages that are currently transmitting will not be prioritized.

TABLE 4-2: COMMAND MESSAGES (STANDARD IDENTIFIER)

| Information Request Messages (to MCP2502X/5X) | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|------------------|-------------|---|---|----|----|
| Standard ID | | | | | | | | | | | | Data Bytes | | | | | |
| 1 | 0 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | R T R E | D L C | | | | |
| Read A/D Regs | x | x | x | x | x | x | x | x | * | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 8* |
| Read Control Regs | x | x | x | x | x | x | x | x | * | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 7* |
| Read Config Regs | x | x | x | x | x | x | x | x | * | 0 | 1 | 0 | 1 | 0 | 1 | 5* | |
| Read CAN Error | x | x | x | x | x | x | x | x | * | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 3* |
| Read PWM Config | x | x | x | x | x | x | x | x | * | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 6* |
| Read User Mem (bank1) | x | x | x | x | x | x | x | x | * | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 8* |
| Read User Mem (bank2) | x | x | x | x | x | x | x | x | * | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 8* |

| Output Messages (from MCP2502X/5X) | | | | | | | | | | | | | | | | | | |
|------------------------------------|---|---|---|---|---|---|---|---|---|---|---|------------------|-------------|---|---|---|---|---|
| Standard ID | | | | | | | | | | | | Data Bytes | | | | | | |
| 1 | 0 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | R T R E | D L C | | | | | |
| Read A/D Regs | x | x | x | x | x | x | x | x | * | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 8 |
| Read Control Regs | x | x | x | x | x | x | x | x | * | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 7 |
| Read Config Regs | x | x | x | x | x | x | x | x | * | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 5 |
| Read CAN Error | x | x | x | x | x | x | x | x | * | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 3 |
| Read PWM Config | x | x | x | x | x | x | x | x | * | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 6 |
| Read User Mem (bank1) | x | x | x | x | x | x | x | x | * | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 8 |
| Read User Mem (bank2) | x | x | x | x | x | x | x | x | * | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 8 |

| Input Messages** (to MCP2502X/5X) | | | | | | | | | | | | | | | | | | |
|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|------------------|-------------|---|---|---|---|---|
| Standard ID | | | | | | | | | | | | Data Bytes | | | | | | |
| 1 | 0 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | R T R E | D L C | | | | | |
| Write Register | x | x | x | x | x | x | x | x | x | x | x | 0 | 0 | 0 | 1 | 1 | 3 | |
| Write TX Message ID 0 | x | x | x | x | x | x | x | x | x | x | x | 0 | 0 | 1 | 0 | 0 | 4 | |
| Write TX Message ID 1 | x | x | x | x | x | x | x | x | x | x | x | 0 | 1 | 0 | 0 | 0 | 4 | |
| Write TX Message ID 2 | x | x | x | x | x | x | x | x | x | x | x | 0 | 1 | 0 | 0 | 0 | 4 | |
| Write I/O Configuration | x | x | x | x | x | x | x | x | x | x | x | 1 | 0 | 0 | 0 | 1 | 5 | |
| Write RX Mask | x | x | x | x | x | x | x | x | x | x | x | 1 | 0 | 0 | 1 | 0 | 4 | |
| Write RX Filter0 | x | x | x | x | x | x | x | x | x | x | x | 1 | 1 | 0 | 0 | 1 | 0 | 4 |
| Write RX Filter1 | x | x | x | x | x | x | x | x | x | x | x | 1 | 1 | 1 | 0 | 0 | 0 | 4 |

* If using non-RTR messages for information request messages (IRM), the RTR bit = 0, DLC bit field = 0, and bit 3 of the output message ID = 0.
 If using RTR messages for IRMs, the RTR bit = 1, DLC bit field = number of bytes in corresponding output message, and bit three of the IRM ID = x (don't care), also, bit 3 of the output message = x (don't care).
 ** User-defined IRM IDs must be different from input message IDs to avoid message contention between the corresponding output message and the input message.

4.5 Automatic Transmission

The MCP2502X/5X can automatically initiate four different message types to indicate the following situations:

- Edge detected on a digital input (TXID2)
- Threshold exceeded on an analog input (TXID2)
- Error condition (Read Error output message)
- Scheduled transmissions (TXID0)

The buffers have an implied transmit priority, where buffer 2 is the highest and buffer 0 is the lowest. Therefore, multiple message buffers can be requested for transmission and each one will be sent in order of priority.

4.5.1 DIGITAL INPUT EDGE DETECTION

Each GPIO pin configured as a digital input can be individually configured to automatically transmit a message when a defined edge occurs, as explained in the GPIO module section. When transmitting this message, the MCP2502X/5X uses TXID2. The DLC is set to two and the first two bytes of the Read A/D registers (IOINTFL and GPIO) are sent.

4.5.2 ANALOG INPUT THRESHOLD DETECTION

Each GPIO pin that has been configured as an analog input can be individually configured to automatically transmit a message when a threshold is exceeded as described in the Analog-to-Digital Converter Module section. The MCP2502X/5X sends TXID2 when transmitting this message. The DLC is set to eight and the eight bytes of the 'Read A/D Registers' are sent.

Note: The GPIO register that is sent with the message (data byte 2) can be ignored if there are no digital inputs enabled for change-of-state, as it contains no useful information for the Analog Input Threshold Detect function.

4.5.2.1 Hysteresis Function

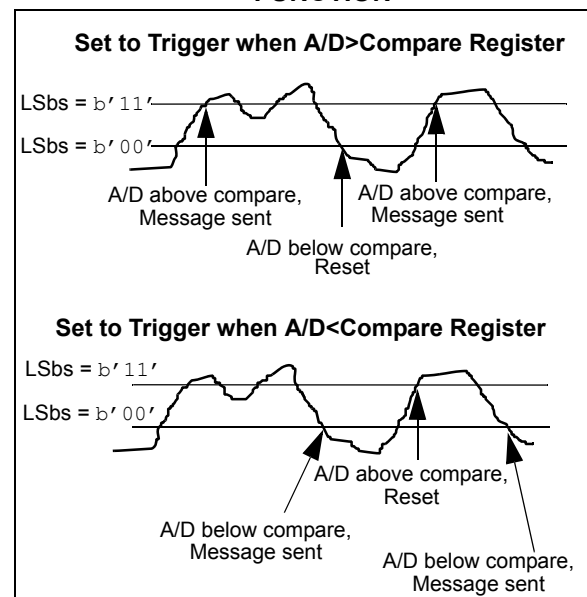
This function is automatic and will insure that an analog value that is on the compare edge (i.e., toggling LSB) does not fill the CAN bus with continuous A/D message transmissions.

The hysteresis uses the two LSB's of the compare register. These two bits are forced and are not configurable by the user. They will be forced to either $b'00'$ or $b'11'$, depending on the compare polarity. If configured for A/D result $>$ compare register, the automatic transmission will occur when the A/D value is greater than or equal to $b'nnnn\ nnnn\ 11'$ and reset when less than or equal to $b'nnnn\ nnnn\ 00'$. The opposite conditions must occur if the compare polarity is set for A/D result $<$ compare register.

A hysteresis example:

- The user sets the upper-eight bits of the 10-bit compare register (ADCMP0H). The lower-two bits of the compare register are not configurable by the user and are forced to either $b'11'$ or $b'00'$ depending on the polarity of the compare threshold (i.e., transmit is triggered above or below the compare value via the IOINTPO register).
- The user sets the polarity of the compare threshold (IOINTPO). In this example, the threshold is set for triggering a message on an $A/D >$ compare register. The two LSB's are forced to $b'11'$.
- When the A/D conversion exceeds the compare register ($b'nnnn\ nnnn\ 11'$), an automatic transmission will occur once.
- In order for the automatic transmission to occur again, the A/D value must first drop below the compare register $b'nnnn\ nnnn\ 00'$ and then back above the compare register $b'nnnn\ nnnn\ 11'$.

FIGURE 4-1: HYSTERESIS FUNCTION



4.5.3 ERROR CONDITION

The MCP2502X/5X can be configured to automatically transmit a message whenever one or more of the following error conditions occur:

- Receiver has entered error-warning state
- Receiver has entered error-passive state
- Transmitter has entered error-warning state
- Transmitter has entered error-passive state
- A Receive buffer has overflowed

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If the Error Condition message is enabled (OPTREG2.TXONE = 1) and one of the above conditions occur, the MCP2502X/5X sends TXID1 identifier with output message Read CAN Error States data field (three data bytes).

4.5.4 SCHEDULED TRANSMISSIONS

The MCP2502X/5X has the capability of sending scheduled transmissions (On Bus message), if enabled.

The scheduled transmission control register (STCON) enables and configures the occurrence of the scheduled message. Setting the STEN bit in the STCON register enables the scheduled message. The STBF1:STBF0 and STM3:STM0 bits allow a scheduled transmission to be initiated from a minimum of 256 μ s to a maximum of 16.8 seconds (using a 16 MHz Fosc) and the following equation:

$$\text{Scheduled Transmission} = \text{STBF1:STBF0}(\text{STM3:STM0})$$

Message Type - The message sent for scheduled transmissions consists of either TXID0 with zero data bytes or TXID0 with eight data bytes containing the Read A/D Regs message, depending on STMS bit in the STCON register.

Note: The actual scheduled transmission intervals may vary slightly due to the internal event queue of the control module.

REGISTER 4-1: STCON - SCHEDULED TRANSMISSION CONTROL REGISTER

| | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| | STEN | STMS | STBF1 | STBF0 | STM3 | STM2 | STM1 | STM0 |
| bit 7 | | | | | | | | bit 0 |

- bit 7 **STEN:** Scheduled Transmission Enable bits
1 = Enabled
0 = Disabled
- bit 6 **STMS:** Scheduled Transmission Message Select
1 = Sends Transmit ID 0 (TXID0) with the "Read A/D Regs" data (DLC = 8)
0 = Sends Transmit ID 0 (TXID0) with no data (DLC = 0)
- bit 5-4 **STBF1:STBF0:** Base Transmission Frequency bits
00 = 4096Tosc
01 = 16•(4096Tosc)
10 = 256•(4096Tosc)
11 = 4096•(4096Tosc)
(e.g., STBF1:STBF0 => 00 => 256 μ s for a 16 MHz Fosc)
- bit 3-0 **STM3:STM0:** Scheduled Transmission Multiplier bits
0000 = 1
0001 = 2
-
-
1110 = 15
1111 = 16

Legend:

| | | |
|--------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

TABLE 4-4: REGISTERS ASSOCIATED WITH THE CAN MODULE

| Addr | Name | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Value on POR | Value on RST |
|------|----------|----------|-------|---------|---------|---------|---------|---------|---------|--------------|--------------|
| 0Bh | CNF1 | SJW1 | SJW0 | BRP5 | BRP4 | BRP3 | BRP2 | BRP1 | BRP0 | xxxx xxxx | uuuu uuuu |
| 0Ch | CNF2 | BTLM-ODE | SAM | PHSEG12 | PHSEG11 | PHSEG10 | PRSEG2 | PRSEG1 | PRSEG0 | xxxx xxxx | uuuu uuuu |
| 0Dh | CNF3 | — | WAKF | — | — | — | PHSEG22 | PHSEG21 | PHSEG20 | -x- xxxx | -u- uuuu |
| 10h | STCON | STEM | STMS | STBF1 | STBF0 | STM3 | STM2 | STM1 | STM0 | 0xxx xxxx | 0uuu uuuu |
| 11h | OPTREG2 | CAEN | ERRE | TXONE | SLPEN | MTYPE | PDEFEN | PUSLP | PUNRM | 0000 0000 | uuuu uuuu |
| 14h | RXMSIDH | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | xxxx xxxx | uuuu uuuu |
| 15h | RXMSIDL | SID2 | SID1 | SID0 | — | — | — | EID17 | EID16 | xxx- --xx | uuu- --uu |
| 16h | RXMEID8 | EID15 | EID14 | EID13 | EID12 | EID11 | EID10 | EID9 | EID8 | xxxx xxxx | uuuu uuuu |
| 17h | RXMEID0 | EID7 | EID6 | EID5 | EID4 | EID3 | EID2 | EID1 | EID0 | xxxx xxxx | uuuu uuuu |
| 18h | RXF0SIDH | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | xxxx xxxx | uuuu uuuu |
| 19h | RXF0SIDL | SID2 | SID1 | SID0 | — | — | — | EID17 | EID16 | xxx- --xx | uuu- --uu |
| 1Ah | RXF0EID8 | EID15 | EID14 | EID13 | EID12 | EID11 | EID10 | EID9 | EID8 | xxxx xxxx | uuuu uuuu |
| 1Bh | RXF0EID0 | EID7 | EID6 | EID5 | EID4 | EID3 | EID2 | EID1 | EID0 | xxxx xxxx | uuuu uuuu |
| 1Ch | RXF1SIDH | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | xxxx xxxx | uuuu uuuu |
| 1Dh | RXF1SIDL | SID2 | SID1 | SID0 | — | — | — | EID17 | EID16 | xxx- --xx | uuu- --uu |
| 1Eh | RXF1EID8 | EID15 | EID14 | EID13 | EID12 | EID11 | EID10 | EID9 | EID8 | xxxx xxxx | uuuu uuuu |
| 1Fh | RXF1EID0 | EID7 | EID6 | EID5 | EID4 | EID3 | EID2 | EID1 | EID0 | xxxx xxxx | uuuu uuuu |
| 20h | TXB0SIDH | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | xxxx xxxx | uuuu uuuu |
| 21h | TXB0SIDL | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxx- x-xx | uuu- u-uu |
| 22h | TXB0EID8 | EID15 | EID14 | EID13 | EID12 | EID11 | EID10 | EID9 | EID8 | xxxx xxxx | uuuu uuuu |
| 23h | TXB0EID0 | EID7 | EID6 | EID5 | EID4 | EID3 | EID2 | EID1 | EID0 | xxxx xxxx | uuuu uuuu |
| 24h | TXB1SIDH | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | xxxx xxxx | uuuu uuuu |
| 25h | TXB1SIDL | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxx- x-xx | uuu- u-uu |
| 26h | TXB1EID8 | EID15 | EID14 | EID13 | EID12 | EID11 | EID10 | EID9 | EID8 | xxxx xxxx | uuuu uuuu |
| 27h | TXB1EID0 | EID7 | EID6 | EID5 | EID4 | EID3 | EID2 | EID1 | EID0 | xxxx xxxx | uuuu uuuu |
| 28h | TXB2SIDH | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | xxxx xxxx | uuuu uuuu |
| 29h | TXB2SIDL | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxx- x-xx | uuu- u-uu |
| 2Ah | TXB2EID8 | EID15 | EID14 | EID13 | EID12 | EID11 | EID10 | EID9 | EID8 | xxxx xxxx | uuuu uuuu |
| 2Bh | TXB2EID0 | EID7 | EID6 | EID5 | EID4 | EID3 | EID2 | EID1 | EID0 | xxxx xxxx | uuuu uuuu |

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NOTES:

5.0 GPIO MODULE

5.1 Description

The MCP2502X/5X has eight general-purpose input/output pins (GP0 to GP7), collectively labeled GPIO. All GPIO port pins have TTL input levels and full CMOS output drivers, with the exception of GP7, which is input only. Pins GP6:GP0 can be individually configured as input or output via the GPDDR register.

Note: The GPDDR register controls the direction of the GPIO pins, even when they are being used as analog inputs. The user must ensure that the bits in the GPDDR register are maintained set (input) when using them as analog inputs.

Each of the GPIO pins has a weak internal pull-up resistor. A single control bit (OPTREG.GPPU) can turn on/off all the pull-ups. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled during a Power-on Reset.

All pins are multiplexed with an alternate function, including analog-to-digital conversion on up to four of the GPIO pins, analog VREF inputs up to two pins, PWM outputs up to two pins, clock-out function and external Reset. The operation of each pin is selected by clearing, or setting, control bits in various control registers. GPIO pin functions are summarized in [Table 5-1](#).

TABLE 5-1: GPIO FUNCTIONS

| Name | Bit# | Function |
|--------------|------|--|
| GP0/AN0 | bit0 | I/O or analog input |
| GP1/AN1 | bit1 | I/O or analog input |
| GP2/AN2/PWM2 | bit2 | I/O, analog input or PWM out |
| GP3/AN3/PWM3 | bit3 | I/O, analog input or PWM out |
| GP4/VREF- | bit4 | I/O or analog voltage reference |
| GP5/VREF+ | bit5 | I/O or analog voltage reference |
| GP6/CLKOUT | bit6 | I/O or Clock output |
| GP7/nRST/VPP | bit7 | Input, external Reset input or programming voltage input |

5.2 Digital Input Edge Detection

All GPIO pins have a digital input edge detection feature that will automatically transmit a message when an edge with the proper polarity occurs on any of the digital inputs. Only pins configured as inputs and enabled for this function via control register IOINTPO will perform this operation.

Note: Refer to [Section 7.4 “A/D Threshold Detection”](#) for information regarding A/D channels.

Three control registers are associated with this function. An enable pin for each GPIO pin resides in the IOINTEN register. When a bit is set to a '1', the corresponding GPIO pin is enabled to generate a transmit-on-change message (TXID2) when an edge of specified polarity occurs.

The digital edge detection function on a GPIO pin configured as a digital input is edge triggered. A rising-edge will generate a transmission if the corresponding bit in the IOINTPO register is set. A falling-edge will generate a transmission if the bit is cleared. When a valid edge appears on the enabled GPIO pin, CAN message TXID2 is initiated.

The edge-detection function on any given GPIO pin (configured as a digital input) can wake up the processor from SLEEP if the corresponding interrupt enable bit in the IOINTEN register was set prior to going into SLEEP mode. If a wake-up from SLEEP is caused in this manner, the device will immediately initiate a transmit message (TXID2).

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REGISTER 5-1: GPDDR - DATA DIRECTION REGISTER

| U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| — | DDR6 | DDR5 | DDR4 | DDR3 | DDR2 | DDR1 | DDR0 |
| bit 7 | | | | | | | bit 0 |

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **DDR6:DDR0:** Data Direction Register* bits

1 = corresponding GPIO pin is configured as an input

0 = corresponding GPIO pin is configured as an output

* must be set if corresponding analog channel is enabled (see ADCON1)

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

REGISTER 5-2: GPLAT - GPIO OUTPUT REGISTER

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| — | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 |
| bit 7 | | | | | | | bit 0 |

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **GP6:GP0:** GPIO Bits

1 = corresponding GPIO pin output latch is a '1'

0 = corresponding GPIO pin output latch is a '0'

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

REGISTER 5-3: IOINTEN REGISTER

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| GP7TXC | GP6TXC | GP5TXC | GP4TXC | GP3TXC | GP2TXC | GP1TXC | GP0TXC |
| bit 7 | | | | | | | bit 0 |

bit 7-0 **GP7TXC:GP0TXC:** Transmit-on-change Enable bits

1 = Enable Transmit-On-Change/Compare For Corresponding GPIO/AN Channel

0 = Disable Transmit-On-Change/Compare For Corresponding GPIO/AN Channel

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

REGISTER 5-4: IOINTPO REGISTER

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| GP7POL | GP6POL | GP5POL | GP4POL | GP3POL | GP2POL | GP1POL | GP0POL |
| bit 7 | | | | | | | bit 0 |

bit 7-0 **GP7POL:GP0POL:** Transmit-on-change Polarity bits

- 1 = Digital Inputs: Low-to-High Transition On Corresponding GPIO Input Pin Generates a transmit message
Analog Inputs: A/D result above compare value generates a transmit message
- 0 = Digital Inputs: High-to-Low Transition On Corresponding GPIO Input Generates transmit message
Analog Inputs: A/D result below compare value generates a transmit message

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 5-5: IOINTFL REGISTER

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| GP7TXF | GP6TXF | GP5TXF | GP4TXF | GP3TXF | GP2TXF | GP1TXF | GP0TXF |
| bit 7 | | | | | | | bit 0 |

bit 7-0 **GP7TXF:GP0TXF:** Transmit-on-change Polarity bits

- 1 = Digital Inputs: A valid edge has occurred on the digital input
Analog Inputs: A/D result does exceed the compare threshold
- 0 = Digital Inputs: A valid edge has not occurred on the digital input
Analog Inputs: A/D result does not exceed the compare threshold

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

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REGISTER 5-6: OPTREG1 REGISTER

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|--------|--------|-----|-------|-------|-------|
| GPPU | CLKEN | CLKPS1 | CLKPS0 | — | CMREQ | AQT1 | AQT0 |
| bit 7 | | | | | | | bit 0 |

- bit 7 **GPPU:** Weak pull-up enabled
 1 = Weak pull-ups disabled
 0 = Weak pull-ups enabled (GP7:GP0)
- bit 6 **CLKEN:**
 1 = Clock Out Function disabled
 0 = Clock Out Function enabled
- bit 5-4 **CLKPS1:CLKPS0:** CLKOUT Prescaler bits
 00 = Fosc/1
 01 = Fosc/2
 10 = Fosc/4
 11 = Fosc/8
- bit 3 **Reserved:**
- bit 2 **CMREQ:** Requests mode of operation (allows mode changes via the CAN bus)
 1 = Requests Listen-only mode
 0 = Requests Normal mode *
 * CMREQ must be cleared as default to avoid device entering Listen-only mode on first "Input" message.
- bit 1-0 **AQT1:AQT0:** Analog Acquisition Time bits
 00 = 64Tosc
 01 = 2•(64Tosc)
 10 = 4•(64Tosc)
 11 = 8•(64Tosc)
 (e.g., AQT1:AQT0 => 00 => 2.56 µs for a 25 MHz Fosc)

| Legend: | | | |
|--------------------|------------------|------------------------------------|--------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

REGISTER 5-7: OPTREG2 REGISTER

| | | | | | | | |
|-------|-------|--------|-------|-------|--------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CAEN | ERREN | TXONEN | SLPEN | MTYPE | PDEFEN | PUSLP | PUNRM |
| bit 7 | | | | bit 0 | | | |

- bit 7 **CAEN:** Command Acknowledge Enable bit
 1 = Enables the command acknowledge message (TXID1)
 0 = Enables the receive overflow message (TXID1)
- bit 6 **ERREN:** Error Recovery Enable bit
 1 = MCP2502X/5X will recover into Listen-only mode from bus off
 0 = MCP2502X/5X will recover into Normal mode from bus-off
- bit 5 **TXONEN:** Transmit on Error Condition bit (REC or TEC)
 1 = Enable, will send message if error counter(s) go high enough
 0 = Disable, will NOT send message regardless of error counter values
- bit 4 **SLPEN:** Low power SLEEP mode enable/disable
 1 = Device will enter Sleep if bus is idle for at least 1408 bit times
 0 = SLEEP mode is disabled
- bit 3 **MTYPE:** Determines if information request messages use RTR or not
 1 = RTR is NOT used for IRM (Data Frame)
 0 = RTR is used for IRM (Remote Frame)
- bit 2 **PDEFEN:** Enables PWM outputs to return to POR default values when CAN bus communication is lost
 1 = Enables PWM output default values
 0 = Disables PWM output default values
- bit 1 **PUSLP:** Allows device to enter SLEEP while in Listen-only mode during Power-up sequence
 1 = Enables SLEEP when in Listen-only mode during Power-up sequence
 0 = Disables SLEEP when in Listen-only mode during Power-up sequence
- bit 0 **PUNRM:** Enters Normal mode after completing self-configuration during Power-up sequence
 1 = Enters "Normal" mode after completing self-configuration during Power-up sequence
 0 = Enables "Listen-only" mode after completing self-configuration during Power-up sequence and waits for an error-free message before switching to Normal mode

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH GPIO MODULE

| Addr | Name | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Value on POR | Value on RST |
|---------------|---------|--------|--------|--------|--------|--------|--------|--------|--------|--------------|--------------|
| Bank 0 | | | | | | | | | | | |
| 34h | GPDDR | — | DDR6 | DDR5 | DDR4 | DDR3 | DDR2 | DDR1 | DDR0 | -111 1111 | -111 1111 |
| 00h | IOINTEN | GP7TXC | GP6TXC | GP5TXC | GP4TXC | GP3TXC | GP2TXC | GP1TXC | GP0TXC | 0000 0000 | 0000 0000 |
| 01h | IOINTPO | GP7POL | GP6POL | GP5POL | GP4POL | GP3POL | GP2POL | GP1POL | GP0POL | 0000 0000 | 0000 0000 |
| 04h | OPTREG1 | GPPU | CLKEN | CLKPS1 | CLKPS0 | — | CMREQ | AQT1 | AQT0 | 0000 ---- | 0000 ---- |

Legend: x = unknown, U = unchanged, - = unimplemented read as '0'. Shaded cells are not used by module.

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NOTES:

6.0 PWM MODULE

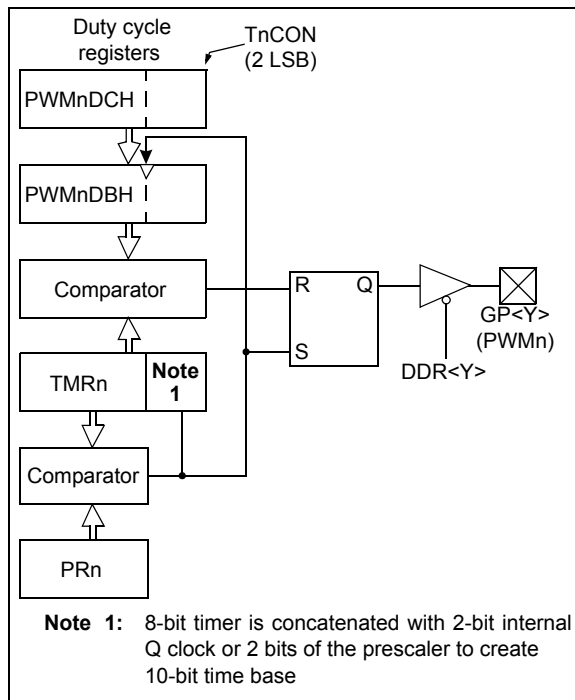
6.1 Description

There are two Pulse Width Modulation (PWM) modules (PWM1 and PWM2) that generate up to a 10-bit resolution output signal on GP2 and GP3, respectively. Each of these outputs can be separately enabled, with each having its own associated timer, duty cycle and period registers for controlling the PWM output shape.

Each PWM module contains a set of master/slave duty cycle registers, providing up to a 10-bit resolution PWM output. Figure 6-1 shows a simplified block diagram of the PWM module. A PWM output has a time base (period) and a time that the output stays high (duty cycle), as shown in Figure 6-2. The frequency of the PWM is the inverse of the period ($1/\text{period}$).

At Power-on, the PWM outputs are not enabled until after the self-configuration sequence has been completed (i.e., all SRAM registers have been loaded with their default values) to prevent invalid signals from occurring on the PWM outputs.

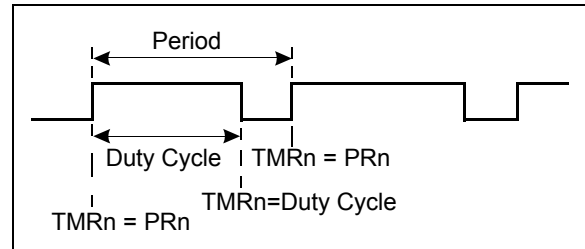
FIGURE 6-1: SIMPLIFIED BLOCK DIAGRAM



The PWM outputs can be forced to their default POR conditions if CAN bus communication is lost and is enabled via OPTREG2.PDEFEN. The system designer must implement a hand-shaking protocol, such that the MCP2505X will receive a valid message into one of the receive buffers before four successive scheduled transmissions occur. If a valid message is not received, the PWM outputs GP2 and GP3 will automatically

reconfigure to their default conditions. This includes the PWM module itself being disabled and the GPIO being forced low, high or tri-state.

FIGURE 6-2: PWM OUTPUT



6.2 PWM Timer Modules

There are two 8-bit timers supporting the two PWM outputs. Both timers have a prescaler only. The timers are readable and writable and are cleared on any device Reset or when the timer is turned off.

The input clock ($F_{osc}/4$) has a prescale option of 1:1, 1:4 or 1:16, selected by control bits TnCKPS[1:0] in register TnCON<5:4> (where n corresponds to the appropriate timer).

Each timer module has an 8-bit period register, PRn. PRn is a readable and writable register. The timer module increments from 00h until it matches PRn and then resets to 00h on the next increment cycle. The PRn register is set when the device is reset.

Each timer can be shut off by clearing control bit TMRnON (TnCON<7>).

6.2.1 TIMER MODULE PRESCALER

The prescaler counters are cleared when a write to the TnCON or TMRn register or any device Reset (\overline{RST} Reset or Power-on Reset) occurs.

6.3 PWM Modules

Each PWM module contains a set of master/slave duty cycle registers, providing up to a 10-bit resolution PWM output. Figure 6-2 shows a simplified block diagram of the PWM module.

6.3.1 PWM PERIOD

The PWM period is specified by writing to the PRn register. The PWM period can be calculated using the following formula:

$$\text{PWM period} = [(PR_n) + 1] * 4T_{OSC} * (\text{TMRn prescale value})$$

$$\text{PWM frequency} = 1 / (\text{PWM period})$$

When TMRn is equal to PRn, the following two events occur on the next cycle:

- TMRn is cleared
- The PWM duty cycle is latched from PWMnDCH into PWMnDBH

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6.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the PWMnDCH and TnCON registers. Up to 10-bit resolution is available. The PWMnDCH contains the eight MSb's, while the TnCON register contains the two LSb's. This 10-bit value is represented by PWM1DCH:T1CON<1:0> for PWM Module 1 and PWM2DCH:T2CON<1:0> for PWM Module 2.

The following equation is used to calculate the PWM duty cycle:

$$PWMDC = (PWMnDC) * T_{OSC} * TMRn \text{ (prescale)}$$

PWMnDCH can be written to at any time, but the duty cycle value is not latched into PWMnDBH until after a match between PRn and TMRn occurs (i.e., the period is complete).

The PWMnDBH register and 2-bit internal latch are used to double-buffer the PWM duty cycle. This double-buffering is essential for glitchless PWM operation.

When the PWMnDBH and 2-bit latch match TMRn concatenated with an internal 2-bit Q clock or 2 bits of the TMRn prescaler, the PWM output pin is cleared.

Maximum PWM resolution (bits) for a given PWM frequency is equal to:

$$\log((F_{OSC}) / (F_{pwm})) / (\log(2) \text{ bits})$$

Note: If the PWM duty cycle value is longer than the PWM period (PWM duty cycle = 100%), the PWM output pin will not be cleared.

In order to achieve higher resolution, the PWM frequency must be decreased. In order to achieve higher PWM frequency, the resolution must be decreased. Table 6-1 lists example PWM frequencies and resolutions for Fosc = 20 MHz. TMRn prescaler and PRn values are also shown.

TABLE 6-1: PWM FREQUENCIES AND RESOLUTIONS AT 20 MHZ

| PWM Frequency | 1.22 kHz | 4.88 kHz | 19.53 kHz | 78.12 kHz | 156.30 kHz | 208.30 kHz |
|----------------------------|----------|----------|-----------|-----------|------------|------------|
| Timer Prescaler (1, 4, 16) | 16 | 4 | 1 | 1 | 1 | 1 |
| PRn Value | 0xFF | 0xFF | 0xFF | 0x3F | 0x1F | 0x17 |
| Maximum Resolution (bits) | 10 | 10 | 10 | 8 | 7 | 5.5 |

REGISTER 6-1: PWM1 DUTY CYCLE REGISTER MSB (PWM1DCH)

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| DC1B9 | DC1B8 | DC1B7 | DC1B6 | DC1B5 | DC1B4 | DC1B3 | DC1B2 |
| bit 7 | | | | bit 0 | | | |

bit 7-0 **DC1B9:DC1B2:** Most Significant PWM0 Duty Cycle bits

Legend:
 R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 6-2: PWM2 DUTY CYCLE REGISTER MSB (PWM2DCH)

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| DC2B9 | DC2B8 | DC2B7 | DC2B6 | DC2B5 | DC2B4 | DC2B3 | DC2B2 |
| bit 7 | | | | bit 0 | | | |

bit 7-0 **DC2B9:DC2B2:** Most Significant PWM2 Duty Cycle bits

Legend:
 R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 6-3: T1CON: TIMER1 CONTROL REGISTER

| R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-x | R/W-x |
|--------|-----|---------|---------|-----|-----|-------|-------|
| TMR1ON | — | T1CKPS1 | T1CKPS0 | — | — | DC1B1 | DC1B0 |
| bit 7 | | | | | | bit 0 | |

- bit 7 **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Disables Timer1
- bit 6 **Unimplemented:** Read as '0'
- bit 5-4 **T1CKPS1:T1CKPS0:** Timer1 Clock Prescale Select bits
00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16
- bit 3-2 **Unimplemented:** Read as '0'
- bit 1-0 **DC1B1:DC1B0:** Least Significant PWM1 Duty Cycle bits

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
- n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 6-4: T2CON: TIMER2 CONTROL REGISTER

| R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-x | R/W-x |
|--------|-----|---------|---------|-----|-----|-------|-------|
| TMR2ON | — | T2CKPS1 | T2CKPS0 | — | — | DC2B1 | DC2B0 |
| bit 7 | | | | | | bit 0 | |

- bit 7 **TMR2ON:** Timer2 On bit
1 = Enables Timer2
0 = Disables Timer2
- bit 6 **Unimplemented:** Read as '0'
- bit 5-4 **T2CKPS1:T2CKPS0:** Timer2 Clock Prescale Select bits
00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16
- bit 3-2 **Unimplemented:** Read as '0'
- bit 1-0 **DC2B1:DC2B0:** Least Significant PWM2 Duty Cycle bits

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
- n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

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REGISTER 6-5: PR1: PERIOD REGISTER

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| PR1B7 | PR1B6 | PR1B5 | PR1B4 | PR1B3 | PR1B2 | PR1B1 | PR1B0 |
| bit 7 | | | | | | | bit 0 |

bit 7-0 **PR1B7:PR1B0**: PWM1 Period Register bits

| |
|--|
| Legend: |
| R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' |
| - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown |

REGISTER 6-6: PR2: PERIOD REGISTER

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| PR2B7 | PR2B6 | PR2B5 | PR2B4 | PR2B3 | PR2B2 | PR2B1 | PR2B0 |
| bit 7 | | | | | | | bit 0 |

bit 7-0 **PR2B7:PR2B0**: PWM2 Period Register bits

| |
|--|
| Legend: |
| R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' |
| - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown |

TABLE 6-2: REGISTERS ASSOCIATED WITH THE PWM MODULE

| Addr | Name | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Value on POR | Value on RST |
|------|---------|----------------------------------|-------|---------|---------|-------|-------|-------|-------|--------------|--------------|
| 34h | GPDDR | — | DDR6 | DDR5 | DDR4 | DDR3 | DDR2 | DDR1 | DDR0 | -111 1111 | -111 1111 |
| 05h | T1CON | TMR1ON | — | T1CKPS1 | T1CKPS0 | — | — | DC1B1 | DC1B0 | 0-00 --xx | 0-00 --uu |
| 06h | T2CON | TMR2ON | — | T2CKPS1 | T2CKPS0 | — | — | DC2B1 | DC2B0 | 0-00 --xx | 0-00 --uu |
| 07h | PR1 | Timer 1 Module's Period Register | | | | | | | | 1111 1111 | 1111 1111 |
| 08h | PR2 | Timer 2 Module's Period Register | | | | | | | | 1111 1111 | 1111 1111 |
| 09h | PWM1DCH | DC1B9 | DC1B8 | DC1B7 | DC1B6 | DC1B5 | DC1B4 | DC1B3 | DC1B2 | xxxx xxxx | uuuu uuuu |
| 0Ah | PWM2DCH | DC2B9 | DC2B8 | DC2B7 | DC2B6 | DC2B5 | DC2B4 | DC2B3 | DC2B2 | xxxx xxxx | uuuu uuuu |

Legend: x = unknown, U = unchanged, - = unimplemented read as '0'. Shaded cells are not used by module.

7.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

7.1 Description

The Analog-to-Digital (A/D) module is a four-channel, 10-bit successive approximation type of A/D. The A/D allows conversion of an analog input signal to a corresponding 10-bit number. The four channels are multiplexed on the GP[3:0] pins. The converter is turned off/on via the ADCON0 register and each channel is individually enabled via the ADCON1 control register. The VREF+ and VREF- sources are user-selectable as internal or external. Each channel can be set to one of two conversion modes:

1. Auto-conversion
2. Convert-on-request.

7.2 A/D Module Registers

The A/D module itself has several registers. The registers are:

- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- Transmit-on-Change Register (IOINTEN)
- Compare and Polarity Register (ADCMPnL)
- A/D Result Registers (ADRESnL, ADRESnH)

The ADCON0 register controls the operation of the A/D module, including auto-conversion rate and enable bit. The ADCON1 register enables the A/D function on port pins GP3:GP0, A/D conversion rate and selects the voltage reference source. The IOINTEN register's four least significant bits enable/disable the transmit-on-change function. The ADCMPnL.ADPOL bit sets the polarity (above or below threshold) for the transmit-on-change function.

The result of an A/D conversion is made available to the user within the data field of the Read A/D Registers output message via the CAN bus. This message can be directly requested by another CAN node or be automatically transmitted (TXIDO), as has been described previously.

Additionally, the individual channel results may be read using the "Read Register" command as described in [Section 4.3.1 "Information Request Messages"](#) and as shown in [Table 3-2](#) by addressing the appropriate A/D result register (ADRESnL and ADRESnH).

Note: The GPDDR register controls the direction of the GPIO pins, even when they are being used as analog inputs. The user must ensure that the bits in the GPDDR register are maintained set (input) when using them as analog inputs.

7.3 A/D Conversion Modes

There are two modes of conversion that can be individually selected for each analog channel that has been enabled. These are auto-conversion and conversion-on-request.

7.3.1 AUTO-CONVERSION MODE

If the Auto-conversion mode is selected (STCON), an A/D conversion is performed sequentially for each channel that has been set to Analog Input mode and has been configured for Auto-conversion mode. Conversion starts with AN0 and is immediately followed by AN1, etc. Once the conversion has completed, the value is stored in the analog channel registers for the respective channel.

The rate of the auto-conversion is determined by a timer and prescaler. The formula for determining conversion rates is:

$$(T_{OSC})(1024)(\text{Prescaler rate})$$

Typical conversion rates with a 20 MHz oscillator input are shown in [Table 7-1](#).

TABLE 7-1: AUTO-CONVERSION RATES FOR GIVEN PRESCALE RATES AT 20 MHZ

| TOPS[2:0] | Prescale Rate | Auto-Conversion Rate |
|-----------|---------------|----------------------|
| 000 | 1:1 | 51 μ s |
| 001 | 1:8 | 410 μ s |
| 010 | 1:32 | 2 ms |
| 011 | 1:128 | 7 ms |
| 100 | 1:512 | 26 ms |
| 101 | 1:1024 | 52 ms |
| 110 | 1:2048 | 105 ms |
| 111 | 1:4096 | 210 ms |

The timer is turned on if one of the GPnTXC bits are set in the IOINTEN register and configured as analog input.

The prescaler counter is cleared when the device is reset (RST Reset or Power-on Reset).

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7.3.2 CONVERSION-ON-REQUEST MODE

If the Conversion-on-request mode is selected, the device performs an A/D conversion only after receiving a Read A/D Registers or Read Register Receive message (IRM). In the case of the Read A/D Registers command, all of the GPIO pins that have been configured as analog input channels will have an A/D conversion done before the data frame is sent. When a Read Register Receive message is initiated (extended message format only), the A/D conversion is performed when the MSB of the analog channel is requested, with the MSB result being transferred. A subsequent read of the LSB will transmit the value latched when the MSB was requested (it is recommended that the Read A/D Registers receive message is used to obtain complete analog channel values in one message).

7.4 A/D Threshold Detection

Once an A/D auto-conversion has been completed, the A/D channel result(s) can be compared to a value stored in the associated A/D channel comparator registers.

If the value in the analog channel result registers (i.e., AN0L and AN10H registers for analog channel 0) is lower or higher than the value in the A/D comparator registers (as specified by a corresponding polarity bit), a transmit-on-change message will be sent (TXID2). The threshold-detection function for all analog channels is bit-selectable.

If the A/D channel has been configured for transmit-on-change mode, the MCP2505 will send a transmit message with the appropriate data. It is possible that more than one A/D channel has a change-of-state condition. This does not pose a problem since all analog channel data is provided in the transmit message.

REGISTER 7-1: A/D MODULE RESULT REGISTER MSB (ADRESnH)

| | | | | | | | |
|-------|-----|-----|-----|-----|-----|-----|-------|
| R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| AD9 | AD8 | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 |
| bit 7 | | | | | | | bit 0 |

bit 7-0 **AD9:AD2:** Most Significant A/D Result bits

| | | | |
|--------------------|------------------|------------------------------------|--------------------|
| Legend: | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

REGISTER 7-2: A/D MODULE RESULT REGISTER LSB (ADRESnL)

| | | | | | | | |
|-------|-----|-----|-----|-----|-----|-----|-------|
| R-x | R-x | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| AD1 | AD0 | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

bit 7-6 **AD1:AD0:** Least significant A/D Result bits

bit 5-0 **Unimplemented:** Reads as '0'

| | | | |
|--------------------|------------------|------------------------------------|--------------------|
| Legend: | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

REGISTER 7-3: A/D MODULE COMPARE REGISTER MSB (ADCMP_{NH})

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---------|---------|---------|---------|---------|---------|---------|---------|
| ANnCMP9 | ANnCMP8 | ANnCMP7 | ANnCMP6 | ANnCMP5 | ANnCMP4 | ANnCMP3 | ANnCMP2 |
| bit 7 | | | | bit 0 | | | |

bit 7-0 **ANnCMP9:ANnCMP2:** Most Significant A/D Compare bits

| Legend: | | | |
|--------------------|------------------|------------------------------------|--------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

REGISTER 7-4: A/D MODULE COMPARE REGISTER LSB (ADCMP_{NL})

| R/W-x | R/W-x | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---------|---------|-------|-----|-----|-----|-----|-----|
| ANnCMP1 | ANnCMP0 | — | — | — | — | — | — |
| bit 7 | | bit 0 | | | | | |

bit 7-6 **ANnCMP1:ANnCMP0:** Least Significant A/D Compare bits

bit 5-0 **Unimplemented:** Reads as '0'

| Legend: | | | |
|--------------------|------------------|------------------------------------|--------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

REGISTER 7-5: ADCON0 REGISTER

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-x | U-0 | U-x | U-x |
|-------|-------|-------|-------|-------|-----|-----|-----|
| ADON | T0PS2 | T0PS1 | T0PS0 | — | — | — | — |
| bit 7 | | | | bit 0 | | | |

bit 7 **ADON:** A/D On Bit

1 = A/D converter module is operating

0 = A/D converter module is shut off and consumes no operating current

bit 6-4 **T0PS2:T0PS0:** Timer0 Prescaler Rate Select bits (used for auto-conversions)

000 = 1:1 Prescaler Rate

001 = 1:8 Prescaler Rate

010 = 1:32 Prescaler Rate

011 = 1:128 Prescaler Rate

100 = 1:512 Prescaler Rate

101 = 1:1024 Prescaler Rate

110 = 1:2048 Prescaler Rate

111 = 1:4096 Prescaler Rate

Formula: (Tosc)(1024) (Prescaler Rate)

bit 3 **Reserved**

bit 2 **Unimplemented:** Reads as '0'

bit 1-0 **Reserved**

| Legend: | | | |
|--------------------|------------------|------------------------------------|--------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

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REGISTER 7-6: ADCON1 REGISTER

| | | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | |
| ADCS1 | ADCS0 | VCFG1 | VCFG0 | PCFG3 | PCFG2 | PCFG1 | PCFG0 | |
| bit 7 | | | | | | | | bit 0 |

bit 7-6 **ADCS1:ADCS0:** A/D Conversion Select bits

- 00 = Fosc/2
- 01 = Fosc/8
- 10 = Fosc/32
- 11 = Reserved

bit 5-4 **VCFG1:VCFG0:** Voltage Reference Configuration bits

| VCFG1:VCFG0 | A/D VREF+ | A/D VREF- |
|-------------|----------------|----------------|
| 00 | VDD | VSS |
| 01 | External VREF+ | VSS |
| 10 | VDD | External VREF- |
| 11 | External VREF+ | External VREF- |

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits*

- 1 = Corresponding GPIO pin configured as Digital I/O
- 0 = Corresponding GPIO pin configured as A/D Input

* corresponding data direction bit (GPDDR register) must be set for each enabled analog channel.

Legend:

| | | |
|--------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

7.5 Read A/D Registers Output Message

When the MCP2502X/5X responds to a Read A/D Regs IRM with an OM, the analog values are contained in [Register 7-7](#), [Register 7-8](#) and [Register 7-9](#).

REGISTER 7-7: A/D OM RESULT REGISTER (ANnH)

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| ANnR9 | ANnR8 | ANnR7 | ANnR6 | ANnR5 | ANnR4 | ANnR3 | ANnR2 |
| | | | | | | | bit 0 |

bit 7-0 **ANnR9:ANnR2:** Bits 9-2 of channel 'n' results

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 7-8: A/D OM RESULT REGISTER (AN32L)

| | | | | | | | |
|--------|--------|-----|-----|--------|--------|-----|-------|
| R-x | R-x | U-x | U-x | R-x | R-x | U-x | U-x |
| AN3R.1 | AN3R.0 | — | — | AN2R.1 | AN2R.0 | — | — |
| | | | | | | | bit 0 |

bit 7-6 **AN3R.1:AN3R.0:** A/D Channel 3, bits 1:0 results

bit 5-4 **Unimplemented:** Reads as '0'

bit 3-2 **AN2R.1:AN2R.0:** A/D Channel 2, bits 1:0 results

bit 1-0 **Unimplemented:** Reads as '0'

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

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REGISTER 7-9: A/D OM RESULT REGISTER (AN10L)

| | | | | | | | |
|--------|--------|-----|-----|--------|--------|-----|-----|
| R-x | R-x | U-x | U-x | R-x | R-x | U-x | U-x |
| AN1R.1 | AN1R.0 | — | — | AN0R.1 | AN0R.0 | — | — |
| bit 7 | | | | bit 0 | | | |

- bit 7-6 **AN1R.1:AN1R.0:** A/D Channel 1, bits 1:0 results
- bit 5-4 **Unimplemented:** Reads as '0'
- bit 3-2 **AN0R.1:AN0R.0:** A/D Channel 0, bits 1:0 results
- bit 1-0 **Unimplemented:** Reads as '0'

| | | | |
|--------------------|------------------|------------------------------------|--------------------|
| Legend: | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

TABLE 7-2: REGISTERS ASSOCIATED WITH THE A/D MODULE

| Addr | Name | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Value on POR | Value on RST |
|------|---------|--------|---------|---------|---------|----------|----------|---------|---------|--------------|--------------|
| 1Eh | GPPIN | GP7 | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | 0000 0000 | 0000 0000 |
| 34h | GPDDR * | — | DDR6 | DDR5 | DDR4 | DDR3 | DDR2 | DDR1 | DDR0 | -111 1111 | -111 1111 |
| 00h | IOINTEN | GP7TXC | GP6TXC | GP5TXC | GP4TXC | GP3TXC | GP2TXC | GP1TXC | GP0TXC | 0000 0000 | 0000 0000 |
| 01h | IOINTPO | GP7POL | GP6POL | GP5POL | GP4POL | GP3POL | GP2POL | GP1POL | GP0POL | 0000 0000 | 0000 0000 |
| 0Eh | ADCON0 | ADON | T0PS2 | T0PS1 | T0PS0 | GO/DONE | — | CHS1 | CHS0 | 0000 0-00 | 0000 0-00 |
| 0Fh | ADCON1 | ADCS1 | ADCS0 | VCFG1 | VCFG0 | PCFG3 | PCFG2 | PCFG1 | PCFG0 | 0000 0000 | 0000 0000 |
| 2Ch | ADC- | AN3CM | AN3CMP. | AN3CMP. | AN3CMP. | AN3CMP.5 | AN3CMP.4 | AN3CMP. | AN3CMP2 | xxxx xxxx | uuuu uuuu |
| 2Dh | ADC- | AN3CM | AN3CMP. | — | — | Reserved | | | ADPOL | xx-- ---- | uu-- ---- |
| 2Eh | ADC- | AN2CM | AN2CMP. | AN2CMP. | AN2CMP. | AN2CMP.5 | AN2CMP.4 | AN2CMP. | AN2CMP2 | xxxx xxxx | uuuu uuuu |
| 2Fh | ADC- | AN2CM | AN2CMP. | — | — | Reserved | | | ADPOL | xx-- ---- | uu-- ---- |
| 30h | ADC- | AN1CM | AN1CMP. | AN1CMP. | AN1CMP. | AN1CMP.5 | AN1CMP.4 | AN1CMP. | AN1CMP2 | xxxx xxxx | uuuu uuuu |
| 31h | ADC- | AN1CM | AN1CMP. | — | — | Reserved | | | ADPOL | xx-- ---- | uu-- ---- |
| 32h | ADC- | AN0CM | AN0CMP. | AN0CMP. | AN0CMP. | AN0CMP.5 | AN0CMP.4 | AN0CMP. | AN0CMP2 | xxxx xxxx | uuuu uuuu |
| 33h | ADC- | AN0CM | AN0CMP. | — | — | Reserved | | | — | xx-- ---- | uu-- ---- |
| 10h | STCON | STEM | STMS | STBF1 | STBF0 | STM3 | STM2 | STM1 | STM0 | 0xxx xxxx | 0uuu uuuu |

* The GPDDR register controls the direction of the GPIO pins, even when they are being used as analog inputs. The user must ensure that the bits in the GPDDR register are maintained **set** (input) when using them as analog inputs.

8.0 SPECIAL FEATURES OF THE MCP2502X/5X

8.1 Description

There are a number of special circuits in the MCP2502X/5X that deal with the needs of real-time applications. These features are intended to maximize system reliability, minimize cost through elimination of external components and provide power-saving operating modes. These are:

- Oscillator selection
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
- SLEEP
- In-Circuit Serial Programming

Several oscillator options are offered to allow the device to fit the application. XT and HS modes allow the device to support a wide range of crystal frequencies while the LP crystal option saves power.

Two timers are implemented to offer necessary delays on Power-up. One is the Oscillator Start-up Timer (OST), intended to keep the device in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on Power-up only, designed to keep the part in Reset while the power supply stabilizes. With these two timers on-chip, most applications do not need any external Reset circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can wake-up from SLEEP through external Reset, transmit-on-change or CAN bus activity.

A set of Configuration bits are used to select various options.

FIGURE 8-1: CRYSTAL/CERAMIC RESONATOR OPERATION

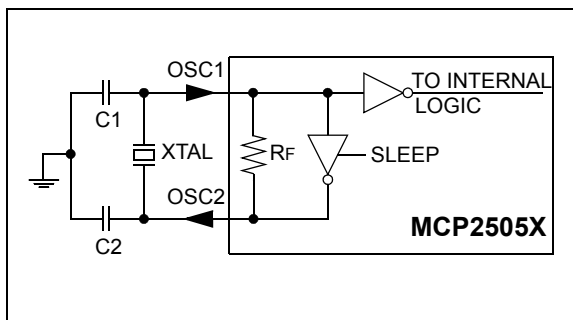
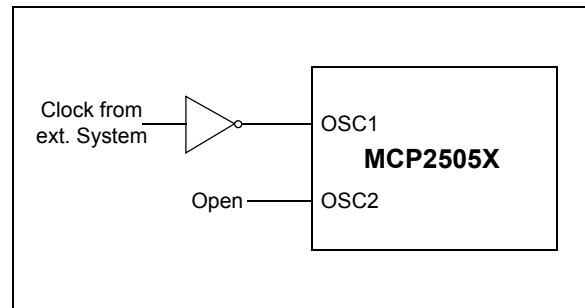


FIGURE 8-2: EXTERNAL CLOCK INPUT OPERATION



8.2 Configuration Bits

The Configuration bits can be either programmed (read as '0') or unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h. The Configuration register is actually beyond program memory space and belongs to the special test/Configuration memory space (2000h-3FFFh) that can be accessed only during programming.

8.3 Oscillator Configurations

Four different oscillator modes can be selected. The user can program two Configuration bits ($F_{OSC1}:F_{OSC0}$) in the CONFIG register to select one of these modes:

- LP = Low-Power Crystal
- XT = Crystal/Resonator
- HS = High-speed Crystal Resonator

In all modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 8-1). The oscillator design requires the use of a parallel-cut crystal. The device can also have an external clock source to drive the OSC1/CLKIN pin (Figure 8-2).

The device will default to HS mode if the CONFIG register is not programmed.

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REGISTER 8-1: CONFIGURATION REGISTER

| | | | | | | | | | |
|--------|-----|-------|-------|-------|-------|-------|-------|-------|-------|
| U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | | | | |
| — | — | R | R | R | R | | | | |
| bit 13 | | | | | | | | bit 8 | |
| | | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W | R/W | R/W |
| | | R | R | R | R | R | RSTEN | FOSC1 | FOSC0 |
| | | bit 7 | | | | | | bit 0 | |

- bit 13-11 **Unimplemented:** Read as '0'
- bit 10-3 **Reserved:** do not attempt to modify
- bit 2 **RSTEN:** Enable RST input on GP7
1 = $\overline{\text{RST}}$ input Enabled
0 = RST input Disabled
- bit 1-0 **Fosc1:Fosc0:** Oscillator Selection bits
11 = HS oscillator
10 = Reserved for Test (EC oscillator)
01 = XT oscillator
00 = LP oscillator

| | | | |
|--------------------|------------------|------------------------------------|--------------------|
| Legend: | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

8.4 Reset

The MCP2502X/5X differentiates between two kinds of Reset:

- Power-on Reset (POR)
- External $\overline{\text{RST}}$ Reset

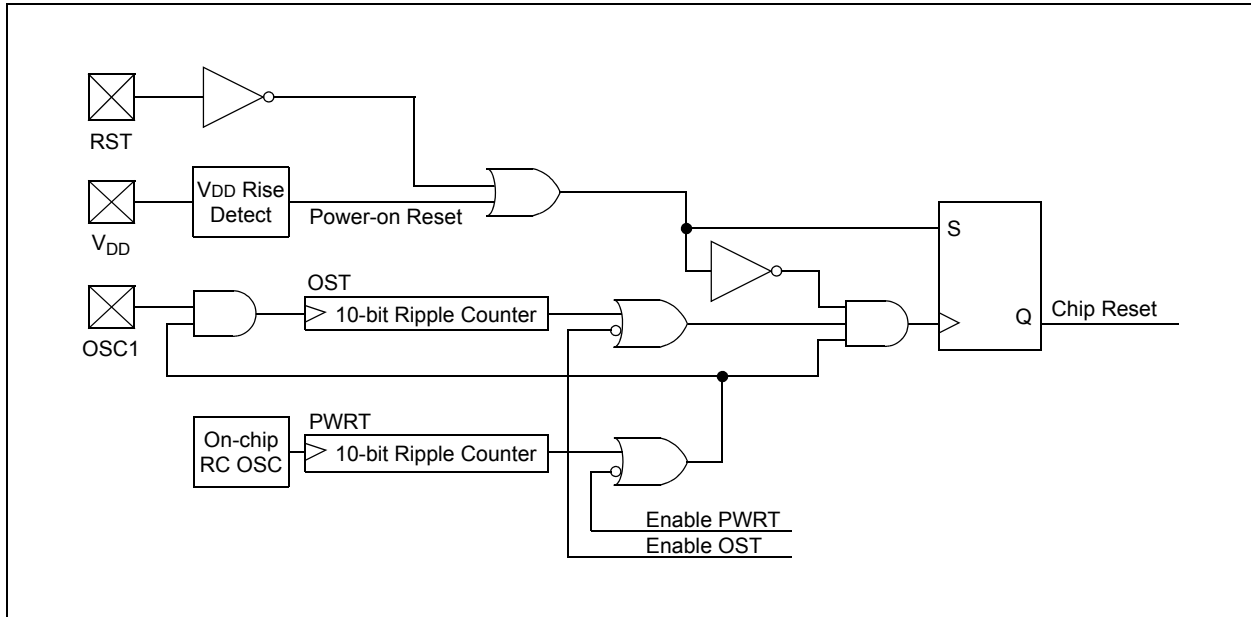
Some registers are not affected in any Reset condition. Their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a Reset state on Power-on Reset (POR), on $\overline{\text{RST}}$ and on $\overline{\text{RST}}$ during SLEEP. They are not affected by a wake-up from SLEEP, which is viewed as the resumption of normal operation. A simplified block diagram of the on-chip Reset circuit is shown in Figure 8-3. The MCP2502X/5X has a RST noise filter in the RST Reset path. The filter will detect and ignore small pulses.

8.4.1 POWER-ON RESET

A Power-on Reset pulse is generated on-chip when V_{DD} rise is detected (in the range of 1.5V to 2.1V). If the $\overline{\text{RST}}$ input on the GP7 pin is selected, the $\overline{\text{RST}}$ pin may be tied through a series resistor to V_{DD} , eliminating the need for external RC components usually required for a Power-on Reset. A maximum rise time for V_{DD} is specified in Section 9.0 "Electrical Characteristics" of this document.

When the device starts normal operation (exits the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure proper operation. For additional information, refer to AN607, *Power-up Trouble Shooting Application Note*, DS00000607).

FIGURE 8-3: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



8.4.2 POWER-UP TIMER

The Power-up Timer (PWRT) provides a fixed, 72 ms nominal time-out, on Power-up only, from the POR. The Power-up Timer operates on an internal RC oscillator, with the device being kept in Reset as long as the PWRT is active. The PWRT's time delay allows V_{DD} to rise to an acceptable level. The Power-up time delay will vary from device to device due to V_{DD} , temperature and process variation. For more information, please see [Section 9.2 "DC Characteristics"](#).

8.5 Oscillator Start-up Timer

The Oscillator Start-up Timer (OST) provides a 512 oscillator cycle (T_{osc}) delay after the PWRT delay is complete. This ensures that the crystal oscillator has started and stabilized and must be less than the total time it takes (704 oscillator cycles or 44 T_Q) for the minimum standard data frame or remote transmit message to be completed on the CAN bus once a wake-up from SLEEP occurs. The OST time-out is invoked only on Power-on Reset or wake-up from SLEEP.

8.6 Power-down Mode (SLEEP)

Power-down mode (or SLEEP) is enabled via the SLPEN bit in the OPTREG2 register. When enabled, the MCP2502X/5X will enter SLEEP once the CAN bus has been idle for a minimum 1408 bit times while in Normal mode.

Additionally, the device may be configured to enter SLEEP while in Listen-only mode immediately after Power-up if there is no activity on the CAN bus. Subsequent CAN bus activity will wake the device up from SLEEP and the NEXT message will be confirmed

as a valid message before entering Normal mode. This feature is enabled via the PUSLIP bit in the OPTREG2 register.

While in SLEEP, the I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, low or hi-impedance).

The following operations will not function while the device is in SLEEP:

- A/D Module data conversion
- Auto-conversion mode
- Auto-messaging
- PWM module and outputs
- Clock output

8.6.1 WAKE-UP FROM SLEEP

The MCP2502X/5X can wake-up from SLEEP through one of the following events:

- External Reset input on \overline{RST} pin
- Transmit-on-change due to edge detected on GPIO pin
- Activity detected on CAN bus

For the device to wake-up due to a GPIO transmit-on-change, the corresponding interrupt enable bit must be set (enabled). Wake-up occurs regardless of the state of the GIE bit.

If a wake-up from SLEEP is caused by activity on the CAN bus, the message that caused the wake-up will not be received or acknowledged by the MCP2502X/5X.

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8.7 In-Circuit Serial Programming

The MCP2502X/5X can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product, also allowing the most recent firmware (or a custom firmware) to be programmed.

The device is placed into a Program/Verify mode by holding the GP4 and GP5 pins low while raising GP7 (VPP) pin from V_{IL} to V_{IH} . See the MCP2502X/5X programming specification, *MCP250XX Development Kit User's Guide*, DS20072, for more information. GP4 becomes the programming data and GP5 becomes the programming clock. Both GP4 and GP5 are Schmitt Trigger inputs in this mode. The signal definitions are summarized in [Table 8-1](#)

TABLE 8-1: IN-CIRCUIT SERIAL PROGRAMMING PIN FUNCTIONS

| Pin Name | Pin Number | Programming Mode Function |
|----------|------------|---------------------------|
| VSS | 7 | Ground |
| GP4 | 5 | Data |
| GP5 | 6 | Clock |
| GP7 | 11 | VPP |
| VDD | 14 | Power |

9.0 ELECTRICAL CHARACTERISTICS

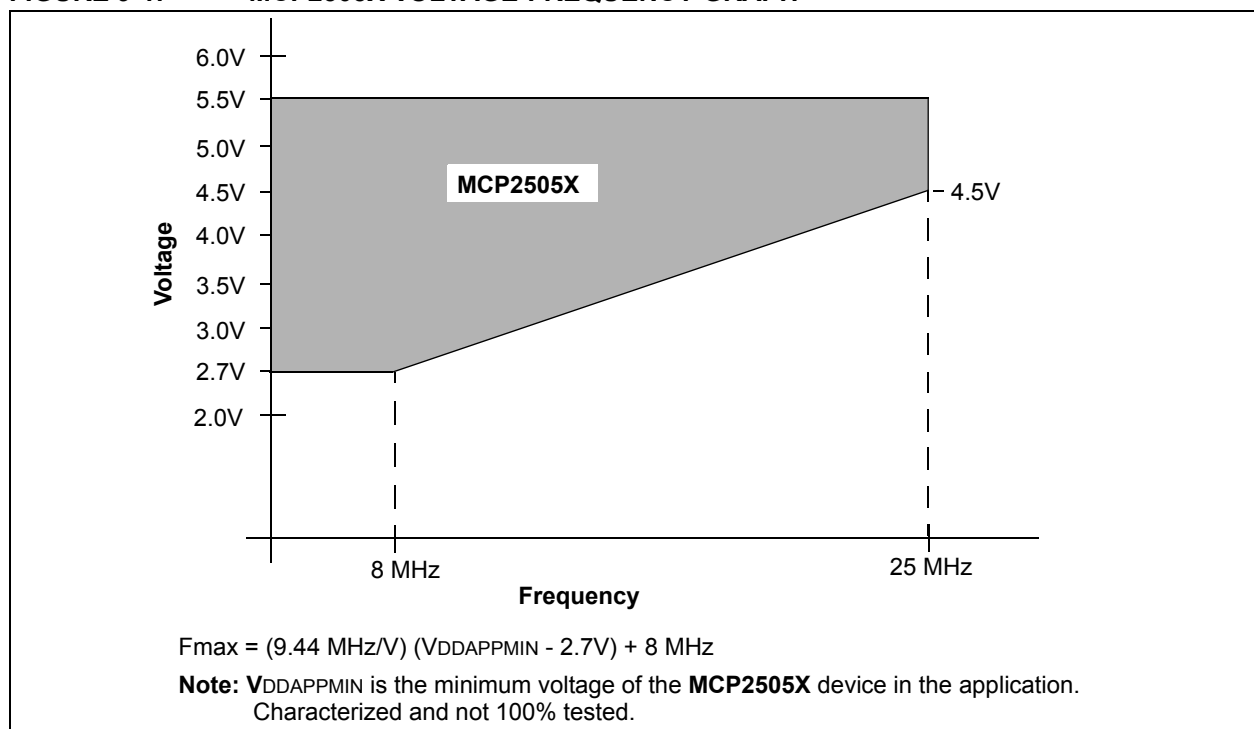
9.1 Absolute Maximum Ratings†

| | |
|---|-----------------------|
| Ambient temperature under bias..... | -55°C to +125°C |
| Storage temperature..... | -65°C to +150°C |
| Voltage on any pin with respect to Vss (except VDD and $\overline{\text{RST}}$)..... | -0.3V to (VDD + 0.6V) |
| VDD..... | 0V to 7.0V |
| Voltage on $\overline{\text{RST}}$ with respect to Vss..... | 0V to 14V |
| Total power dissipation (Note 1)..... | 1.0 W |
| Maximum source current out of Vss pin..... | 300 mA |
| Maximum sink current into VDD pin..... | 250 mA |
| Input clamp current, I _{ik} (V _i < 0 or V _i > VDD)..... | ±20 mA |
| Output clamp current, I _{ok} (V _o < 0 or V _o > VDD)..... | ±20 mA |
| Maximum current sunk by any I/O pin..... | 25 mA |
| Maximum current sourced by any input pin..... | 25 mA |
| Maximum current sunk by GPIO port..... | 200 mA |
| Maximum current sourced by GPIO port..... | 200 mA |
| Soldering temperature of leads (10 seconds)..... | +300°C |
| ESD protection on all pins..... | ≥ 3.5 kV |

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIGURE 9-1: MCP2505X VOLTAGE-FREQUENCY GRAPH



MCP2502X/5X

9.2 DC Characteristics

| DC Characteristics | | | Industrial (I): T _{AMB} = -40°C to +85°C V _{CC} = 2.7V to 5.5V Automotive (E): T _{AMB} = -40°C to +125°C V _{CC} = 4.5V to 5.5V | | | |
|--------------------|---|---|---|--|--------------------|---|
| Param. No. | Sym | Characteristics | Min | Max | Units | Test Conditions |
| | V _{DD} | Supply Voltage | 2.7 4.5 | 5.5 5.5 | V V | XT and LP OSC Configuration HS OSC Configuration (Note 2) |
| | SVDD | V _{DD} Rise Rate to ensure internal Power-on Reset signal | 0.05 | — | V/ms | (Note 3) |
| | V _{IH} V _{IH} V _{IH} | High-level input voltage GPIO pins RXCAN (Schmitt Trigger) OSC1 | 2 .7 V _{DD} .85 V _{DD} | V _{DD} +0.3 V _{DD} V _{DD} | V V V | |
| | V _{IL} V _{IL} V _{IL} | Low-level input voltage RXCAN (Schmitt Trigger) GPIO pins OSC1 | V _{SS} -0.3 V _{SS} | 0.2 V _{DD} 0.5V 0.2 V _{DD} | V V V | |
| | V _{OL} V _{OH} ILI | Low-level output voltage TXCAN GPIO pins High-level output voltage TXCAN, GPIO pins Input leakage current All I/O except OSC1, GP7 OSC1, GP7 pin | V _{DD} -0.7 -1 -5 | 0.6 — +1 +5 | V V μA μA | I _{OL} = 8.5 mA, V _{DD} = 4.5V I _{OH} = -3.0 mA, V _{DD} = 4.5V, I-temp |
| | C _{INT} | Internal Capacitance (all inputs and outputs, except GP7) GP7 | — — | 7 15 | pF pF | T _{AMB} = 25°C, f _c = 1.0 MHz, V _{DD} = 5.0V (Note 3) |
| | I _{DD} | Operating Current | — | 20 | mA | XT OSC V _{DD} = 5.5V; F _{OSC} = 25 MHz |
| | I _{DDS} | Standby Current (CAN Sleep Mode) | — | 30 | μA | Inputs tied to V _{DD} or V _{SS} |

Note 1: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

2: Refer to [Figure 9-1](#).

3: This parameter is periodically sampled and not 100% tested.

9.3 AC Characteristics

| AC Characteristics | | | Industrial (I): T _{AMB} = -40°C to +85°C V _{CC} = 2.7V to 5.5V Automotive (E): T _{AMB} = -40°C to +125°C V _{CC} = 4.5V to 5.5V | | | |
|--------------------|--------------|--|---|-----|-------|---|
| Param. No. | Sym | Characteristics | Min | Max | Units | Test Conditions |
| | Fos | CLKIN Frequency | DC | 4 | MHz | XT osc mode |
| | | | DC | 25 | MHz | HS osc mode (Note 3) |
| | | | DC | 200 | kHz | LP osc mode |
| | Fos | Oscillator Frequency | 0.1 | 4 | MHz | XT osc mode |
| | | | 4 | 25 | MHz | HS osc mode (Note 3) |
| | | | 5 | 200 | kHz | LP osc mode |
| 1 | Tosc | CLKIN Period | 250 | — | ns | XT osc mode |
| | | | 40 | — | ns | HS osc mode |
| | | | 5 | — | µs | LP osc mode |
| | | Oscillator Period | 0.25 | 10 | µs | XT osc mode |
| | | | 40 | 250 | ns | HS osc mode |
| | | | 5 | — | µs | LP osc mode |
| 3 | TOSL TOSH | CLKIN High or Low Time | 100 | — | ns | XT osc mode |
| | | | 15 | — | ns | HS osc mode |
| | | | 2.5 | — | µs | LP osc mode |
| 4 | Tosr | CLKIN Rise or Fall Time | — | 25 | ns | XT osc mode (Note 1) |
| | | | — | 50 | ns | HS osc mode (Note 1) |
| | | | — | 15 | ns | LP osc mode (Note 1) |
| 10 | TdCLKOUT | CLKOUT Propagation Delay | — | 60 | ns | V _{DD} = 4.5 V (Note 2) |
| 12 | TCKR | CLKOUT Rise Time | — | 100 | ns | Note 2 |
| 13 | TCKR | CLKOUT Fall Time | — | 200 | ns | Note 2 |
| 20 | TioR | Port output rise time | — | 40 | ns | Note 1 |
| 21 | TioF | Port output fall time | — | 40 | ns | Note 1 |
| 30 | TMCL | RST Pulse Low | 2 | — | µs | V _{DD} = 5V |
| 32 | TOST | Oscillation Start-up Timer | 512 | — | Tosc | Tosc = OSC1 period |
| 33 | TPWRT | Power-up Timer | 28 | 132 | ms | V _{DD} = 5V |
| 34 | TioZ | I/O Hi-impedance from RST low | — | 2.1 | µs | Note 1 |
| | TPWMR | PWM output rise time | — | 25 | ns | Note 1 |
| | TPWMF | PWM output fall time | — | 25 | ns | Note 1 |
| | TAD | A/D clock period | 1.6 | — | µs | V _{REFA} ≥ 2.5V |
| | | | 3.0 | — | µs | V _{REF} full range |
| | TCNV | Conversion Time (not including acquisition time) | — | 13 | TAD | |

- Note 1:** This parameter is periodically sampled and not 100% tested.
Note 2: Measurements are taken with CLKOUT output configured as 4 x Tosc.
Note 3: Refer to [Figure 9-1](#).

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FIGURE 9-2: I/O TIMING

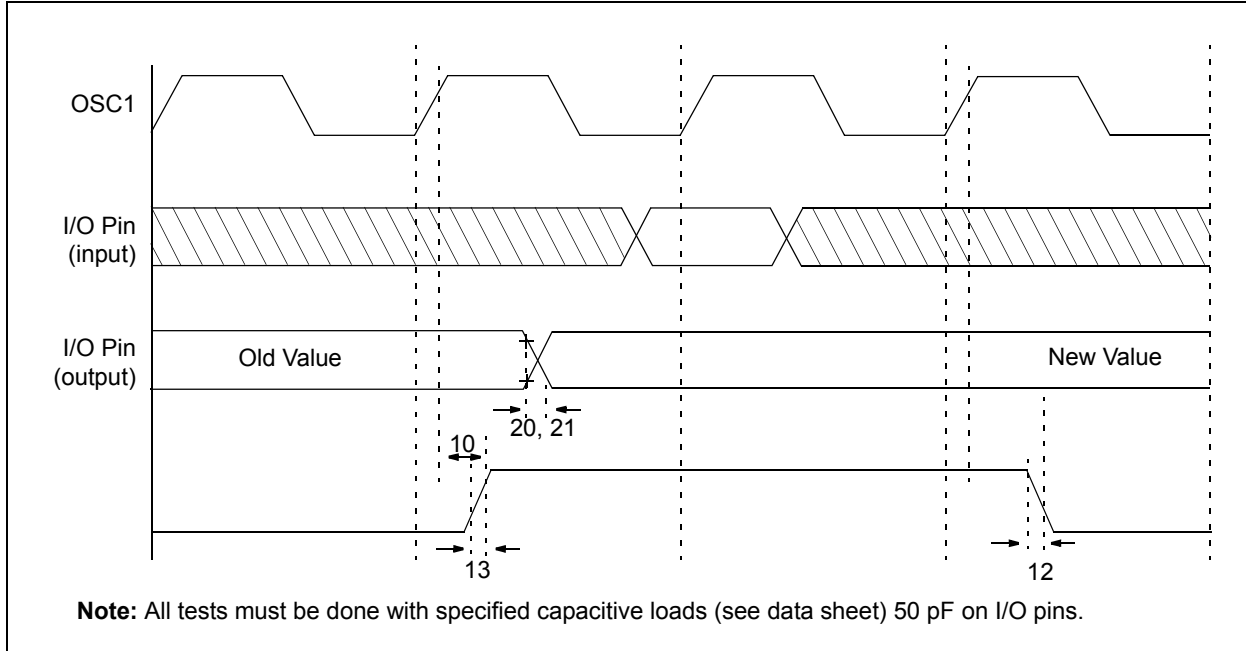
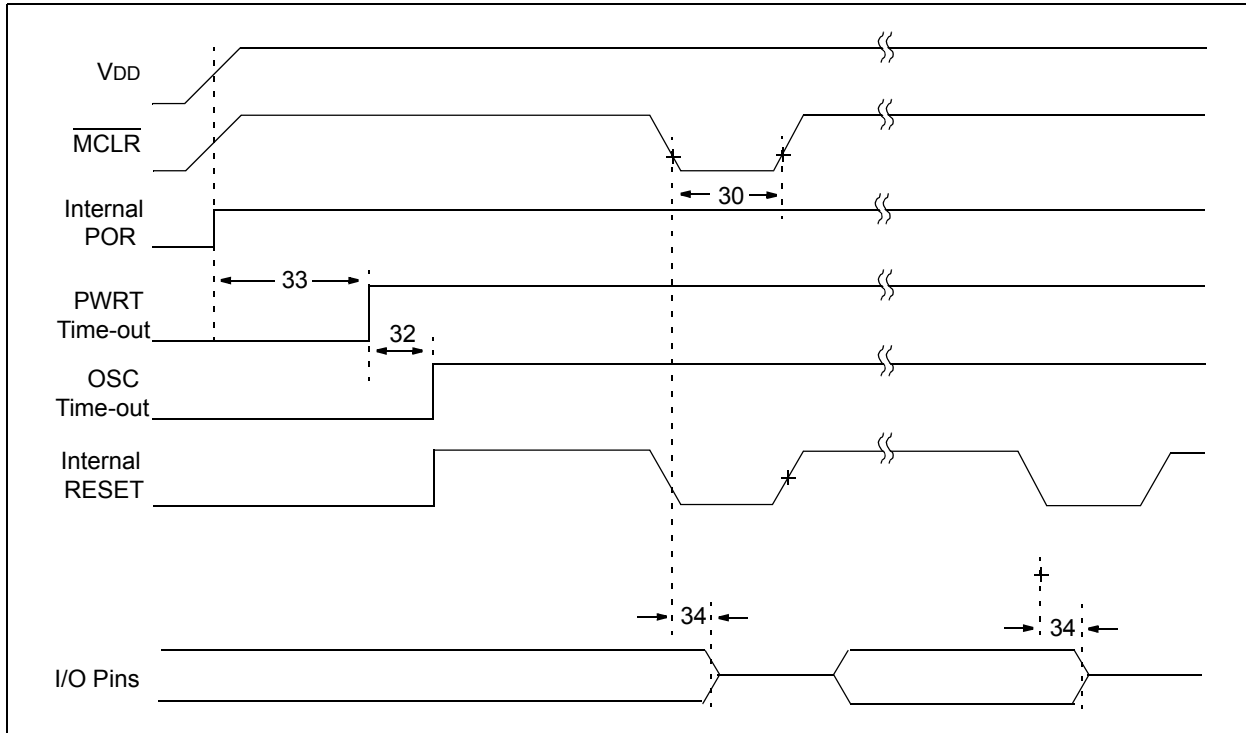


FIGURE 9-3: RESET, OST AND POWER-UP TIMER



9.4 A/D Converter Characteristics

| AC Converter Characteristics | | | Industrial (I): T _{AMB} = -40°C to +85°C V _{CC} = 2.7V to 5.5V Automotive (E): T _{AMB} = -40°C to +125°C V _{CC} = 4.5V to 5.5V | | | |
|------------------------------|-------|--|---|----------------------|-------|--|
| Param. No. | Sym | Characteristics | Min | Max | Units | Test Conditions |
| | NR | A/D resolution | — | 10-bits | | V _{REF} = V _{DD} = 5.12V, V _{SS} ≤ in ≤ V _{REF} |
| | NINT | A/D Integral error | — | less than ±1 LSb | | V _{REF+} = V _{DD} = 5.12V, V _{SS-} = V _{SS} = 0 V (I TEMP) |
| | NDIF | A/D Differential error | — | less than ±1 LSb | | V _{REF+} = V _{DD} = 5.12V, V _{SS-} = V _{SS} = 0 V (I TEMP) |
| | NG | A/D Gain error | — | less than ±1 LSb | | V _{REF+} = V _{DD} = 5.12V, V _{SS-} = V _{SS} = 0 V |
| | NOFF | A/D Offset error | — | less than ±2 LSb | | V _{REF+} = V _{DD} = 5.12V, V _{SS-} = V _{SS} = 0 V |
| | | Monotonicity | — | — | | V _{SS} ≤ in ≤ V _{REF} |
| | VREF | Reference Voltage | 4.096 | V _{DD} +0.3 | V | Absolute minimum to ensure 10-bit accuracy. |
| | VREF+ | Reference V high | VREF- | V _{DD} +0.3 | V | Minimum resolution for A/D is 1 mV. |
| | VREF- | Reference V low | V _{SS} -0.3 | VREF+ | V | Minimum resolution for A/D is 1 mV. |
| | VAIN | Analog input V | VREF- | VREF+ | V | |
| | ZAIN | Recommended impedance of analog voltage source | — | 2.5 | kΩ | Note |
| | IREF | VREF input current | — | 10 | μA | |
| | NHYS | Analog Transmit-on-change Hysteresis | — | 2 LSb | | Specified by design (see Section 4.5.2.1 “Hysteresis Function”) |

Note: Design guidance only

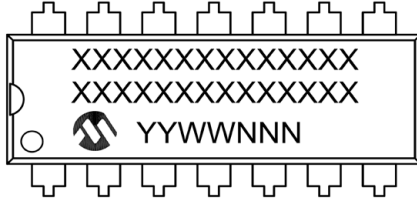
MCP2502X/5X

NOTES:

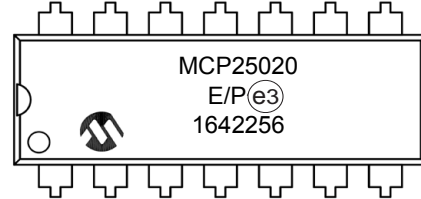
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

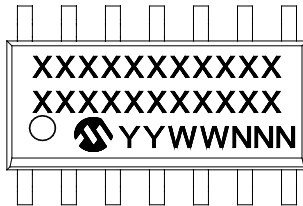
14-Lead PDIP (300 mil)



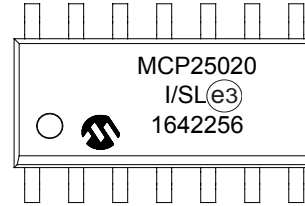
Example:



14-Lead SOIC (208 mil)



Example:



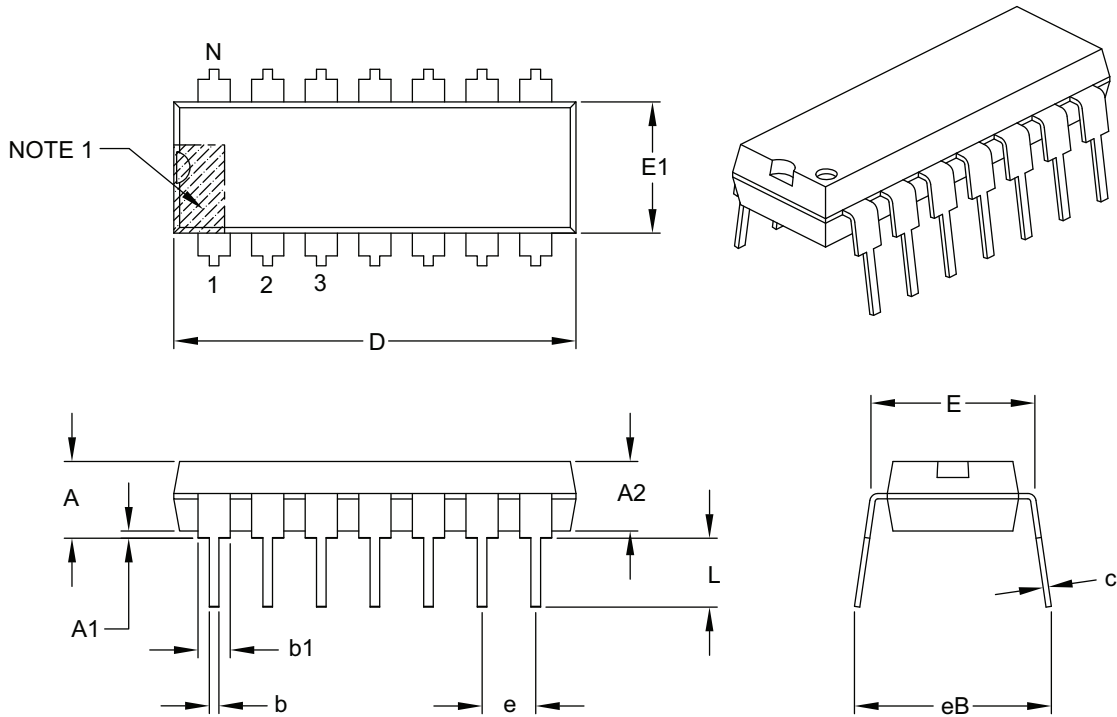
| | | |
|----------------|--------|--|
| Legend: | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

MCP2502X/5X

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| | | Units | INCHES | | |
|----------------------------|----|-------|----------|------|------|
| Dimension Limits | | | MIN | NOM | MAX |
| Number of Pins | N | | 14 | | |
| Pitch | e | | .100 BSC | | |
| Top to Seating Plane | A | – | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 | |
| Base to Seating Plane | A1 | .015 | – | – | |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 | |
| Molded Package Width | E1 | .240 | .250 | .280 | |
| Overall Length | D | .735 | .750 | .775 | |
| Tip to Seating Plane | L | .115 | .130 | .150 | |
| Lead Thickness | c | .008 | .010 | .015 | |
| Upper Lead Width | b1 | .045 | .060 | .070 | |
| Lower Lead Width | b | .014 | .018 | .022 | |
| Overall Row Spacing § | eB | – | – | – | .430 |

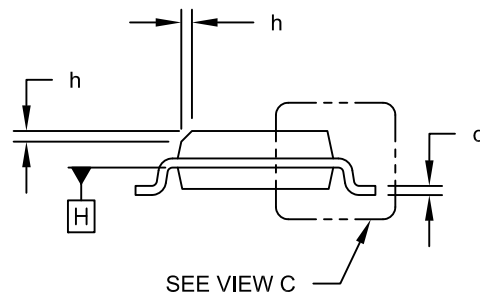
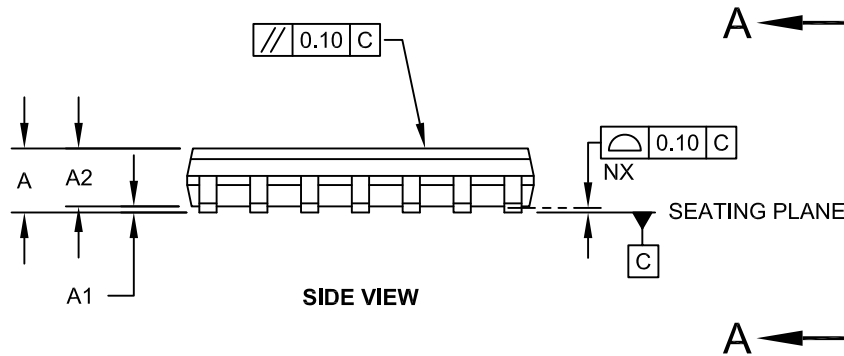
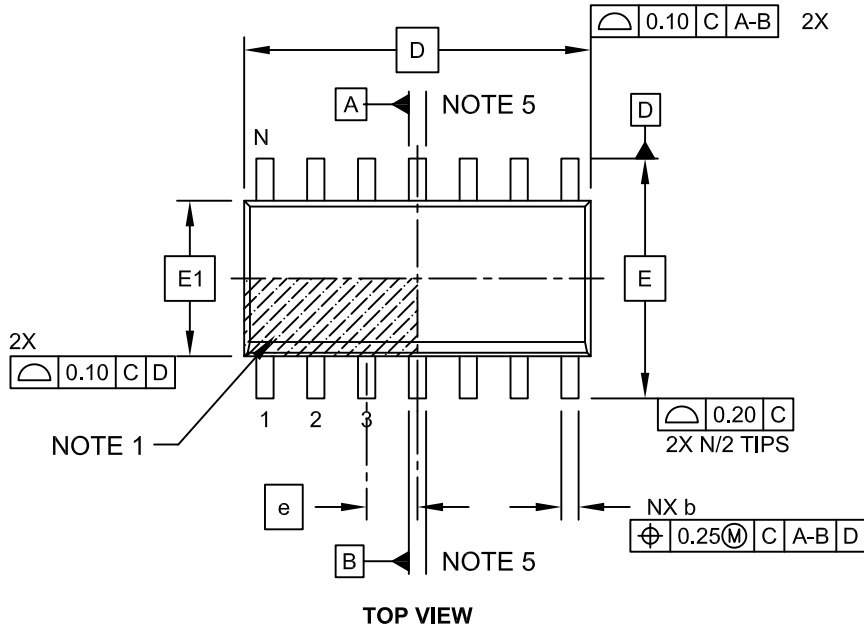
Notes:

- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

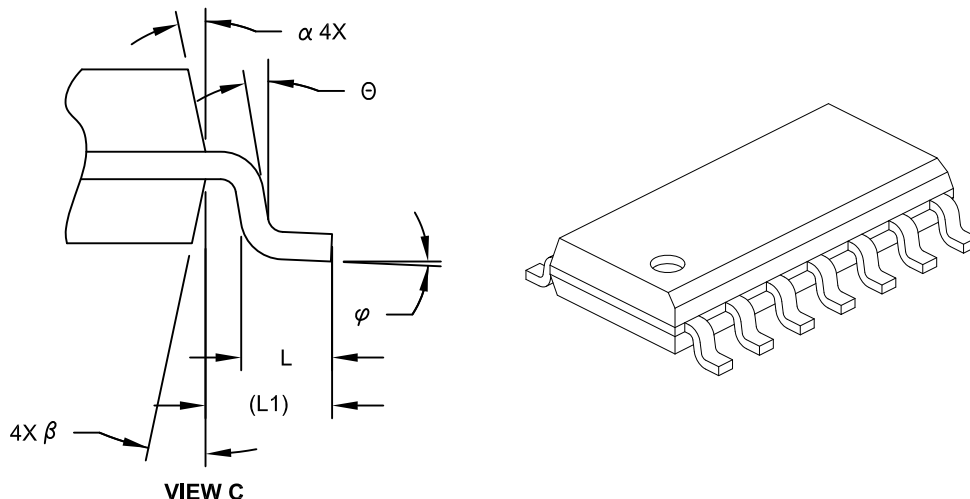


Microchip Technology Drawing No. C04-065C Sheet 1 of 2

MCP2502X/5X

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| | | MILLIMETERS | | |
|--------------------------|----|-------------|-----|------|
| Units | | MIN | NOM | MAX |
| Dimension Limits | | | | |
| Number of Pins | N | 14 | | |
| Pitch | e | 1.27 BSC | | |
| Overall Height | A | - | - | 1.75 |
| Molded Package Thickness | A2 | 1.25 | - | - |
| Standoff § | A1 | 0.10 | - | 0.25 |
| Overall Width | E | 6.00 BSC | | |
| Molded Package Width | E1 | 3.90 BSC | | |
| Overall Length | D | 8.65 BSC | | |
| Chamfer (Optional) | h | 0.25 | - | 0.50 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | 1.04 REF | | |
| Lead Angle | Θ | 0° | - | - |
| Foot Angle | φ | 0° | - | 8° |
| Lead Thickness | c | 0.10 | - | 0.25 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | α | 5° | - | 15° |
| Mold Draft Angle Bottom | β | 5° | - | 15° |

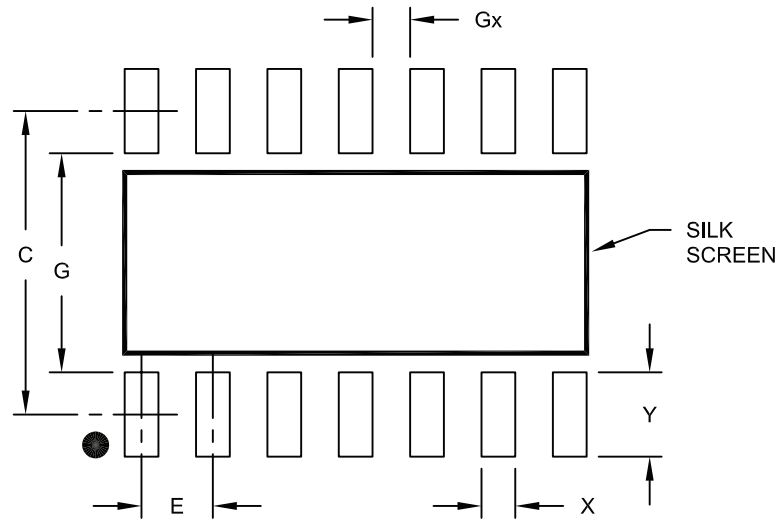
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|-----------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 1.27 BSC | | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width | X | | | 0.60 |
| Contact Pad Length | Y | | | 1.50 |
| Distance Between Pads | Gx | 0.67 | | |
| Distance Between Pads | G | 3.90 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

MCP2502X/5X

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | /XX |
|---------------------------|--------------------------|---|
| Device | Temperature Range | Package |
| Device: | | |
| | MCP25020: | CAN I/O Expander |
| | MCP25020T: | CAN I/O Expander (Tape and Reel) |
| | MCP25025: | CAN I/O Expander |
| | MCP25025T: | CAN I/O Expander (Tape and Reel) |
| | MCP25050: | Mixed Signal CAN I/O Expander |
| | MCP25050T: | Mixed Signal CAN I/O Expander (Tape and Reel) |
| | MCP25055: | Mixed Signal CAN I/O Expander |
| | MCP25055T: | Mixed Signal CAN I/O Expander (Tape and Reel) |
| Temperature Range: | I = | -40°C to +85°C |
| | E = | -40°C to +125°C (not available on MCP25025 or MCP25055 devices) |
| Package: | P = | Plastic DIP (300 mil Body), 14-lead |
| | SL = | Plastic SOIC (150 mil Body), 14-lead |

Examples:

- a) MCP25020-I/P: Industrial temperature, PDIP package.
- b) MCP25025-I/SL: Industrial temperature, SOIC package.
- c) MCP25050T-E/SL: Tape and Reel, Extended temperature, SOIC package.
- d) MCP25055-I/SL: Industrial temperature SOIC package.

MCP2502X/5X

NOTES:

APPENDIX A: REVISION HISTORY

Revision E (March 2017)

The following is the list of modifications:

1. Added note to page 1 header: "Not recommended for new designs".
2. Updated [Section 10.1 "Package Marking Information"](#).
3. Minor typographical corrections.

Revision D (January 2007)

This revision includes updates to the packaging diagrams.

NOTES:

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