Micro Linear

ML2035

Serial Input Programmable Sine Wave Generator

GENERAL DESCRIPTION

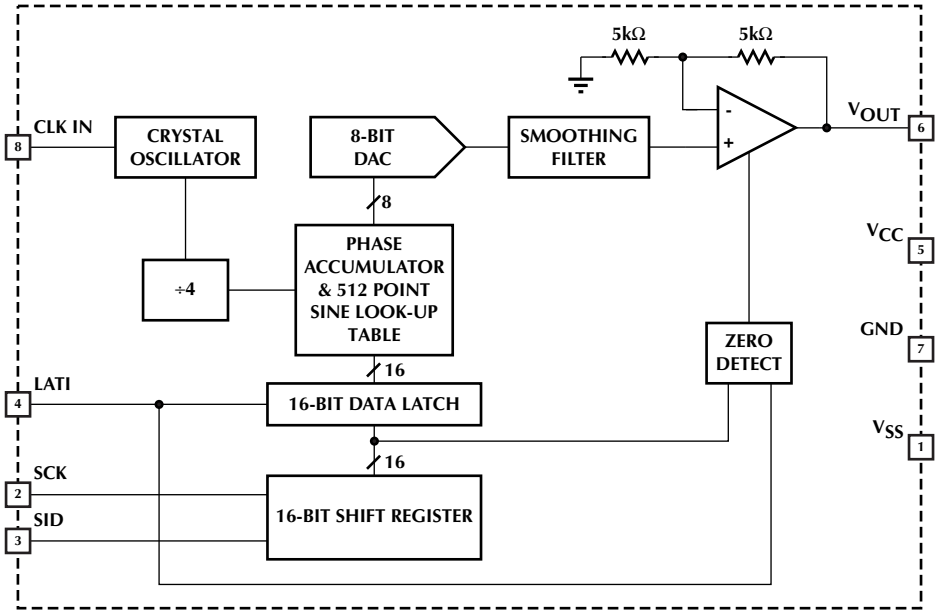
The ML2035 is a monolithic sinewave generator whose output is programmable from DC to 25kHz. No external components are required. The frequency of the sinewave output is derived from either an external crystal or clock input, providing a stable and accurate frequency reference. The frequency is programmed by a 16-bit serial data word. The ML2035 has a V_{OUT} amplitude of $\pm V_{CC}/2$.

The ML2035 is intended for telecommunications and modem applications that need low cost and accurate generation of precise test tones, call progress tones, and signaling tones.

FEATURES

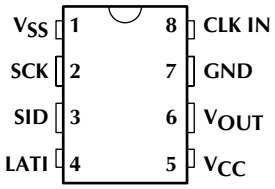
- Programmable output frequency - DC to 25kHz
- Low gain error and total harmonic distortion
- 3-wire SPI compatible serial microprocessor interface with double buffered data latch
- Fully integrated solution - no external components required
- Frequency resolution of 1.5Hz (±0.75Hz) with a 12MHz clock input
- Onboard 3 to 12MHz crystal oscillator
- Synchronous or asynchronous data loading capability
- Compatible with ML2031 and ML2032 tone detectors and ML2004 logarithmic gain/attenuator

BLOCK DIAGRAM



PIN CONFIGURATION

ML2035
8-Pin PDIP (P08)



TOP VIEW

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	V_{SS}	Negative supply (-5V).
2	SCK	Serial clock. Digital input which clocks in serial data on its rising edges.
3	SID	Serial input data which programs the frequency of V_{OUT}.
4	LATI	Digital input which latches serial data into the internal data latch on falling edges.
5	V_{CC}	Positive supply (5V).
6	V_{OUT}	Analog output. V_{OUT} swing is $\pm V_{CC}/2$.
7	GND	Ground. All inputs and outputs are referenced to this point.
8	CLK IN	Clock input. The internal clock can be generated by tying a 3 to 12MHz crystal from this pin to GND, or applying a digital clock signal directly to the pin.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{CC} 6.5V
V_{SS} ..... -6.5V
V_{OUT} ..... V_{SS} - 0.3V to V_{CC} + 0.3V
Voltage on any other pin ..... GND - 0.3V to V_{CC} + 0.3V
Input Current ..... ±25mA
Junction Temperature 150ºC
Storage Temperature Range ..... –65ºC to 150ºC
Lead Temperature (Soldering, 10 sec) 260ºC
Thermal Resistance (θ_{JA}) 110ºC/W

OPERATING CONDITIONS

Temperature Range
ML2035CP ..... 0ºC to 70ºC
ML2035IP ..... -40ºC to 85ºC
V_{CC} Range ..... 4.5V to 5.5V
V_{SS} Range ..... -4.5V to -5.5V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CC} = 4.5V to 5.5V, V_{SS} = -4.5V to -5.5V, CLK IN = 12.352MHz, C_L = 100pF, R_L = 1kΩ, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OUTPUT							
HD	Harmonic Distortion	20Hz to 5kHz				-45	dB
	(2nd and 3rd Harmonic)	5kHz to 25kHz				-40	dB
SND	Signal to Noise + Distortion	200Hz to 3.4kHz, f_{OUT} BW = 20Hz to 4kHz				-45	dB
		20Hz to 25kHz, f_{OUT} BW = 20 Hz to 75kHz				-40	dB
V_{GN}	Gain Error	20Hz < f_{OUT} < 5kHz				±0.15	dB
		5kHz < f_{OUT} < 25kHz				±0.3	dB
ICN	Idle Channel Noise	Power Down Mode, Cmsg Weighted			-20	0	dBrnc
		Power Down Mode, 1kHz			50		nV/√Hz
PSRR	Power Supply Rejection Ratio	200mV_{P-P}, 0 - 10kHz	V_{CC}			-40	dB
		Sine, Measured on V_{OUT}	V_{SS}			-40	dB
V_{OS}	V_{OUT} Offset Voltage					±75	mV
V_{P-P}	Peak-to-Peak Output Voltage				±V_{CC}/2		V
OSCILLATOR							
V_{IL} CLK	CLK IN Input Low Voltage					1.5	V
V_{IH} CLK	CLK IN Input High Voltage			3.5			V
I_{IL} CLK	CLK IN Input Low Current			-250			µA
I_{IH} CLK	CLK IN Input High Current					250	µA
C_{IN} CLK	CLK IN Input Capacitance				12		pF
t_{CKI}	CLK IN On/Off Period	t_R = t_F = 10ns, 2.5V Midpoint		30			ns
LOGIC (LATI, SID, SCK)							
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2.0			V
I_{IL}	Input Low Current	V_{IN} = 0V		-1			µA
I_{IH}	Input High Current	V_{IN} = V_{CC}				1	µA

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC (Continued)						
V_{OL}	Output Low Voltage	I_{OL} = -2mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 2mA	4.0			V
t_{SCK}	Serial Clock On/Off Period		100			ns
t_{DS}	SID Data Setup Time		50			ns
t_{DH}	SID Data Hold Time		50			ns
t_{LPW}	LATI Pulse Width		50			ns
t_{LH}	LATI Hold Time		50			ns
t_{LS}	LATI Setup Time		50			ns
SUPPLY						
I_{CC}	V_{CC} Current	No Load, V_{CC} = 5.5V			5.5	mA
		No Load, Power Down Mode			2	mA
I_{SS}	V_{SS} Current	No Load, V_{CC} = 5.5V, V_{SS} = -5.5V			-3.5	mA
		No Load, Power Down Mode			-100	µA

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

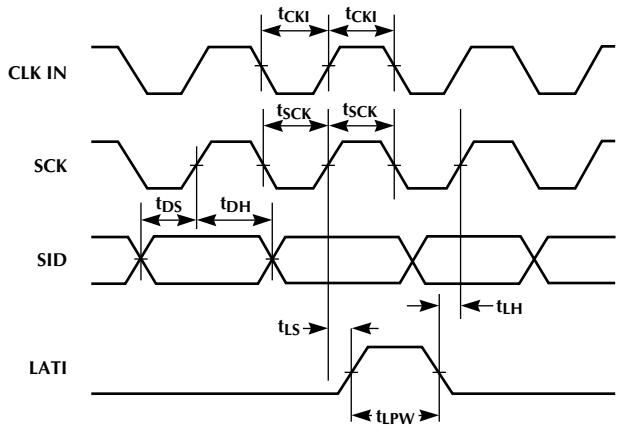


Figure 1. Serial Interface Timing.

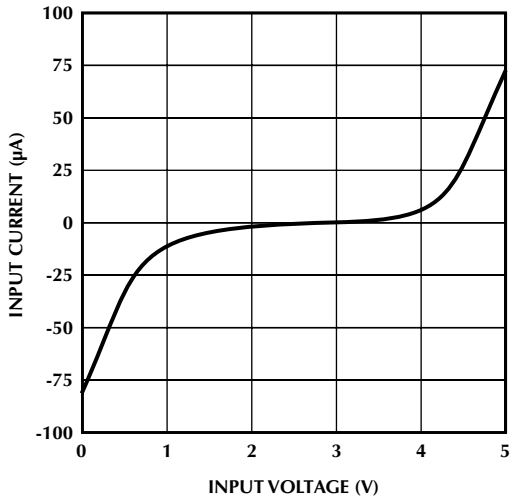


Figure 2. CLK IN Input Current vs. Input Voltage.

FUNCTIONAL DESCRIPTION

The ML2035 is composed of a programmable frequency generator, a sine wave generator, a crystal oscillator, and a serial digital interface. The ML2035 frequency and sine wave generator functional block diagram is shown in Figure 3.

PROGRAMMABLE FREQUENCY GENERATOR

The programmable frequency generator produces a digital output whose frequency is determined by a 16-bit digital word.

The frequency generator is composed of a phase accumulator which is clocked at $f_{CLK\ IN}/4$. The value stored in the data latch is added to the phase accumulator every 4 cycles of CLK IN. The frequency of the analog output is equal to the rate at which the accumulator overflows and is given by the equation:

$$f_{OUT} = \frac{f_{CLKIN} \times (D15 - D0)_{DEC}}{2^{23}} \quad (1)$$

The frequency resolution and the minimum frequency are the same and is given by the following equation:

$$\Delta f_{MIN} = \frac{f_{CLKIN}}{2^{23}} \quad (2)$$

When $f_{CLK\ IN}$ = 12.352MHz, Δf_{MIN} = 1.5Hz (±0.75Hz). Lower frequencies are obtained by using a lower input clock frequency.

Due to the phase quantization nature of the frequency generator, spurious tones can be present in the output range of –55dB relative to fundamental. The energy from these tones is included in the signal to noise + distortion specification. The frequency of these tones can be very close to the fundamental. Therefore, it is not practical to filter them out.

SINEWAVE GENERATOR

The sinewave generator is composed of a sine look-up table, a DAC, and an output smoothing filter. The sine look-up table is addressed by the phase accumulator. The DAC is driven by the output of the look-up table and generates a staircase representation of a sine wave.

The output filter smoothes the analog output by removing the high frequency sampling components. The resultant voltage on V_{OUT} is a sinusoid with the second and third harmonic distortion components at least 45dB below the fundamental.

The ML2035 provides a peak sinewave voltage of $\pm V_{CC}/2$, referenced to GND.

The analog section is designed to operate over a range from DC to 25kHz. Due to slew rate limitations, the peak-to-peak output voltage must be limited to $V_{OUT(P-P)} \leq (125kV \times Hz)/f_{OUT}$. Since the ML2035 peak-to-peak output voltage is equal to V_{CC}, the maximum output frequency must be limited to 25kHz for V_{CC} = 5V. V_{OUT} can drive a 1kΩ, 100pF loads, provided the slew rate limitations mentioned above are not exceeded.

The output offset voltage, V_{OS}, is a function of the peak-to-peak output voltage and is specified as:

(3)

For example, if $V_{OUT(P-P)}$ = 2.5V:

CRYSTAL OSCILLATOR

The crystal oscillator generates an accurate reference clock for the programmable frequency generator. The internal clock can be generated with a crystal or external clock.

If a crystal is used, it must be placed between CLK IN and GND of the ML2035. An on-chip crystal oscillator will then generate the internal clock. No other external capacitors or components are required. The crystal should be a parallel-resonant type with a frequency between 3MHz to 12.4MHz. It should be placed physically as close as possible to the CLK IN and GND.

An external clock can drive CLK IN directly if desired. The frequency of this clock can be anywhere between 0 and 12MHz.

The crystal must have the following characteristics:

1. Parallel resonant type
2. Frequency: 3MHz to 12.4MHz
3. Maximum equivalent series resistance of 15Ω at a drive levels of 1µW to 200µW, and 30Ω at drive levels of 10nW to 1µW
4. Typical load capacitance: 18pF
5. Maximum case capacitance: 7pF

The frequency of oscillation will be a function of the crystal parameters and PC board capacitance. Crystals that meet these requirements at 12.352000MHz are M-tron 3709-010 12.352 for 0ºC to 70ºC and 3709-020 12.352 for -40ºC to 85ºC operation.

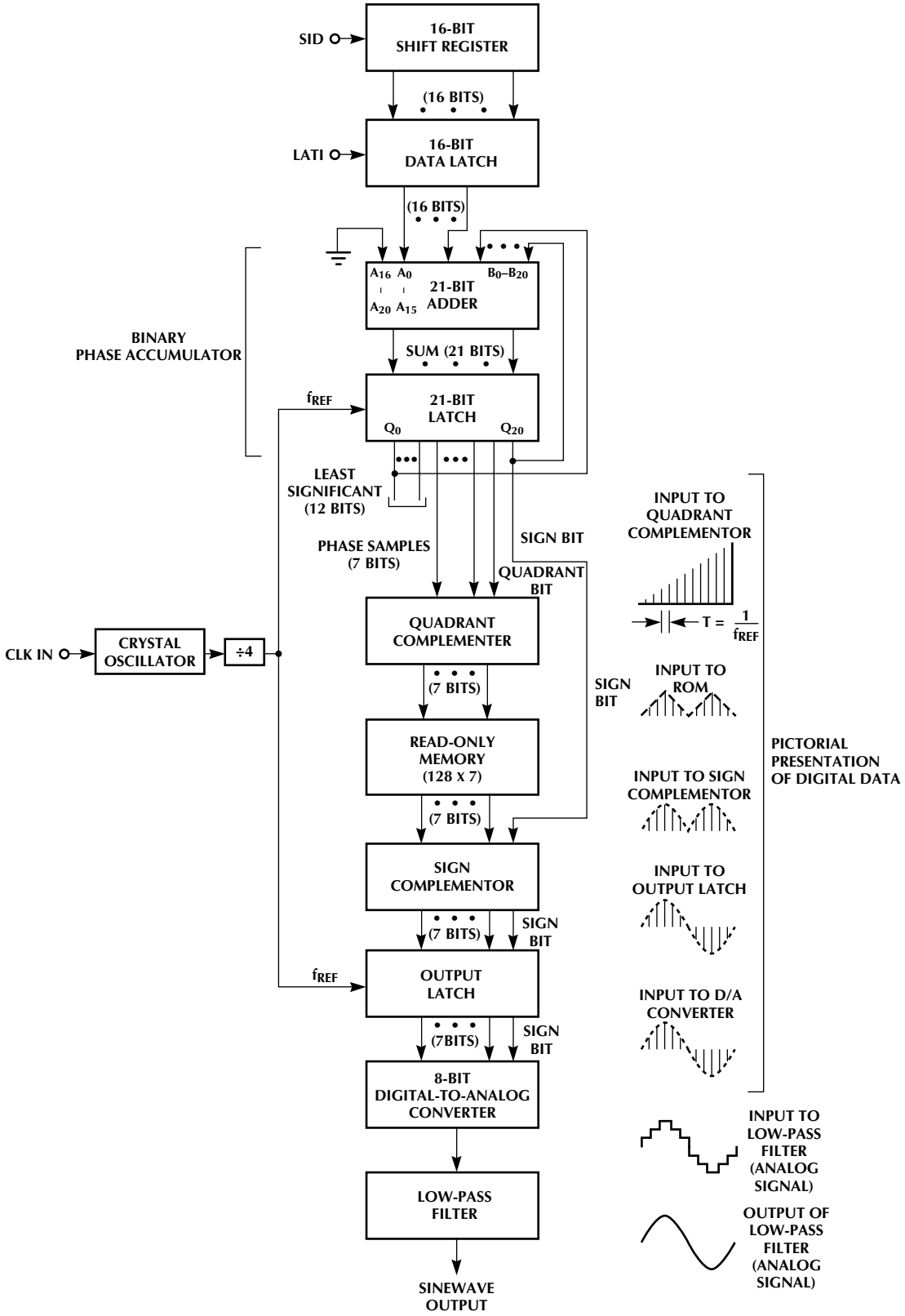


Figure 3. Detailed Block Diagram of the ML2035.

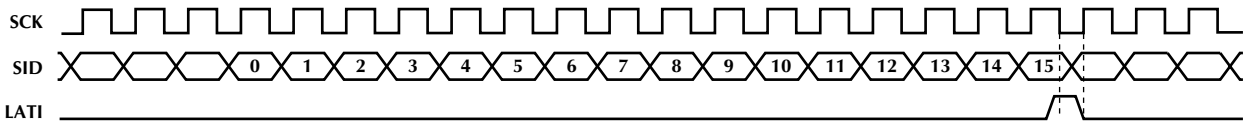


Figure 4. Serial Interface Timing.

FUNCTIONAL DESCRIPTION (Continued)

SERIAL DIGITAL INTERFACE

The digital interface consists of a shift register and data latch. The serial 16-bit data word on SID is clocked into a 16-bit shift register on rising edges of the serial shift clock, SCK. The LSB should be shifted in first and the MSB last as shown in Figure 4. The data that has been shifted into the shift register is loaded into a 16-bit data latch on the falling edge of LATI. To insure that true data is loaded into the data latch from the shift register, LATI falling edge should occur when SCK is low, as shown in figure 1. LATI should be low while shifting data into the shift register to avoid inadvertently entering the power down mode. Note that all data is entered and latched on the edges, not levels, of SCK and LATI.

POWER DOWN MODE

The power down mode of the ML2035 can be selected by entering all zeros in the shift register and applying a logic "1" to LATI and holding it high. A zero data detect circuit detects when all bits in the shift register are zeros. In this state, the power consumption is reduced to 11.5mW max, and V_{OUT} goes to 0V as shown in Figure 5 and appears as 10kΩ to ground. The master clock, CLK IN, can be left active or removed during power down mode.

POWER SUPPLIES

The analog circuits in ML2035 are powered from V_{CC} to V_{SS} and are referenced to GND. The digital circuits in the device are powered from V_{CC} to GND.

It is recommended that the power supplies to the device should be bypassed by placing decoupling capacitors from V_{CC} to GND and V_{SS} to GND as physically close to the device as possible.

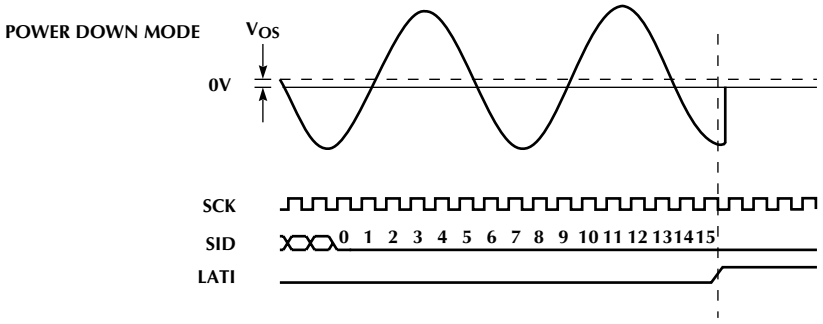


Figure 5. Power Down Mode Waveforms.

TYPICAL APPLICATIONS

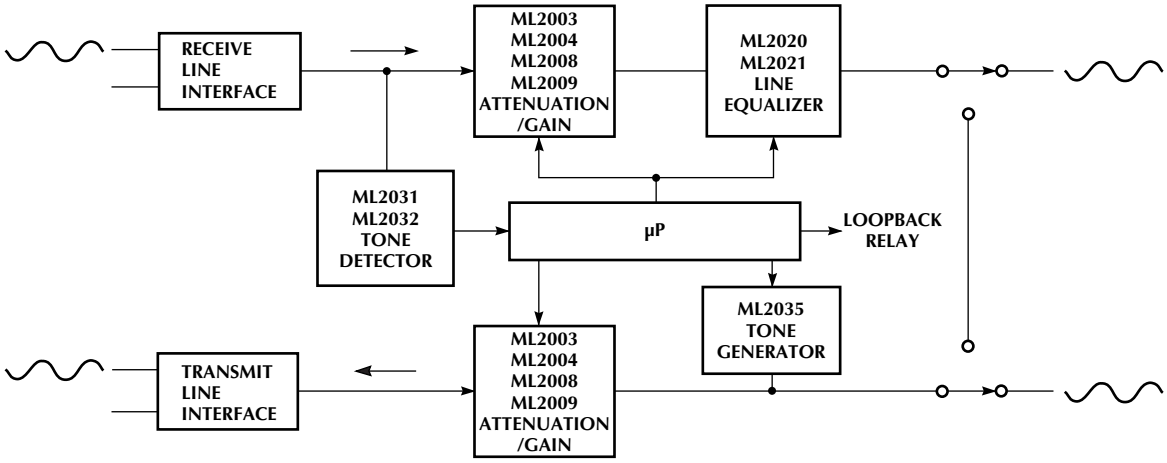


Figure 6. 4-Wire Termination Equipment.

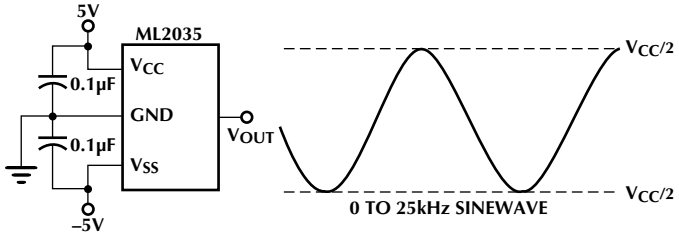
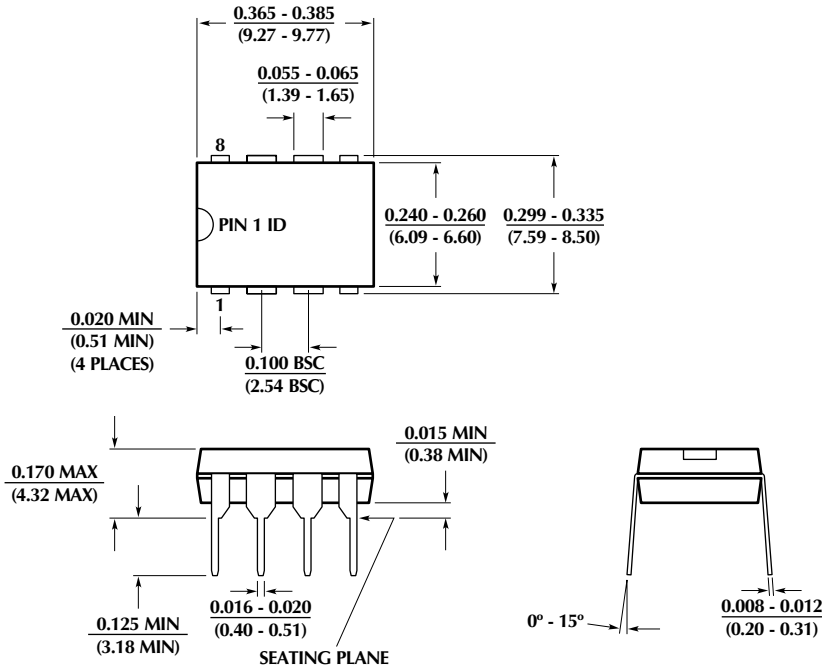


Figure 7. Sine Wave Ratiometric to ±V_{CC}/2.

PHYSICAL DIMENSIONS inches (millimeters)

Package: P08
8-Pin PDIP



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML2035CP	0ºC to 70ºC	8-Pin PDIP (P08)
ML2035IP	-40ºC to 85ºC	8-Pin PDIP (P08)

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