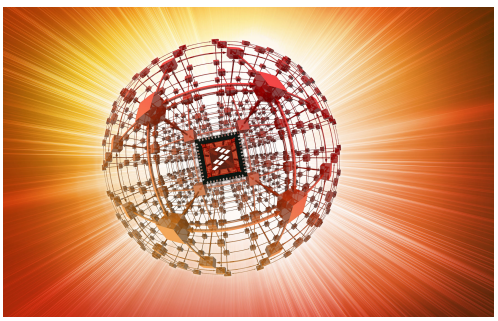
Document Number: K61PB
Rev. 9, 12/2011

K61 Family Product Brief

Supports all K61 devices



Contents

1 Kinetis Portfolio

Kinetis is the most scalable portfolio of low power, mixed-signal ARM®Cortex™-M4 MCUs in the industry. Phase 1 of the portfolio consists of five MCU families with over 200 pin-, peripheral- and software-compatible devices. Each family offers excellent performance, memory and feature scalability with common peripherals, memory maps, and packages providing easy migration both within and between families.

Kinetis MCUs are built from Freescale's innovative 90nm Thin Film Storage (TFS) flash technology with unique FlexMemory. Kinetis MCU families combine the latest low-power innovations and high performance, high precision mixed-signal capability with a broad range of connectivity, human-machine interface, and safety & security peripherals. Kinetis MCUs are supported by a market-leading enablement bundle from Freescale and numerous ARM 3rd party ecosystem partners.

Energy Efficient Solutions optimized for low power

freescale

Family	Program Flash	Packages	Key Features
K70 Family	512KB-1MB	196-256pin	
K6x Family	256KB-1MB	100-256pin	
K50 Family	128-512KB	64-144pin	
K40 Family	64-512KB	64-144pin	
K30 Family	64-512KB	64-144pin	
K20 Family	32KB-1MB	32-144pin	
K10 Family	32KB-1MB	32-144pin	

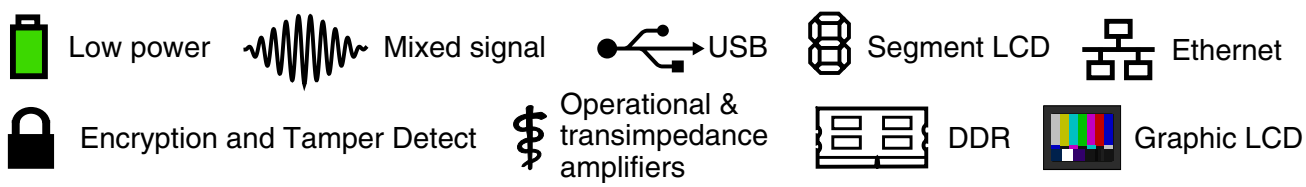


Figure 1. Kinetis MCU portfolio

All Kinetis families include a powerful array of analog, communication and timing and control peripherals with the level of feature integration increasing with flash memory size and the number of inputs/outputs. Some of the available features in Kinetis families include:

- Core:
  - ARM Cortex-M4 Core delivering 1.25 DMIPS/MHz with DSP instructions (floating-point unit available on certain Kinetis families)
  - Up to 32-channel DMA for peripheral and memory servicing with minimal CPU intervention
  - Broad range of performance levels rated at maximum CPU frequencies of 50 MHz, 72 MHz, 100 MHz, 120 MHz, and 150 MHz
- Ultra-low power:
  - Multiple low power operating modes for optimizing peripheral activity and wake-up times for extended battery life.
  - Low–leakage wake-up unit, low power timer, and low power RTC for additional low power flexibility
  - Industry-leading fast wake-up times
- Memory:
  - Scalable memory footprints from 32 KB flash / 8 KB RAM to 1 MB flash / 128 KB RAM. Independent flash banks enable concurrent code execution and firmware updates
  - Optional 16 KB cache memory for optimizing bus bandwidth and flash execution performance. Offered on K10, K20, and K6x family devices with CPU performance of up to 150 MHz.
  - FlexMemory with up to 512 KB FlexNVM and up to 16 KB FlexRAM. FlexNVM can be partitioned to support additional program flash memory (ex. bootloader), data flash (ex. storage for large tables), or EEPROM backup. FlexRAM supports EEPROM byte-write/byte-erase operations and dictates the maximum EEPROM size.
  - EEPROM endurance capable of exceeding 10 million cycles
  - EEPROM erase/write times an order of magnitude faster than traditional EEPROM

    - Multi-function external bus interface capable of interfacing to external memories, gate-array logic
    - DDR memory controller
    - NAND flash controller
- Mixed-signal analog:
    - Fast, high precision 16-bit ADCs, 12-bit DACs, programmable gain amplifiers, high speed comparators and an internal voltage reference. Powerful signal conditioning, conversion and analysis capability with reduced system cost
- Human Machine Interface (HMI):
    - Capacitive Touch Sensing Interface with full low-power support and minimal current adder when enabled
- Connectivity and Communications:
    - UARTs with ISO7816, CEA709.1-B (LON), and IrDA support, I2S, CAN, I2C and DSPI
    - Full-speed USB OTG controller with on-chip transceiver
    - High-speed USB OTG controller with ULPI interface
- Reliability, Safety and Security:
    - Hardware cyclic redundancy check engine for validating memory contents/communication data and increased system reliability
    - Independent-clocked computer operating properly (COP) for protection against code runaway in fail-safe applications
    - External watchdog monitor
    - Secure storage and tamper detect
- Timing and Control:
    - Powerful FlexTimers which support general purpose, PWM, and motor control functions
    - Carrier Modulator Transmitter for IR waveform generation
    - Programmable Interrupt Timer for RTOS task scheduler time base or trigger source for ADC conversion and programmable delay block
- System:
    - 5 V tolerant GPIO with pin interrupt functionality
    - Wide operating voltage range from 1.71 V to 3.6 V with flash programmable down to 1.71 V with fully functional flash and analog peripherals
    - Ambient operating temperature ranges from -40 °C to 105 °C

2 K61 Family Introduction

In addition to providing IEEE 1588 Ethernet, full- and high-speed USB 2.0 On-The-Go with device charger detect capabilities, the K61 MCU family includes security features, such as hardware encryption, tamper detection, and a key storage protection area. The K61 family devices are also PCI PTS 3.0 pre-certified for ePOS PINPAD applications.

Devices start from 512 KB of flash in 144MAPBGA packages extending up to 1 MB in a 256MAPBGA package with a rich suite of analog, communication, timing and control peripherals. High memory density K61 family devices include an optional single precision floating point unit, NAND flash controller and DRAM controller.

3 Block Diagram

The below figure shows a superset block diagram of the device. Other devices within the family have a subset of the features.

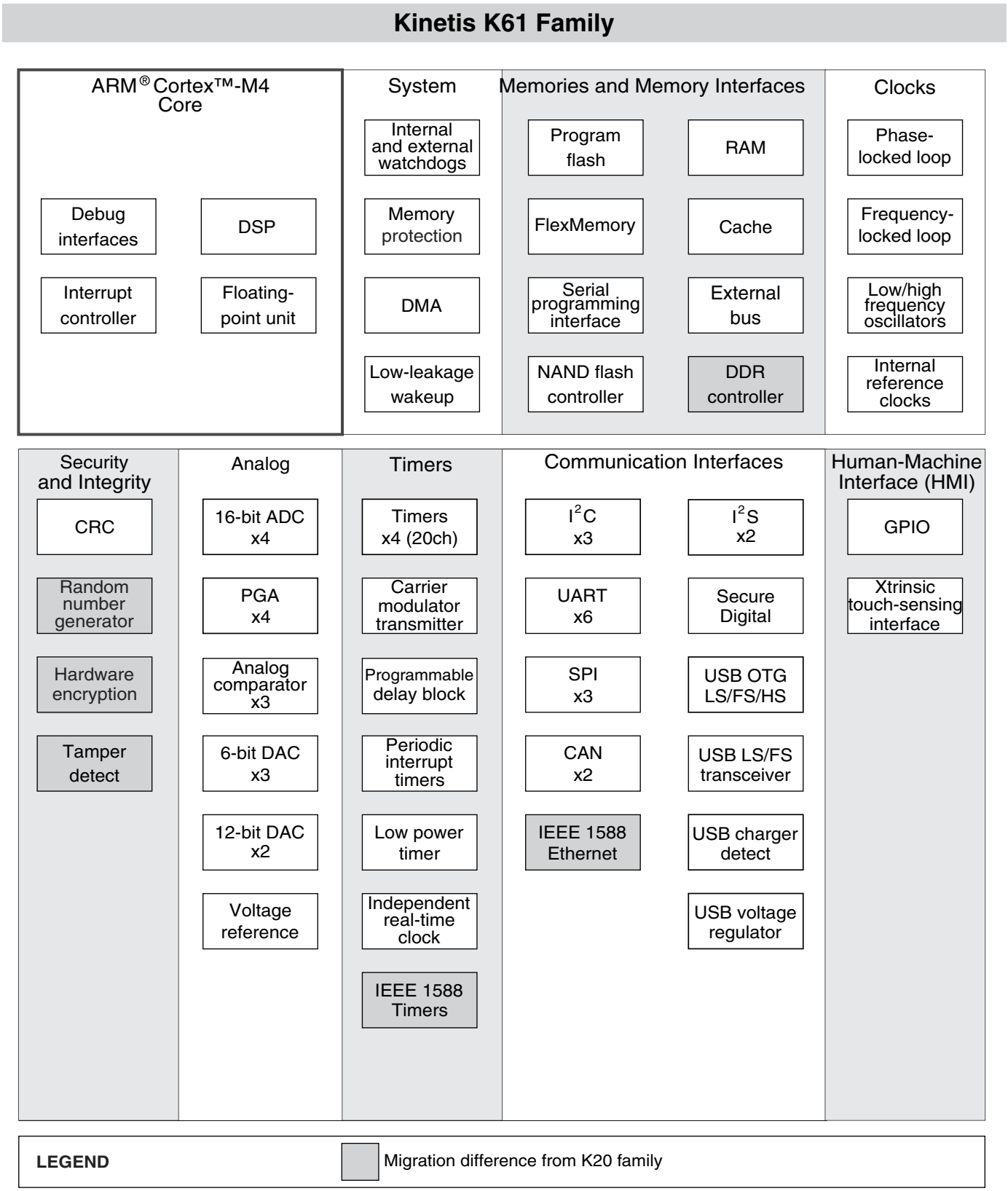


Figure 2. K61 Block Diagram

4 Features

4.1 Common features among the K61 family

All devices within the K61 family features the following at a minimum:

Table 1. Common features among all K61 devices

Operating characteristics	• Voltage range 1.71V - 3.6V • Flash memory programming down to 1.71V • Temperature range (T_A) -40 to 105°C • Flexible modes of operation

Core features	• Next generation 32-bit ARM Cortex-M4 core
	• Supports DSP instructions
	• Nested vectored interrupt controller (NVIC)
	• Asynchronous wake-up interrupt controller (AWIC)
	• Debug & trace capability
	  • 2-pin serial wire debug (SWD)
	  • IEEE 1149.1 Joint Test Action Group (JTAG)
	  • IEEE 1149.7 compact JTAG (cJTAG)
	  • Trace port interface unit (TPIU)
	  • Flash patch and breakpoint (FPB)
	  • Data watchpoint and trace (DWT)
	  • Instrumentation trace macrocell (ITM)

System and power management	• Software and hardware watchdog with external monitor pin • DMA controller • Low-leakage wake-up unit (LLWU) • Power management controller with 10 different power modes • Non-maskable interrupt (NMI) • 128-bit unique identification (ID) number per chip

Clocks	• Multi-purpose clock generator
	  • PLL and FLL operation
	  • Internal reference clocks
	• 3MHz to 32MHz crystal oscillator
	• 32kHz to 40kHz crystal oscillator
	• Internal 1kHz low power oscillator
	• DC to 50MHz external square wave input clock

Memories and Memory Interfaces	• FlexMemory consisting of FlexNVM (non-volatile flash memory that can execute program code, store data, or backup EEPROM data) or FlexRAM (RAM memory that can be used as traditional RAM or as high-endurance EEPROM storage, and also accelerates flash programming) • Flash security and protection features • Serial flash programming interface (EzPort)
Security and integrity	• Cyclic redundancy check (CRC)

Table continues on the next page...

Table 1. Common features among all K61 devices (continued)

Analog	• 16-bit SAR ADC • Programmable voltage reference (VREF) • High-speed Analog comparator (CMP) with 6-bit DAC
Timers	• 1x8ch motor control/general purpose/PWM flexible timer (FTM) • 2x2ch quadrature decoder/general purpose/PWM flexible timer (FTM) • Carrier modulator timer (CMT) • Programmable delay block (PDB) • 1x4ch programmable interrupt timer (PIT) • Low-power timer (LPT)
Communications	• SPI • I^2C with SMBUS support • UART (w/ ISO7816, LON, IrDA and hardware flow control)
Human-machine interface	• GPIO with pin interrupt support, DMA request capability, digital glitch filter, and other pin control options • Capacitive touch sensing inputs

4.1.1 Memory and package options

The following table summarizes the memory and package options for the K61 family. All devices which share a common package are pin-for-pin compatible.

Table 2. K61 family summary

Sub-Family	Performance (MHz)	Memory				Package						
		Flash (KB)	FlexNVM (KB)	SRAM (KB)	EEPROM/FlexRAM (KB)	100 LQFP (14x14)	104BGA (8x8)	121BGA (8x8)	144LQFP (20x20)	144BGA (13x13)	196BGA (15x15)	256BGA (17x17)
K61FN	120	1024	—	128	—	—	—	—	—	+	+	+
	150	1024	—	128	—	—	—	—	—	+	+	+
K61FX	120	512	512	128	16	—	—	—	—	+	+	+
	150	512	512	128	16	—	—	—	—	+	+	+

4.2 FlexMemory

Freescale's new FlexMemory technology provides an extremely versatile and powerful solution for designers seeking on-chip EEPROM and/or additional program or data flash memory. As easy and as fast as SRAM, it requires no user or system intervention to complete programming and erase functions when used as high endurance byte-write/byte-erase EEPROM. EEPROM array size can also be configured for improved endurance to suit application requirements. FlexMemory can also provide additional flash memory (FlexNVM) for data or program storage in parallel with the main program flash.

The key features of FlexMemory include:

- Configurability for designer:
  - EEPROM array size and number of write/erase cycles
  - Program or data flash size
- EEPROM endurance of 10M write/erase cycles possible over full voltage and temperature range
- Seamless EEPROM read/write operations: simply write or read a memory address
- High-speed byte, 16-bit, and 32-bit write/erase operations to EEPROM
- Eliminates the costs associated with external EEPROM ICs, and the software headaches and resource (CPU/flash/RAM) impact of EEPROM emulation schemes
- Storage for large data tables or bootloader
- Read-while-write operation with main program flash memory
- Minimum write voltage 1.71V

4.2.1 Programmable Trade-Off

FlexMemory lets you fully configure the way FlexNVM and FlexRAM blocks are used to provide the best balance of memory resources for their application.

The user can configure several parameters, including EEPROM size, endurance, write size, and the size of additional program/data flash.

In addition to this flexibility, FlexMemory provides superior EEPROM performance, endurance, and low-voltage operation when compared to traditional EEPROM solutions.

- Enhanced EEPROM — Combines FlexRAM and FlexNVM to create byte-write/erase, high-speed, and high-endurance EEPROM
- FlexNVM — Can be used as:
  - part of the EEPROM configuration,
  - additional program or data flash, or
  - a combination of the above. For example, a portion can be used as flash while the rest is used for enhanced EEPROM backup.
- FlexRAM — Can be used as part of the EEPROM configuration or as additional system RAM

4.2.2 Use Case Example

The MCU has 128 KB program flash, 32 KB SRAM, and FlexMemory has 128 KB FlexNVM and 4 KB FlexRAM (maximum EEPROM size). The application requires 8 KB additional program flash for a bootloader and 256 bytes of high-endurance EEPROM. The user allocates 8 KB of FlexNVM for the additional program flash and the remaining 120 KB for EEPROM backup.

The user defines 256 bytes of EEPROM size from the FlexRAM. In this example, the EEPROM endurance results in a minimum of 2.32M write/erase cycles.

4.3 Part Numbers and Packaging

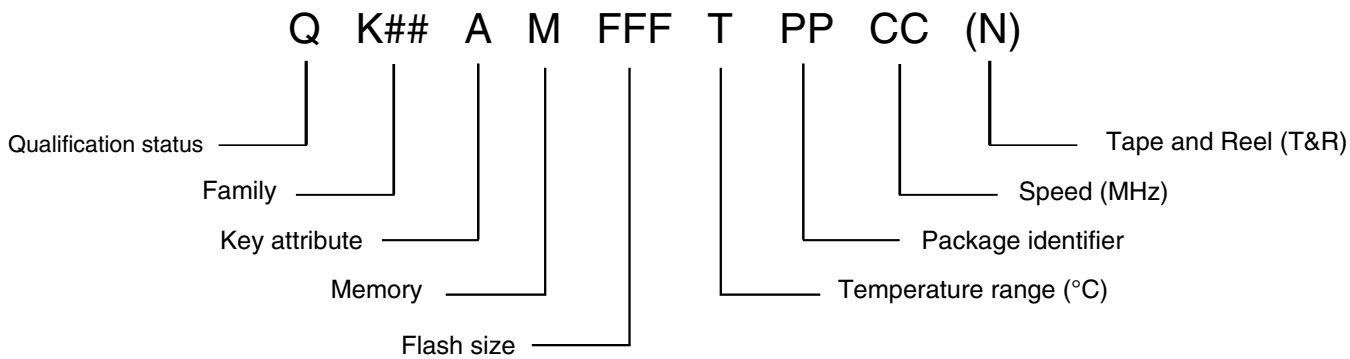


Figure 3. Part numbers diagrams

4.4 K61 family features

The following sections list the differences among the various devices available within the K61 family. The sections are split by levels of performance.

The features listed below each part number specify the maximum configuration available on that device. The signal multiplexing configuration determines which modules can be used simultaneously.

4.4.1 K61 family features (120MHz Performance)

Table 3. K61 120MHz Performance Table

MC Partnumber	MK61FX512VMD12(R)	MK61FN1M0VMD12(R)	MK61FX512VMF12(R)	MK61FN1M0VMF12(R)	MK61FX512VMJ12(R)	MK61FN1M0VMJ12(R)
General						
CPU Frequency	120 MHz	120 MHz	120 MHz	120 MHz	120 MHz	120 MHz
Pin Count	144	144	196	196	256	256
Package	MAPBGA	MAPBGA	MAPBGA	MAPBGA	MAPBGA	MAPBGA
Memories and Memory Interfaces						
Total Flash Memory	1MB	1MB	1MB	1MB	1MB	1MB
Flash	512KB	1MB	512KB	1MB	512KB	1MB

Table continues on the next page...

Table 3. K61 120MHz Performance Table (continued)

MC Partnumber	MK61FX512VMD12(R)	MK61FN1M0VMD12(R)	MK61FX512VMF12(R)	MK61FN1M0VMF12(R)	MK61FX512VMJ12(R)	MK61FN1M0VMJ12(R)
FlexNVM	512KB	-	512KB	-	512KB	-
EEPROM/FlexRAM	16KB	-	16KB	-	16KB	-
SRAM	128KB	128KB	128KB	128KB	128KB	128KB
Serial Programming Interface	YES	YES	YES	YES	YES	YES
External Bus Interface (FlexBus), Addr/ Data/CS	32/32/6	32/32/6	32/32/6	32/32/6	32/32/6	32/32/6
Non-Muxed External Bus Interface (Flexbus), Addr/Data/CS	30/16/6, 30/8/6	30/16/6, 30/8/6	30/16/6, 30/8/6	30/16/6, 30/8/6	30/16/6, 30/8/6	30/16/6, 30/8/6
DDR Controller	-	-	-	-	YES	YES
NAND Flash Controller	YES	YES	YES	YES	YES	YES
Cache	16KB	16KB	16KB	16KB	16KB	16KB
Core Modules						
DSP	YES	YES	YES	YES	YES	YES
SPFPU	YES	YES	YES	YES	YES	YES
Debug	JTAG, cJTAG, SWD	JTAG, cJTAG, SWD	JTAG, cJTAG, SWD	JTAG, cJTAG, SWD	JTAG, cJTAG, SWD	JTAG, cJTAG, SWD
Trace	TPIU, FPB, DWT, ITM, ETM, ETB	TPIU, FPB, DWT, ITM, ETM, ETB	TPIU, FPB, DWT, ITM, ETM, ETB	TPIU, FPB, DWT, ITM, ETM, ETB	TPIU, FPB, DWT, ITM, ETM, ETB	TPIU, FPB, DWT, ITM, ETM, ETB
NMI	YES	YES	YES	YES	YES	YES
System Modules						
Software Watchdog	YES	YES	YES	YES	YES	YES
Hardware Watchdog	YES	YES	YES	YES	YES	YES
PMC	YES	YES	YES	YES	YES	YES
MPU	YES	YES	YES	YES	YES	YES
DMA	32ch	32ch	32ch	32ch	32ch	32ch
Clock Modules						
MCG	YES	YES	YES	YES	YES	YES
OSC (32-40kHz/3-32MHz)	32-40kHz/ 8-32MHz	32-40kHz/ 8-32MHz	32-40kHz/ 8-32MHz	32-40kHz/ 8-32MHz	32-40kHz/ 8-32MHz	32-40kHz/ 8-32MHz

Table continues on the next page...

Table 3. K61 120MHz Performance Table (continued)

MC Partnumber	MK61FX512VMD12(R)	MK61FN1M0VMD12(R)	MK61FX512VMF12(R)	MK61FN1M0VMF12(R)	MK61FX512VMJ12(R)	MK61FN1M0VMJ12(R)
Secondary OSC	32-40kHz/ 8-32MHz	32-40kHz/ 8-32MHz	32-40kHz/ 8-32MHz	32-40kHz/ 8-32MHz	32-40kHz/ 8-32MHz	32-40kHz/ 8-32MHz
RTC (32KHz Osc, Vbat)	YES	YES	YES	YES	YES	YES
RTC_CLKOUT	-	-	YES	YES	YES	YES
RTC_WAKEUP	YES	YES	YES	YES	YES	YES
Security and Integrity						
Hardware Encryption	YES	YES	YES	YES	YES	YES
Tamper Detect	YES	YES	YES	YES	YES	YES
Number of External Tamper Pins	6	6	8	8	8	8
CRC	YES	YES	YES	YES	YES	YES
Analog						
ADC0 (SE:single-ended, DP:differential pair)	15ch SE + 3ch DP	15ch SE + 3ch DP	21ch SE + 3ch DP	21ch SE + 3ch DP	21ch SE + 3ch DP	21ch SE + 3ch DP
ADC1	20ch SE + 3ch DP	20ch SE + 3ch DP	20ch SE + 3ch DP	20ch SE + 3ch DP	20ch SE + 3ch DP	20ch SE + 3ch DP
ADC2	9ch SE + 2ch DP	9ch SE + 2ch DP	17ch SE + 2ch DP	17ch SE + 2ch DP	17ch SE + 2ch DP	17ch SE + 2ch DP
ADC3	8ch SE + 2ch DP	8ch SE + 2ch DP	18ch SE + 2ch DP	18ch SE + 2ch DP	18ch SE + 2ch DP	18ch SE + 2ch DP
ADC DP	4ch	4ch	4ch	4ch	4ch	4ch
ADC SE	53ch	53ch	77ch	77ch	77ch	77ch
PGA	4	4	4	4	4	4
12-bit DAC	2	2	2	2	2	2
Analog Comparator	4	4	4	4	4	4
Analog Comparator Inputs	5 / 2 / 2 / 5	5 / 2 / 2 / 5	5 / 2 / 2 / 5	5 / 2 / 2 / 5	5 / 2 / 2 / 5	5 / 2 / 2 / 5
OPAMP	-	-	-	-	-	-
TRIAMP	-	-	-	-	-	-
Vref	YES	YES	YES	YES	YES	YES
Timers						
Motor Control/General purpose/PWM	2x8ch	2x8ch	2x8ch	2x8ch	2x8ch	2x8ch
Quad decoder/General purpose/PWM	2x2ch	2x2ch	2x2ch	2x2ch	2x2ch	2x2ch

Table continues on the next page...

Table 3. K61 120MHz Performance Table (continued)

MC Partnumber	MK61FX512VMD12(R)	MK61FN1M0VMD12(R)	MK61FX512VMF12(R)	MK61FN1M0VMF12(R)	MK61FX512VMJ12(R)	MK61FN1M0VMJ12(R)
FTM External CLK	2	2	2	2	2	2
Low Power Timer	1	1	1	1	1	1
PIT	1x4ch	1x4ch	1x4ch	1x4ch	1x4ch	1x4ch
PDB	1	1	1	1	1	1
CMT(Carrier Module Transmitter)	YES	YES	YES	YES	YES	YES
Communication Interfaces						
SDHC	8-bit, CLKIN	8-bit, CLKIN	8-bit, CLKIN	8-bit, CLKIN	8-bit, CLKIN	8-bit, CLKIN
High Baudrate UART w/ ISO7816 + LON	1	1	1	1	1	1
High Baudrate UART w/ ISO7816	1	1	1	1	1	1
High Baudrate UART	0	0	0	0	0	0
UART	4	4	4	4	4	4
SPI chip selects per module	6 / 4 / 2	6 / 4 / 2	6 / 4 / 2	6 / 4 / 2	6 / 4 / 2	6 / 4 / 2
I2C	2	2	2	2	2	2
I2S	2	2	2	2	2	2
I2S0 TX/RX	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2
I2S1 TX/RX	0 / 2	0 / 2	2 / 2	2 / 2	2 / 2	2 / 2
CAN	2	2	2	2	2	2
USB OTG LS/FS w/ on-chip xcvr	1	1	1	1	1	1
USB OTG HS	1	1	1	1	1	1
USB DCD	YES	YES	YES	YES	YES	YES
USB 120mAReg	YES	YES	YES	YES	YES	YES
Ethernet w /1588	MII / RMII	MII / RMII	MII / RMII	MII / RMII	MII / RMII	MII / RMII
IEEE1588 Timer	1x4ch, CLKIN	1x4ch, CLKIN	1x4ch, CLKIN	1x4ch, CLKIN	1x4ch, CLKIN	1x4ch, CLKIN
Human-Machine Interface						
Segment LCD	-	-	-	-	-	-
Graphic LCD	-	-	-	-	-	-
TSI(Capacitive Touch)	16 input	16 input	16 input	16 input	16 input	16 input
GPIO (w interrupt)	95	95	128	128	128	128

Table continues on the next page...

Table 3. K61 120MHz Performance Table (continued)

MC Partnumber	MK61FX512VMD12(R)	MK61FN1M0VMD12(R)	MK61FX512VMF12(R)	MK61FN1M0VMF12(R)	MK61FX512VMJ12(R)	MK61FN1M0VMJ12(R)
5V Tolerant GPIOs	91	91	124	124	124	124
Operating Characteristics						
5V Tolerant	YES	YES	YES	YES	YES	YES
Voltage Range	1.71-3.6V	1.71-3.6V	1.71-3.6V	1.71-3.6V	1.71-3.6V	1.71-3.6V
Flash Write V	1.71V	1.71V	1.71V	1.71V	1.71V	1.71V
Temp Range	-40 to 105C	-40 to 105C	-40 to 105C	-40 to 105C	-40 to 105C	-40 to 105C

4.4.2 K61 family features (150MHz Performance)

Table 4. K61 150MHz Performance Table

MC Partnumber	MK61FX512VMD15(R)	MK61FN1M0VMD15(R)	MK61FX512VMF15(R)	MK61FN1M0VMF15(R)	MK61FX512VMJ15(R)	MK61FN1M0VMJ15(R)
General						
CPU Frequency	150 MHz	150 MHz	150 MHz	150 MHz	150 MHz	150 MHz
Pin Count	144	144	196	196	256	256
Package	MAPBGA	MAPBGA	MAPBGA	MAPBGA	MAPBGA	MAPBGA
Memories and Memory Interfaces						
Total Flash Memory	1MB	1MB	1MB	1MB	1MB	1MB
Flash	512KB	1MB	512KB	1MB	512KB	1MB
FlexNVM	512KB	-	512KB	-	512KB	-
EEPROM/FlexRAM	16KB	-	16KB	-	16KB	-
SRAM	128KB	128KB	128KB	128KB	128KB	128KB
Serial Programming Interface	YES	YES	YES	YES	YES	YES

Table continues on the next page...

Table 4. K61 150MHz Performance Table (continued)

MC Partnumber	MK61FX512VMD15(R)	MK61FN1M0VMD15(R)	MK61FX512VMF15(R)	MK61FN1M0VMF15(R)	MK61FX512VMJ15(R)	MK61FN1M0VMJ15(R)
External Bus Interface (FlexBus), Addr/ Data/CS	32/32/6	32/32/6	32/32/6	32/32/6	32/32/6	32/32/6
Non-Muxed External Bus Interface (Flexbus), Addr/Data/CS	30/16/6, 30/8/6	30/16/6, 30/8/6	30/16/6, 30/8/6	30/16/6, 30/8/6	30/16/6, 30/8/6	30/16/6, 30/8/6
DDR Controller	-	-	-	-	YES	YES
NAND Flash Controller	YES	YES	YES	YES	YES	YES
Cache	16KB	16KB	16KB	16KB	16KB	16KB
Core Modules						
DSP	YES	YES	YES	YES	YES	YES
SPFPU	YES	YES	YES	YES	YES	YES
Debug	JTAG, cJTAG, SWD	JTAG, cJTAG, SWD	JTAG, cJTAG, SWD	JTAG, cJTAG, SWD	JTAG, cJTAG, SWD	JTAG, cJTAG, SWD
Trace	TPIU, FPB, DWT, ITM, ETM, ETB	TPIU, FPB, DWT, ITM, ETM, ETB	TPIU, FPB, DWT, ITM, ETM, ETB	TPIU, FPB, DWT, ITM, ETM, ETB	TPIU, FPB, DWT, ITM, ETM, ETB	TPIU, FPB, DWT, ITM, ETM, ETB
NMI	YES	YES	YES	YES	YES	YES
System Modules						
Software Watchdog	YES	YES	YES	YES	YES	YES
Hardware Watchdog	YES	YES	YES	YES	YES	YES
PMC	YES	YES	YES	YES	YES	YES
MPU	YES	YES	YES	YES	YES	YES
DMA	32ch	32ch	32ch	32ch	32ch	32ch
Clock Modules						
MCG	YES	YES	YES	YES	YES	YES
OSC (32-40kHz/3-32MHz)	32-40kHz/ 8-32MHz	32-40kHz/ 8-32MHz	32-40kHz/ 8-32MHz	32-40kHz/ 8-32MHz	32-40kHz/ 8-32MHz	32-40kHz/ 8-32MHz
Secondary OSC	32-40kHz/ 8-32MHz	32-40kHz/ 8-32MHz	32-40kHz/ 8-32MHz	32-40kHz/ 8-32MHz	32-40kHz/ 8-32MHz	32-40kHz/ 8-32MHz
RTC (32KHz Osc, Vbat)	YES	YES	YES	YES	YES	YES
RTC_CLKOUT	-	-	YES	YES	YES	YES
RTC_WAKEUP	YES	YES	YES	YES	YES	YES

Table continues on the next page...

Table 4. K61 150MHz Performance Table (continued)

MC Partnumber	MK61FX512VMD15(R)	MK61FN1M0VMD15(R)	MK61FX512VMF15(R)	MK61FN1M0VMF15(R)	MK61FX512VMJ15(R)	MK61FN1M0VMJ15(R)
Security and Integrity						
Hardware Encryption	YES	YES	YES	YES	YES	YES
Tamper Detect	YES	YES	YES	YES	YES	YES
Number of External Tamper Pins	6	6	8	8	8	8
CRC	YES	YES	YES	YES	YES	YES
Analog						
ADC0 (SE:single-ended, DP:differential pair)	15ch SE + 3ch DP	15ch SE + 3ch DP	21ch SE + 3ch DP	21ch SE + 3ch DP	21ch SE + 3ch DP	21ch SE + 3ch DP
ADC1	20ch SE + 3ch DP	20ch SE + 3ch DP	20ch SE + 3ch DP	20ch SE + 3ch DP	20ch SE + 3ch DP	20ch SE + 3ch DP
ADC2	9ch SE + 2ch DP	9ch SE + 2ch DP	17ch SE + 2ch DP	17ch SE + 2ch DP	17ch SE + 2ch DP	17ch SE + 2ch DP
ADC3	8ch SE + 2ch DP	8ch SE + 2ch DP	18ch SE + 2ch DP	18ch SE + 2ch DP	18ch SE + 2ch DP	18ch SE + 2ch DP
ADC DP	4ch	4ch	4ch	4ch	4ch	4ch
ADC SE	53ch	53ch	77ch	77ch	77ch	77ch
PGA	4	4	4	4	4	4
12-bit DAC	2	2	2	2	2	2
Analog Comparator	4	4	4	4	4	4
Analog Comparator Inputs	5 / 2 / 2 / 5	5 / 2 / 2 / 5	5 / 2 / 2 / 5	5 / 2 / 2 / 5	5 / 2 / 2 / 5	5 / 2 / 2 / 5
OPAMP	-	-	-	-	-	-
TRIAMP	-	-	-	-	-	-
Vref	YES	YES	YES	YES	YES	YES
Timers						
Motor Control/General purpose/PWM	2x8ch	2x8ch	2x8ch	2x8ch	2x8ch	2x8ch
Quad decoder/General purpose/PWM	2x2ch	2x2ch	2x2ch	2x2ch	2x2ch	2x2ch
FTM External CLK	2	2	2	2	2	2
Low Power Timer	1	1	1	1	1	1
PIT	1x4ch	1x4ch	1x4ch	1x4ch	1x4ch	1x4ch
PDB	1	1	1	1	1	1
CMT(Carrier Module Transmitter)	YES	YES	YES	YES	YES	YES

Table continues on the next page...

Table 4. K61 150MHz Performance Table (continued)

MC Partnumber	MK61FX512VMD15(R)	MK61FN1M0VMD15(R)	MK61FX512VMF15(R)	MK61FN1M0VMF15(R)	MK61FX512VMJ15(R)	MK61FN1M0VMJ15(R)
Communication Interfaces						
SDHC	8-bit, CLKIN	8-bit, CLKIN	8-bit, CLKIN	8-bit, CLKIN	8-bit, CLKIN	8-bit, CLKIN
High Baudrate UART w/ ISO7816 + LON	1	1	1	1	1	1
High Baudrate UART w/ ISO7816	1	1	1	1	1	1
High Baudrate UART	0	0	0	0	0	0
UART	4	4	4	4	4	4
SPI chip selects per module	6 / 4 / 2	6 / 4 / 2	6 / 4 / 2	6 / 4 / 2	6 / 4 / 2	6 / 4 / 2
I2C	2	2	2	2	2	2
I2S	2	2	2	2	2	2
I2S0 TX/RX	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2
I2S1 TX/RX	0 / 2	0 / 2	2 / 2	2 / 2	2 / 2	2 / 2
CAN	2	2	2	2	2	2
USB OTG LS/FS w/ on-chip xcvr	1	1	1	1	1	1
USB OTG HS	1	1	1	1	1	1
USB DCD	YES	YES	YES	YES	YES	YES
USB 120mAReg	YES	YES	YES	YES	YES	YES
Ethernet w /1588	MII / RMII	MII / RMII	MII / RMII	MII / RMII	MII / RMII	MII / RMII
IEEE1588 Timer	1x4ch, CLKIN	1x4ch, CLKIN	1x4ch, CLKIN	1x4ch, CLKIN	1x4ch, CLKIN	1x4ch, CLKIN
Human-Machine Interface						
Segment LCD	-	-	-	-	-	-
Graphic LCD	-	-	-	-	-	-
TSI(Capacitive Touch)	16 input	16 input	16 input	16 input	16 input	16 input
GPIO (w interrupt)	95	95	128	128	128	128
5V Tolerant GPIOs	91	91	124	124	124	124
Operating Characteristics						
5V Tolerant	YES	YES	YES	YES	YES	YES
Voltage Range	1.71-3.6V	1.71-3.6V	1.71-3.6V	1.71-3.6V	1.71-3.6V	1.71-3.6V
Flash Write V	1.71V	1.71V	1.71V	1.71V	1.71V	1.71V
Temp Range	-40 to 105C	-40 to 105C	-40 to 105C	-40 to 105C	-40 to 105C	-40 to 105C

4.5 Module-by-module feature list

The following sections describe the high-level module features for the family's superset device. See the previous section for differences among the subset devices.

4.5.1 Core modules

4.5.1.1 ARM Cortex-M4 Core

- Supports up to 150 MHz frequency with 1.25DMIPS/MHz
- ARM Core based on the ARMv7 Architecture & Thumb®-2 ISA
- Microcontroller cores focused on very cost sensitive, deterministic, interrupt driven environments
- Harvard bus architecture
- 3-stage pipeline with branch speculation
- Integrated bus matrix
- Integrated Digital Signal Processor (DSP)
- Configurable nested vectored interrupt controller (NVIC)
- Advanced configurable debug and trace components
- Embedded Trace Macrocell (ETM)
- Optional Single Precision Floating Point Unit (SPFPU)

4.5.1.2 Nested Vectored Interrupt Controller (NVIC)

- Close coupling with Cortex-M4 core's Harvard architecture enables low latency interrupt handling
- Up to 120 interrupt sources
- Includes a single non-maskable interrupt
- 16 levels of priority, with each interrupt source dynamically configurable
- Supports nesting of interrupts when higher priority interrupts are activated
- Relocatable vector table

4.5.1.3 Wake-up Interrupt Controller (WIC)

- Supports interrupt handling when system clocking is disabled in low power modes
- Takes over and emulates the NVIC behavior when correctly primed by the NVIC on entry to very-deep-sleep
- A rudimentary interrupt masking system with no prioritization logic signals for wake-up as soon as a non-masked interrupt is detected
- Contains no programmer’s model visible state and is therefore invisible to end users of the device other than through the benefits of reduced power consumption while sleeping

4.5.1.4 Debug Controller

- Serial Wire JTAG Debug Port (SWJ-DP) combines
  - external interface that provides a standard JTAG or cJTAG interface for debug access
  - external interface that provides a serial-wire bidirectional debug interface
- Debug Watchpoint and Trace (DWT) with the following functionality:
  - four comparators configurable as a hardware watchpoint, an ETM trigger, a PC sampler event trigger, or a data address sampler event trigger

  - several counters or a data match event trigger for performance profiling
  - configurable to emit PC samples at defined intervals or to emit interrupt event information
- Instrumentation Trace Macrocell (ITM) with the following functionality:
  - Software trace - writes directly to ITM stimulus registers can cause packets to be emitted
  - Hardware trace - packets generated by DWT are emitted by ITM
  - Time stamping - emitted relative to packets
- Embedded Trace Macrocell (ETM) supports instruction trace
- CoreSight™ Embedded Trace Buffer (ETB) is a memory-mapped buffer to store trace data. Allows reconstruction of program flow with standard JTAG tools.
- Test Port Interface Unit (TPIU) acts as a bridge between ITM or ETM and an off-chip Trace Port Analyzer
- Flash Patch and Breakpoints (FPB) implements hardware breakpoints and patches code and data from code space to system space

4.5.2 System modules

4.5.2.1 Power Management Control Unit (PMC)

- Separate digital (regulated) and analog (referenced to digital) supply outputs
- Programmable power saving modes
- No output supply decoupling capacitors required
- Available wake-up from power saving modes via RTC and external inputs
- Integrated Power-on Reset (POR)
- Integrated Low Voltage Detect (LVD) with reset (brownout) capability
- Selectable LVD trip points
- Programmable Low Voltage Warning (LVW) interrupt capability
- Buffered bandgap reference voltage output
- Factory programmed trim for bandgap and LVD
- 1 kHz Low Power Oscillator (LPO)

4.5.2.2 DMA Channel Multiplexer (DMA MUX)

- 16 independently selectable DMA channel routers
- 4 periodic trigger sources available
- Each channel router can be assigned to 1 of 63 possible peripheral DMA sources

4.5.2.3 DMA Controller

- Up to 32 fully programmable channels with 32-byte transfer control descriptors
- Data movement via dual-address transfers for 8-, 16-, 32-, 128-, and 256-bit data values
- Programmable source, destination addresses, transfer size, support for enhanced address modes
- Support for major and minor nested counters with one request and one interrupt per channel
- Support for channel-to-channel linking and scatter/gather for continuous transfers with fixed priority and round-robin channel arbitration

4.5.2.4 Watchdog Timer (WDOG)

- Independent, configurable clock source input
- Write-once control bits with unlock sequence
- Programmable timeout period

- Ability to test watchdog timer and reset
- Windowed refresh option
- Robust refresh mechanism
- Cumulative count of watchdog resets between power-on resets
- Configurable interrupt on timeout

4.5.2.5 External Watchdog Monitor (EWM)

- Independent 1 kHz LPO clock source
- Output signal to gate an external circuit which is controlled by CPU service or external input

4.5.2.6 System Clocks

- Frequency-locked loop (FLL)
  - Digitally-controlled oscillator (DCO)
  - DCO frequency range is programmable
  - Option to program DCO frequency for a 32,768 Hz external reference clock source
  - Internal or external reference clock can be used to control the FLL
  - 0.2% resolution using 32 kHz internal reference clock
- Phase-locked loop (PLL)
  - Voltage-controlled oscillator (VCO)
  - External reference clock is used to control the PLL
  - Modulo VCO frequency divider Phase/Frequency detector
  - Integrated loop filter
- Internal reference clock generator
  - Slow clock with nine trim bits for accuracy
  - Fast clock with four trim bits
  - Can be used to control the FLL
  - Either the slow or the fast clock can be selected as the clock source for the MCU
  - Can be used as a clock source for other on-chip peripherals
- External clock from the Crystal Oscillator (XOSC)
  - Can be used to control the FLL and/or the PLL
  - Can be selected as the clock source for the MCU
- External clock monitor with reset request capability
- Lock detector with interrupt request capability for use with the PLL
- Auto Trim Machine (ATM) for trimming both the slow and fast internal reference clocks
- Multiple clock source options available for most peripherals

4.5.3 Memories and Memory Interfaces

4.5.3.1 On-Chip Memory

- Security circuitry to prevent unauthorized access to RAM and flash contents

4.5.3.2 External Bus Interface (FlexBus)

- Six independent, user-programmable chip-select signals that can interface with external SRAM, PROM, EPROM, EEPROM, flash, and other peripherals
- Supports up to 2 GB addressable space

- 8-, 16- and 32-bit port sizes with configuration for multiplexed or non-multiplexed address and data buses
- Byte-, word-, longword-, and 16-byte line-sized transfers
- Programmable address-setup time with respect to the assertion of chip select
- Programmable address-hold time with respect to the negation of chip select and transfer direction

4.5.3.3 Serial Programming Interface (EzPort)

- Same serial interface as, and subset of, the command set used by industry-standard SPI flash memories
- Ability to read, erase, and program flash memory
- Reset command to boot the system after flash programming

4.5.3.4 DDR Controller

- Supports glueless interface to LPDDR, DDR and DDR2 DRAM devices
- Support for 16-bit fixed memory port width
- 16-byte critical word first burst transfer
- Up to 16 lines of row address, up to 16 column address lines, 2 bits of bank address, and up to two chip selects
- Supports up to 256 MByte of memory; minimum memory configuration of 8
- Supports page mode to maximize the data rate
- Supports sleep mode and self-refresh mode

4.5.3.5 NAND Flash Controller

- 8- and 16-bit NAND flash interface
- 9 KB RAM buffer
- Supports flash device commands
- Integrated DMA engine
- Two configurable DMA channels
- Optional ECC mode supports 4/6/8/12/16/24/32-bit error correction

4.5.4 Security and Integrity

4.5.4.1 Cyclic Redundancy Check (CRC)

- Hardware CRC generator circuit using 16/32-bit shift register
- User Configurable 16/32 bit CRC
- Programmable Generator Polynomial
- Error detection for all single, double, odd, and most multi-bit errors
- Programmable initial seed value
- High-speed CRC calculation
- Optional feature to transpose input data and CRC result via transpose register, required on applications where bytes are in lsb format

4.5.4.2 Hardware Cryptographic Acceleration Unit (CAU)

- Supports DES, 3DES, AES, MD5, SHA-1, and SHA-256 algorithms
- Simple C calls to optimized security functions provided by Freescale

4.5.4.3 Random Number Generator (RNG)

- Supports the key generation algorithm defined in the Digital Signature Standard
  - http://www.itl.nist.gov/fipspubs/fip186.htm
- Integrated entropy sources capable of providing the PRNG with entropy for its seed

4.5.4.4 Tamper Detect

- Analog tamper detects (voltage, temperature, and clock)
- External tamper detects
- Active wire-mesh tamper detect
- Internal tamper detects (flash security and secure SRAM)
- Register locks, tamper enables and analog trim configuration bits
- Secure RTC with added support for automatic compensation
- 32-bit monotonic counter
- 256-bit secure storage (asynchronously erased on tamper detect)
- 32- to 256-bit general-purpose storage (not erased)
- Single backup supply
- Voltage monitor
  - Active-low enable (minimum leakage power when disabled)
  - Active-low output which asserts when voltage is lower than 1.5V to 1.62V or higher than 3.6V to 4V
- Temperature monitor
  - Active-low enable (minimum leakage power when disabled)
  - Active-low output which asserts when temperature is lower than -50C to -100C or higher than 125C to 175C
- Clock monitor
  - Active-low enable (minimum leakage power when disabled)
  - Active-low output which asserts when clock < ~16 kHz or > ~1 MHz

4.5.5 Analog

4.5.5.1 16-bit Analog-to-Digital Converter (ADC)

- Linear successive approximation algorithm with up to 16-bit resolution
- Output modes:
  - Differential 16-bit, 13-bit, 11-bit, and 9-bit modes, in two’s complement 16-bit sign-extended format
  - Single-ended 16-bit, 12-bit, 10-bit, and 8-bit modes, in right-justified unsigned format
- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Conversion complete and hardware average complete flag and interrupt
- Input clock selectable from up to four sources
- Operation in low power modes for lower noise operation
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable asynchronous hardware conversion trigger with hardware channel select
- Automatic compare with interrupt for various programmable values
- Temperature sensor
- Hardware average function
- Selectable voltage reference
- Self-calibration mode

4.5.5.2 High-Speed Analog Comparator (CMP)

- 6-bit DAC programmable reference generator output
- Up to eight selectable comparator inputs; each input can be compared with any input by any polarity sequence
- Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
- Comparator output supports:
  - Sampled
  - Windowed (ideal for certain PWM zero-crossing-detection applications
  - Digitally filtered using external sample signal or scaled peripheral clock
- Two performance modes:
  - Shorter propagation delay at the expense of higher power
  - Low power, with longer propagation delay
- Operational in all MCU power modes

4.5.5.3 12-Bit Digital-to-Analog Converter (DAC)

- 12-bit resolution
- Guaranteed 6-sigma monotocity over input word
- High- and low-speed conversions
  - 1 µs conversion rate for high speed, 2 µs for low speed
- Power-down mode
- Choice of asynchronous or synchronous updates
- Automatic mode allows the DAC to generate its own output waveforms including square, triangle, and sawtooth
- Automatic mode allows programmable period, update rate, and range
- DMA support with configurable watermark level

4.5.5.4 Voltage Reference (VREF)

- Programmable trim register with 0.5mV steps, automatically loaded with room temp value upon reset
- Programmable mode selection:
  - Off
  - Bandgap out (or stabilization delay)
  - Tight-regulation buffer mode
- 1.2V output at room temperature
- Dedicated output pin

4.5.6 Timers

4.5.6.1 Programmable Delay Block (PDB)

- Up to 15 trigger input sources and software trigger source
- Up to eight configurable PDB channels for ADC hardware trigger
  - One PDB channel is associated with one ADC.
  - One trigger output for ADC hardware trigger and up to eight pre-trigger outputs for ADC trigger select per PDB channel
  - Trigger outputs can be enabled or disabled independently.
  - One 16-bit delay register per pre-trigger output
  - Optional bypass of the delay registers of the pre-trigger outputs
  - Operation in One-Shot or Continuous modes

  - Optional back-to-back mode operation, which enables the ADC conversions complete to trigger the next PDB channel
  - One programmable delay interrupt
  - One sequence error interrupt
  - One channel flag and one sequence error flag per pre-trigger
  - DMA support
- Up to eight DAC interval triggers
  - One interval trigger output per DAC
  - One 16-bit delay interval register per DAC trigger output
  - Optional bypass the delay interval trigger registers
  - Optional external triggers
- Up to eight pulse outputs (pulse-out's)
  - Pulse-out's can be enabled or disabled independently.
  - Programmable pulse width

4.5.6.2 FlexTimers (FTM)

- Selectale FTM source clock
- Programmable prescaler
- 16-bit counter supporting free-running or initial/final value, and counting is up or up-down
- Input capture, output compare, and edge-aligned and center-aligned PWM modes
- Input capture and output compare modes
- Operation of FTM channels as pairs with equal outputs, pairs with complimentary outputs, or independent channels with independent outputs
- Deadtime insertion is available for each complementary pair
- Generation of hardware triggers
- Software control of PWM outputs
- Up to 4 fault inputs for global fault control
- Configurable channel polarity
- Programmable interrupt on input capture, reference compare, overflowed counter, or detected fault condition
- Quadrature decoder with input filters, relative position counting, and interrupt on position count or capture of position count on external event
- DMA support for FTM events
- Global time base mode shares single time base across multiple FTM instances

4.5.6.3 Programmable Interrupt Timers (PITs)

- Up to 4 general purpose interrupt timers
- Up to 4 interrupt timers for triggering ADC conversions
- 32-bit counter resolution
- Clocked by system clock frequency
- DMA support

4.5.6.4 Low Power Timer

- Operation as timer or pulse counter
- Selectable clock for prescaler/glitch filter
  - 1 kHz internal LPO
  - External low power crystal oscillator
  - Internal reference clock (not available in low leakage power modes)
  - Secondary external reference clock (for example, 32 kHz crystal)
- Configurable glitch filter or prescaler

- Interrupt generated on timer compare
- Hardware trigger generated on timer compare

4.5.6.5 Carrier Modulator Timer (CMT)

- Four modes of operation
  - Time with independent control of high and low times
  - Baseband
  - Frequency shift key (FSK)
  - Direct software control of CMT_IRO signal
- Extended space operation in time, baseband, and FSK modes
- Selectable input clock divider
- Interrupt on end of cycle
- Ability to disable CMT_IRO signal and use as timer interrupt

4.5.6.6 Real-Time Clock (RTC)

- Independent power supply, POR and 32 kHz crystal oscillator
- 32-bit seconds counter with 32-bit alarm
- 16-bit prescaler with compensation
- Register write protection
  - Hard Lock requires VBAT POR to enable write access
  - Soft lock requires system reset to enable write/read access

4.5.7 Communication interfaces

4.5.7.1 10/100Mbps Ethernet MAC

- Ethernet controller with 10/100 BaseT/TX capability; half duplex or full duplex
  - Hardware support for *IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems*, IEEE 1588
  - Media independent interface (MII) and reduced media independent interface (RMII) support
- Built-in unified DMA
  - On-chip transmit and receive FIFOs
  - Supports legacy buffer descriptor programming models and functionality
  - Enchanced buffer descriptor programming model for new Ethernet functionality
- Supports wake-up from low power mode through magic packets
- Multiple clock source options for time-stamping clock

4.5.7.2 USB On-The-Go Module (FS/LS)

- Complies with USB specification rev 2.0
- USB host mode
  - Supports enhanced-host-controller interface (EHCI)
  - Allows direct connection of FS/LS devices without an OHCI/UHCI companion controller
  - Supported by Linux and other commercially available operating systems
- USB device mode
  - Full-speed operation via the on-chip transceiver
  - Supports one upstream facing port
  - Supports four programmable, bidirectional USB endpoints, including endpoint 0

- Suspend mode/low power
  - As host, firmware can suspend individual devices or the entire USB and disable chip clocks for low-power operation
  - Device supports low-power suspend
  - Remote wake-up supported for host and device
  - Integrated with the processor's low power modes
- Includes an on-chip full-speed (12 Mbps) and low-speed (1.5 Mbps) transceiver

4.5.7.3 USB Device Charger Detect (USBDCD)

- Compatible with systems powered from:
  - Rechargable battery
  - Non-rechargable battery
  - External 3.3v LDO regulator powered from USB or
  - Directly from USB using internal regulator
- Programmable event timers for flexibility and better compatibility with future udpates to the standards
- Compliant with the latest industry standard specification, USB Battery Charging Specification, Revision 1.1

4.5.7.4 USB Voltage Regulator

- 5V regulator input typically provided by USB VBUS power
- 3.3V regulated output powers on-chip USB transceiver
- Output pin from regulator can be used to power external board components and source up to 120mA
- Eliminates cost of external LDO
- 3.3V regulated output can power MCU main power supply

4.5.7.5 USB On-The-Go Module (HS/FS/LS)

- Complies with USB specification rev 2.0
- USB host mode
  - Supports enhanced-host-controller interface (EHCI)
  - HS/FS/LS operation via an external ULPI transceiver
  - Supported by Linux and other commercially available operating systems
- USB device mode
  - HS/FS operation via an external ULPI transceiver
  - Supports one upstream facing port
  - Supports four programmable, bidirectional USB endpoints, including endpoint 0
- Suspend mode/low power
  - As host, firmware can suspend individual devices or the entire USB and disable chip clocks for low-power operation
  - Device supports low-power suspend
  - Remote wake-up supported for host and device
  - Integrated with the processor's low power modes
- Support for off-chip HS/FS/LS transceiver
  - External ULPI transceiver supports high speed (480 Mbps), full speed, and low speed operation in host mode, and high-speed and full-speed operation in device mode
  - Interface uses 8-bit single-data-rate ULPI data bus
  - ULPI PHY supplies a 60 MHz USB reference clock input to the processor

4.5.7.6 CAN Module

- Supports the full implementation of the *CAN Specification Version 2.0, Part B*
  - Standard data and remote frames (up to 109 bits long)
  - Extended data and remote frames (up to 127 bits long)
  - 0–8 bytes data length
  - Programmable bit rate up to 1 Mbit/sec
  - Content-related addressing
- Flexible message buffers (MBs), totalling up to 16 message buffers of 0–8 bytes data length each, configurable as Rx or Tx, all supporting standard and extended messages
- Listen-only mode capability
- Individual mask registers for each message buffer
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Timestamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message

4.5.7.7 Serial Peripheral Interface (SPI)

- Master and slave mode
- Full-duplex, three-wire synchronous transfers
- Programmable transmit bit rate
- Double-buffered transmit and receive data registers
- Serial clock phase and polarity options
- Slave select output
- Mode fault error flag with CPU interrupt capability
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting
- Programmable 8-bit or 16-bit data transmission length
- Receive data buffer hardware match feature
- 64-bit FIFO mode for high speed transfers of large amounts of data
- Support for both transmit and receive by DMA

4.5.7.8 Inter-Integrated Circuit (I^2C)

- Compatible with I^2C bus standard and *SMBus Specification Version 2* features
- Up to 100 kbps with maximum bus loading
- Multi-master operation
- Software programmable for one of 64 different serial clock frequencies
- Programmable slave address and glitch input filter
- Interrupt or DMA driven byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Bus busy detection broadcast and 10-bit address extension
- Address matching causes wake-up when processor is in low power mode

4.5.7.9 UART

- Support for ISO 7816 protocol for interfacing with smartcards
- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse width
- 13-bit baud rate selection with fractional divide of 32
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Programmable transmitter output polarity

- Programmable receive input polarity
- 13-bit break character option
- 11-bit break character detection option
- Parameterizable buffer support for one dataword for each transmit and receive
- Independent FIFO structure for transmit and receive
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Address match feature in receiver to reduce address mark wakeup ISR overhead
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- Support for CEA709.1-B protocol (LON) used in building automation and home networking systems
- Interrupt or DMA driven operation
- Receiver framing error detection
- Hardware parity generation and checking
- 1/16 bit-time noise detection

4.5.7.10 Secure Digital Host Controller (SDHC)

- Compatible with the following specifications:
  - *SD Host Controller Standard Specification, Version 2.0* (http://www.sdcard.org) with test event register and advanced DMA support
  - *MultiMediaCard System Specification, Version 4.2* (http://www.mmca.org)
  - *SD Memory Card Specification, Version 2.0* (http://www.sdcard.org), supporting high capacity SD memory cards
  - *SDIO Card Specification, Version 2.0* (http://www.sdcard.org)
  - *CE-ATA Card Specification, Version 1.0* (http://www.sdcard.org)
- Designed to work with CE-ATA, SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMCplus, and RS-MMC cards
- SD bus clock frequency up to 50 MHz
- Supports 1-/4-bit SD and SDIO modes, 1-/4-/8-bit MMC modes, 1-/4-/8-bit CE-ATA devices
- Up to 200 Mbps data transfer for SD/SDIO cards using four parallel data lines
- Up to 416 Mbps data transfer for MMC using 8 parallel data lines
- Single- and multi-block read and write
- 1-4096 byte block size
- Write-protection switch for write operations
- Synchronous and asynchronous abort
- Pause during the data transfer at a block gap
- SDIO read wait and suspend/resume operations
- Auto CMD12 for multi-block transfer
- Host can initiate non-data transfer commands while the data transfer is in progress
- Allows cards to interrupt the host in 1- and 4-bit SDIO modes
- Supports interrupt period, defined in the SDIO standard
- Fully configurable 128 x 32-bit FIFO for read/write data
- Internal DMA capabilities
- Supports voltage selection by configuring vendor specific register bit
- Supports advanced DMA to perform linked memory access

4.5.7.11 Synchronous Serial Interface (I2S)

- Independent (asynchronous) or shared (synchronous) transmit and receive sections with separate or shared internal/external clocks and frame syncs, operating in master or slave mode intended for audio support
- Master or slave mode operation
- Normal mode operation using frame sync

- Network mode operation allowing multiple devices to share the port with up to 32 time slots
- Programmable data interface modes, such as I^2S, LSB aligned, and MSB aligned
- Programmable word length (8, 10, 12, 16, 18, 20, 22 or 24 bits)
- AC97 support

4.5.8 Human-machine interface

4.5.8.1 General Purpose Input/Output (GPIO)

- Progammable glitch filter and interrupt with selectable polarity on all input pins
- Hysteresis and configurable pull up/down device on all input pins
- Configurable slew rate and drive strength on all output pins
- Independent pin value register to read logic level on digital pin
- Optional devices with 5V tolerance

4.5.8.2 Touch Sensor Input (TSI)

- 16 channel inputs, supporting up to 16 individual touch buttons
- 4 touch buttons can be combined for a slider
- Configurable button- and slider-sensitive interrupts
- Operation in low-power modes allows wakeup from lowest power mode via a single touch
- Option to use internal reference clock

5 Power modes

The power management controller (PMC) provides multiple power options to allow the user to optimize power consumption for the level of functionality needed.

Depending on the stop requirements of the user application, a variety of stop modes are available that provide state retention, partial power down or full power down of certain logic and/or memory. I/O states are held in all modes of operation. The following table compares the various power modes available.

For each run mode there is a corresponding wait and stop mode. Wait modes are similar to ARM sleep modes. Stop modes (VLPS, STOP) are similar to ARM sleep deep mode. The very low power run (VLPR) operating mode can drastically reduce runtime power when the maximum bus frequency is not required to handle the application needs.

The three primary modes of operation are run, wait and stop. The WFI instruction invokes both wait and stop modes for the chip. The primary modes are augmented in a number of ways to provide lower power based on application needs.

Table 5. Chip power modes

Chip mode	Description	Core mode	Normal recovery method
Normal run	Allows maximum performance of chip. Default mode out of reset; on-chip voltage regulator is on.	Run	-
Normal Wait - via WFI	Allows peripherals to function while the core is in sleep mode, reducing power. NVIC remains sensitive to interrupts; peripherals continue to be clocked.	Sleep	Interrupt

Table continues on the next page...

Table 5. Chip power modes (continued)

Chip mode	Description	Core mode	Normal recovery method
Normal Stop - via WFI	Places chip in static state. Lowest power mode that retains all registers while maintaining LVD protection. NVIC is disabled; AWIC is used to wake up from interrupt; peripheral clocks are stopped.	Sleep Deep	Interrupt
VLPR (Very Low Power Run)	On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency. Reduced frequency Flash access mode (1 MHz); LVD off; internal oscillator provides a low power 4 MHz source for the core, the bus and the peripheral clocks.	Run	Interrupt
VLPW (Very Low Power Wait) -via WFI	Same as VLPR but with the core in sleep mode to further reduce power; NVIC remains sensitive to interrupts (FCLK = ON). On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency.	Sleep	Interrupt
VLPS (Very Low Power Stop)-via WFI	Places chip in static state with LVD operation off. Lowest power mode with ADC and pin interrupts functional. Peripheral clocks are stopped, but LPTimer, RTC, CMP, TSI, DAC can be used. NVIC is disabled (FCLK = OFF); AWIC is used to wake up from interrupt. On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency. All SRAM is operating (content retained and I/O states held).	Sleep Deep	Interrupt
LLS (Low Leakage Stop)	State retention power mode. Most peripherals are in state retention mode (with clocks stopped), but LLWU, LPTimer, RTC, CMP, TSI, DAC can be used. NVIC is disabled; LLWU is used to wake up. **NOTE:** The LLWU interrupt must not be masked by the interrupt controller to avoid a scenario where the system does not fully exit stop mode on an LLS recovery. All SRAM is operating (content retained and I/O states held).	Sleep Deep	Wakeup Interrupt[1]
VLLS3 (Very Low Leakage Stop3)	Most peripherals are disabled (with clocks stopped), but LLWU, LPTimer, RTC, CMP, TSI, DAC can be used. NVIC is disabled; LLWU is used to wake up. SRAM_U and SRAM_L remain powered on (content retained and I/O states held).	Sleep Deep	Wakeup Reset[2]
VLLS2 (Very Low Leakage Stop2)	Most peripherals are disabled (with clocks stopped), but LLWU, LPTimer, RTC, CMP, TSI, DAC can be used. NVIC is disabled; LLWU is used to wake up. SRAM_L is powered off. A portion of SRAM_U remains powered on (content retained and I/O states held).	Sleep Deep	Wakeup Reset[2]
VLLS1 (Very Low Leakage Stop1)	Most peripherals are disabled (with clocks stopped), but LLWU, LPTimer, RTC, CMP, TSI, DAC can be used. NVIC is disabled; LLWU is used to wake up. All of SRAM_U and SRAM_L are powered off. The 32-byte system register file and the 32-byte VBAT register file remain powered for customer-critical data.	Sleep Deep	Wakeup Reset[2]
BAT (backup battery only)	The chip is powered down except for the VBAT supply. The RTC and the 32-byte VBAT register file for customer-critical data remain powered.	Off	Power-up Sequence

1. Resumes normal run mode operation by executing the LLWU interrupt service routine.
2. Follows the reset flow with the LLWU interrupt flag set for the NVIC.

6 Developer Environment

Freescale's products are supported by a widespread, established network of tools and third party developers and software vendors. The Kinetis families take advantage of these and similar development resources.

6.1 Freescale's Tower System Support

Freescale's Tower System is a modular development platform for 8-bit, 16-bit, and 32-bit microcontrollers that enables advanced development through rapid prototyping. Featuring multiple development boards or modules, the Tower System provides designers with building blocks for entry-level to advanced microcontroller development.

The Freescale Tower System

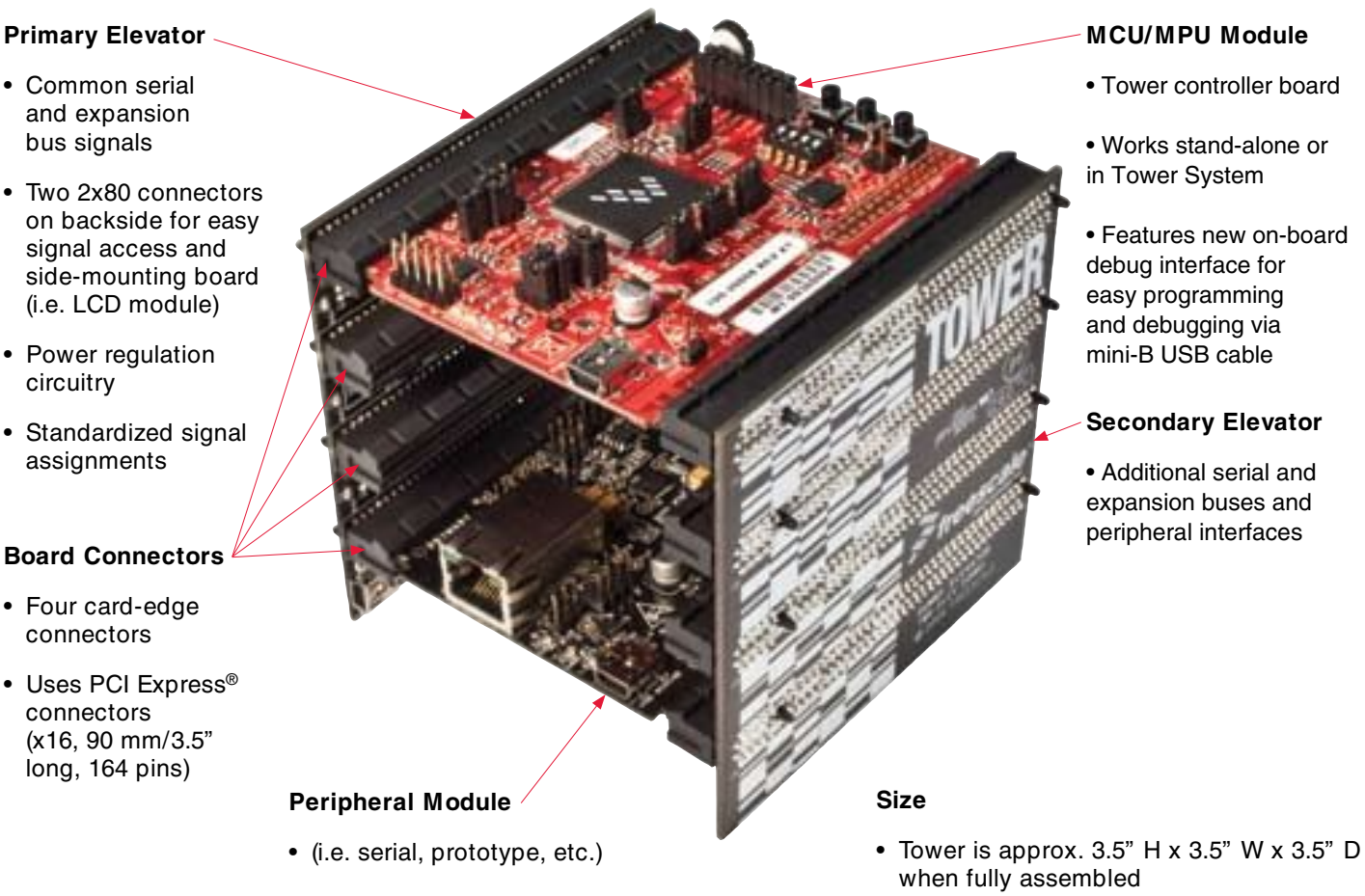


Figure 4. Freescale's Tower System

The following Tower modules are available for the Kinetis families. For more information on the Tower System see http://www.freescale.com/tower.

Table 6. Tower Modules for Kinetis MCU Families

Microcontroller Modules	Features
Kinetis K70 Family MCU Module	K70 family 1 MB flash MCU in 256 MAPBGA package On-board JTAG debug interface Access to all features including Ethernet, USB, and graphical LCD
Kinetis K60 Family MCU Module	K60 family 1MB flash MCU in 144 LQFP package On-board JTAG debug interface Access to all features including Ethernet, USB, and graphical LCD
Kinetis K40 Family MCU Module	K40 family 512 KB flash MCU in 144 MAPBGA package On-board JTAG debug interface Access to all features including Segment LCD and USB
Kinetis K60 Family MCU Module	K60 family 512 KB flash MCU in 144 MAPBGA package On-board JTAG debug interface Access to all features including Ethernet and USB
Kinetis K53 Family MCU Module	K53 family 512 KB flash MCU in 144 MAPBGA package On-board JTAG debug interface Access to all features including Ethernet, USB, Segment LCD (TWRPI), and medical expansion connector

6.2 CodeWarrior Development Studio

Freescale's CodeWarrior Development Studio for Microcontrollers v10.x integrates the development tools for the RS08, HCS08, ARM, and ColdFire architectures into a single product based on the Eclipse open development platform. Eclipse offers an excellent framework for building software development environments and is becoming a standard framework used by many embedded software vendors.

- Eclipse IDE 3.4
- Build system with optimizing C/C++ compilers for RS08, HCS08, ARM, and ColdFire processors
- Extensions to Eclipse C/C++ Development Tools (CDT) to provide sophisticated features to troubleshoot and repair embedded applications

Table 7. CodeWarrior 10.x Differentiating Features

Differentiating features	Customer benefits	Details
MCU Change Wizard	Ability to easily retarget project to a new processor	Simply select a new device (from the same or a different architecture) and select the default connection, and the CodeWarrior tool suite automatically reconfigures the project for the new device with the correct build tools and support files. • Compiler • Assembler • Linker • Header files • Vector tables • Libraries • Linker configuration files

Table continues on the next page...

Table 7. CodeWarrior 10.x Differentiating Features (continued)

Differentiating features	Customer benefits	Details
Freescale Processor Expert	Problems in hardware layer can be resolved during initial design phase	Combines easy-to-use component-based application creation with an expert knowledge system. • CPU, on-chip peripherals, external peripherals, and software functionality are encapsulated into embedded components • Each component's functionality can be tailored to fit application requirements by modifying the component's properties, methods and events • When the project is built, Processor Expert automatically generates highly optimized embedded C code and places the source files into the project • Graphical user interface: Allows an application to be specified by the functionality needed • Automatic code generator: Creates tested, optimized C code tuned to application needs and the selected Freescale device • Built-in knowledgebase: Immediately flags resource conflicts and incorrect settings, so errors are caught early in design cycle • Component wizard: Allows user-specific, hardware-independent embedded components to be created
Trace and profile support for on-chip trace buffers	Sophisticated emulator-like debug capability without additional hardware	The CodeWarrior profiling and analysis tools provide visibility into an application as it runs on the processor to identify operational problems. • Supports architectures with on-chip trace buffers (HCS08, V1 ColdFire, ARM) • Allows tracepoints to be set to enable and disable trace output • Can step through trace data and the corresponding source code simultaneously • Allows trace data to be exported into a Microsoft® Excel® file

For more information see the CodeWarrior web site at http://www.freescale.com/codewarrior.

6.3 Freescale's MQX™ Software Solutions

The increasing complexity of industrial applications and expanding functionality of semiconductors are driving embedded developers toward solutions that combine proven hardware and software platforms. These solutions help accelerate time to market and improve application development success.

Freescale Semiconductor offers the MQX real-time operating system (RTOS), with TCP/IP and USB software stacks and peripheral drivers, to customers of ARM, ColdFire and ColdFire+ MCUs at no additional charge. The combination of Freescale's MQX software solutions and Freescale's silicon portfolio creates a comprehensive source for hardware, software, tools, and services.

Freescale Comprehensive Solution

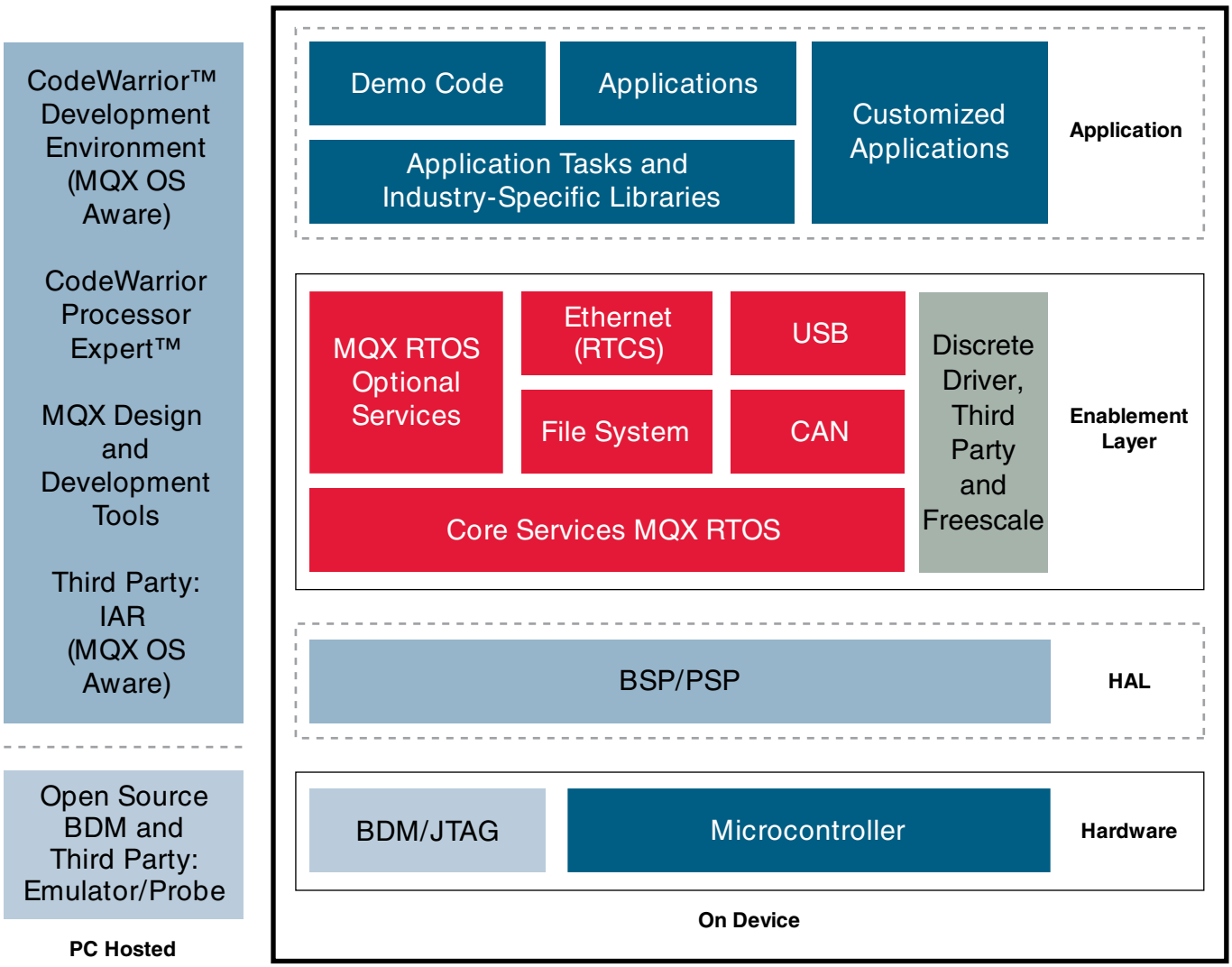


Figure 5. MQX Comprehensive Solution

Key benefits of Freescale's MQX RTOS include:

- Small memory footprint: The RTOS was designed for speed and size efficiency in embedded systems. It delivers true real-time performance, with context switching and low-level interrupt routines hand-optimized in assembly.
- Component-based architecture: Provides a fully-functional RTOS core with additional, optional services. Freescale's MQX RTOS includes 25 components (8 core components and 17 optional). Components are linked in only if needed, preventing unused functions from bloating the memory footprint.
- Full and lightweight components: Key components are included in both full and lightweight versions for further control of size, RAM/ROM utilization, and performance options.
- Real-time, priority-based, preemptive multithreading: Allows high-priority threads to meet their deadlines consistently, no matter how many other threads are competing for CPU time.
- Scheduling: Enables faster development time by offloading from developers the task of creating or maintaining an efficient scheduling system and interrupt handling.
- Code reuse: Provides a framework with a simple, intuitive API to build and organize the features across Freescale's broad portfolio of embedded processors.

- Fast boot sequence: Ensures the application is running quickly after the hardware has been reset.
- Simple Message Passing: Messages can be passed either from a system pool or a private pool, sent with either urgent status or a user-defined priority, and broadcast or task specific. For maximum flexibility, a receiving task can operate on either the same CPU as the sending task or on a different CPU within the same system.

For more information see the MQX web site at http://www.freescale.com/mqx.

MQX RTOS—Customizable Component Set

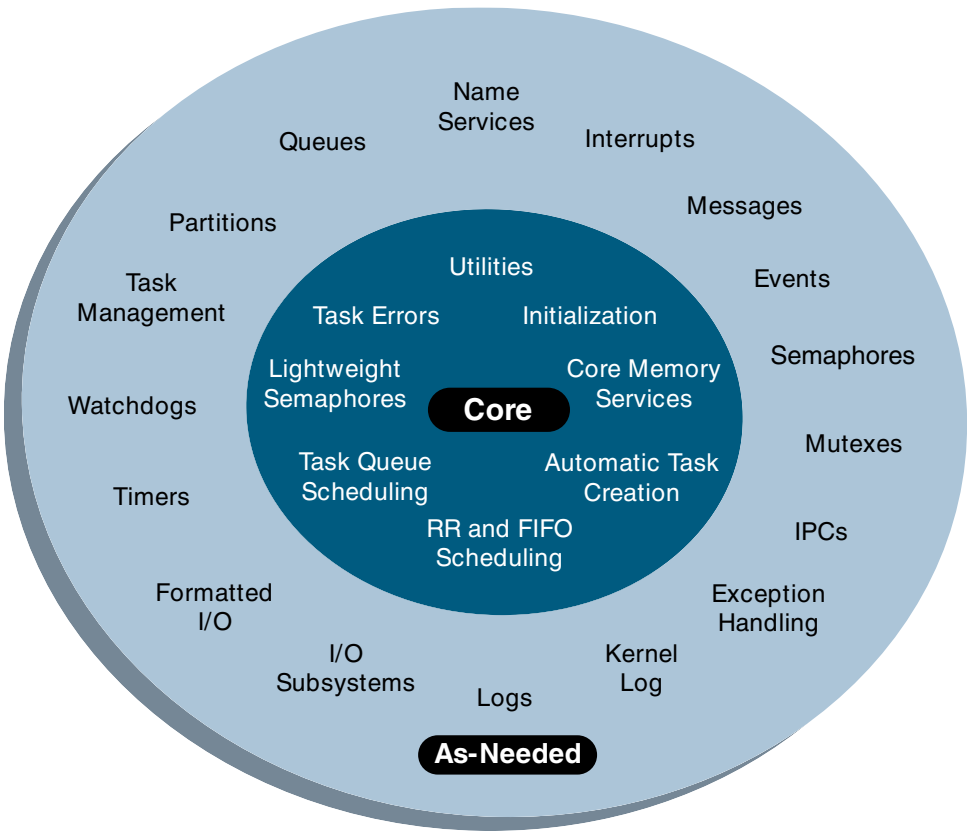


Figure 6. MQX Customizable Component Set

6.4 Additional Software Stacks Provided

- Math, DSP and Encryption Libraries
- Motor Control Libraries
- Touch Sensing Software Suite
- Complimentary Bootloaders (USB, Ethernet, RF, serial)
- Complimentary Freescale Embedded GUI
- Complimentary Freescale MQX™ RTOS , USB, TCP/IP stack and MFS filesystem
- Low Cost Nano™ SSL/Nano™ SSH for Freescale MQX™ RTOS
- Plus full ARM® ecosystem

7 Revision History

The following table provides a revision history for this document.

Table 8. Revision History

Rev. No.	Date	Substantial Changes
9	12/2011	Initial public revision

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: K61PB
Rev. 9, 12/2011