25AA02E48

2K SPI Bus Serial EEPROM with EUI-48™ Node Identity

Device Selection Table

Part Number	Vcc Range	Page Size	Temp. Ranges	Packages
25AA02E48	1.8-5.5V	16 Bytes	I	SN, OT

Features:

- Pre-programmed Globally Unique, 48-bit Node Address
- Compatible with EUI-48™ and EUI-64™
- 10 MHz max. Clock Frequency
- Low-Power CMOS Technology:
  - Max. Write Current: 5 mA at 5.5V
  - Read Current: 5 mA at 5.5V, 10 MHz
  - Standby Current: 1 μA at 2.5V
- 256 x 8-bit Organization
- Write Page mode (up to 16 bytes)
- Sequential Read
- Self-Timed Erase and Write Cycles (5 ms max.)
- Block Write Protection:
  - Protect none, 1/4, 1/2 or all of array
- Built-in Write Protection:
  - Power-on/off data protection circuitry
  - Write enable latch
  - Write-protect pin
- High Reliability:
  - Endurance: 1,000,000 erase/write cycles
  - Data retention: >200 years
  - ESD protection: >4000V
- Temperature Ranges Supported:
  - Industrial (I): -40°C to +85°C
- Pb-Free and RoHS Compliant

Pin Function Table

Name	Function
$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write-Protect
VSS	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Hold Input
VCC	Supply Voltage

Description:

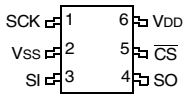
The Microchip Technology Inc. 25AA02E48 is a 2 Kbit Serial Electrically Erasable Programmable Read-Only Memory (EEPROM). The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select ($\overline{CS}$) input.

Communication to the device can be paused via the hold pin ($\overline{HOLD}$). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

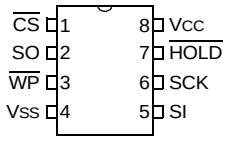
The 25AA02E48 is available in the standard 8-lead SOIC and 6-lead SOT-23 packages.

Package Types (not to scale)

SOT-23
(OT)



SOIC
(SN)



Note: This document is supplemented by the "*25AA020A Data Sheet*" (DS21833). See **Section 2.0 "Functional Description"**.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature .....-65°C to 150°C

Ambient temperature under bias.....-40°C to 85°C

ESD protection on all pins.....4 kV

† NOTICE**:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial (I): TA = -40°C to +85°C VCC = 1.8V to 5.5V			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
D001	VIH1	High-level Input voltage	0.7 VCC	VCC +1	V	
D002	VIL1	Low-level Input Voltage	-0.3	0.3 VCC	V	VCC ≥ 2.7V **(Note 1)**
D003	VIL2		-0.3	0.2 VCC	V	VCC < 2.7V **(Note 1)**
D004	VOL	Low-level Output Voltage	—	0.4	V	IOL = 2.1 mA
D005	VOL		—	0.2	V	IOL = 1.0 mA, VCC < 2.5V
D006	VOH	High-level Output Voltage	VCC -0.5	—	V	IOH = -400 µA
D007	ILI	Input Leakage Current	—	±1	µA	$\overline{CS}$ = VCC, VIN = VSS TO VCC
D008	ILO	Output Leakage Current	—	±1	µA	$\overline{CS}$ = VCC, VOUT = VSS TO VCC
D009	CINT	Internal Capacitance (all inputs and outputs)	—	7	pF	TA = 25°C, CLK = 1.0 MHz, VCC = 5.0V **(Note 1)**
D010	ICC Read	Operating Current	—	5	mA	VCC = 5.5V; FCLK = 10.0 MHz; SO = Open
			—	2.5	mA	VCC = 2.5V; FCLK = 5.0 MHz; SO = Open
D011	ICC Write		—	5	mA	VCC = 5.5V
			—	3	mA	VCC = 2.5V
D012	ICCS	Standby Current	—	1	µA	$\overline{CS}$ = VCC = 2.5V, Inputs tied to VCC or VSS, TA = +85°C

Note: This parameter is periodically sampled and not 100% tested.

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TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial (I): T_A = -40°C to +85°C V_{CC} = 1.8V to 5.5V			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
1	F_{CLK}	Clock Frequency	— — —	10 5 3	MHz MHz MHz	4.5V ≤ V_{CC} < 5.5V 2.5V ≤ V_{CC} < 4.5V 1.8V ≤ V_{CC} < 2.5V
2	T_{CSS}	$\overline{CS}$ Setup Time	50 100 150	— — —	ns ns ns	4.5V ≤ V_{CC} < 5.5V 2.5V ≤ V_{CC} < 4.5V 1.8V ≤ V_{CC} < 2.5V
3	T_{CSH}	$\overline{CS}$ Hold Time	100 200 250	— — —	ns ns ns	4.5V ≤ V_{CC} < 5.5V 2.5V ≤ V_{CC} < 4.5V 1.8V ≤ V_{CC} < 2.5V
4	T_{CSD}	$\overline{CS}$ Disable Time	50	—	ns	—
5	Tsu	Data Setup Time	10 20 30	— — —	ns ns ns	4.5V ≤ V_{CC} < 5.5V 2.5V ≤ V_{CC} < 4.5V 1.8V ≤ V_{CC} < 2.5V
6	T_{HD}	Data Hold Time	20 40 50	— — —	ns ns ns	4.5V ≤ V_{CC} < 5.5V 2.5V ≤ V_{CC} < 4.5V 1.8V ≤ V_{CC} < 2.5V
7	T_R	CLK Rise Time	—	100	ns	**(Note 1)**
8	T_F	CLK Fall Time	—	100	ns	**(Note 1)**
9	T_{HI}	Clock High Time	50 100 150	— — —	ns ns ns	4.5V ≤ V_{CC} < 5.5V 2.5V ≤ V_{CC} < 4.5V 1.8V ≤ V_{CC} < 2.5V
10	T_{LO}	Clock Low Time	50 100 150	— — —	ns ns ns	4.5V ≤ V_{CC} < 5.5V 2.5V ≤ V_{CC} < 4.5V 1.8V ≤ V_{CC} < 2.5V
11	T_{CLD}	Clock Delay Time	50	—	ns	—
12	T_{CLE}	Clock Enable Time	50	—	ns	—
13	T_V	Output Valid from Clock Low	— — —	50 100 160	ns ns ns	4.5V ≤ V_{CC} < 5.5V 2.5V ≤ V_{CC} < 4.5V 1.8V ≤ V_{CC} < 2.5V
14	T_{HO}	Output Hold Time	0	—	ns	**(Note 1)**
15	T_{DIS}	Output Disable Time	— — —	40 80 160	ns ns ns	4.5V ≤ V_{CC} < 5.5V **(Note 1)** 2.5V ≤ V_{CC} < 4.5V **(Note 1)** 1.8V ≤ V_{CC} < 2.5V **(Note 1)**
16	T_{HS}	$\overline{HOLD}$ Setup Time	20 40 80	— — —	ns ns ns	4.5V ≤ V_{CC} < 5.5V 2.5V ≤ V_{CC} < 4.5V 1.8V ≤ V_{CC} < 2.5V

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at www.Microchip.com.

3: T_{WC} begins on the rising edge of $\overline{CS}$ after a valid write sequence and ends when the internal write cycle is complete.

TABLE 1-2: AC CHARACTERISTICS (CONTINUED)

AC CHARACTERISTICS			Industrial (I): T_A = -40°C to +85°C V_{CC} = 1.8V to 5.5V			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
17	T_{HH}	$\overline{HOLD}$ Hold Time	20 40 80	— — —	ns ns ns	4.5V ≤ V_{CC} < 5.5V 2.5V ≤ V_{CC} < 4.5V 1.8V ≤ V_{CC} < 2.5V
18	T_{HZ}	$\overline{HOLD}$ Low to Output High-Z	30 60 160	— — —	ns ns ns	4.5V ≤ V_{CC} < 5.5V **(Note 1)** 2.5V ≤ V_{CC} < 4.5V **(Note 1)** 1.8V ≤ V_{CC} < 2.5V **(Note 1)**
19	T_{HV}	$\overline{HOLD}$ High to Output Valid	30 60 160	— — —	ns ns ns	4.5V ≤ V_{CC} < 5.5V 2.5V ≤ V_{CC} < 4.5V 1.8V ≤ V_{CC} < 2.5V
20	T_{WC}	Internal Write Cycle Time (byte or page)	—	5	ms	**(Note 3)**
21	—	Endurance	1M	—	E/W Cycles	**(NOTE 2)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at www.Microchip.com.

3: T_{WC} begins on the rising edge of $\overline{CS}$ after a valid write sequence and ends when the internal write cycle is complete.

TABLE 1-3: AC TEST CONDITIONS

AC Waveform:	
V_{LO} = 0.2V	—
V_{HI} = V_{CC} - 0.2V	**(Note 1)**
V_{HI} = 4.0V	**(Note 2)**
C_L = 100 pF	—
Timing Measurement Reference Level	
Input	0.5 V_{CC}
Output	0.5 V_{CC}

Note 1: For V_{CC} ≤ 4.0V

2: For V_{CC} > 4.0V

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FIGURE 1-1: HOLD TIMING

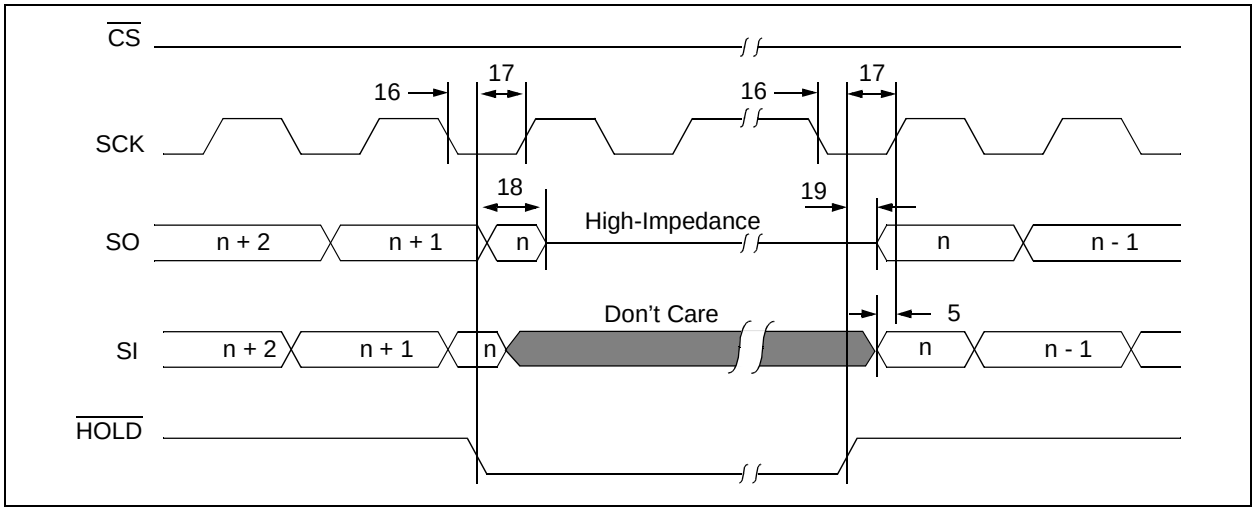


FIGURE 1-2: SERIAL INPUT TIMING

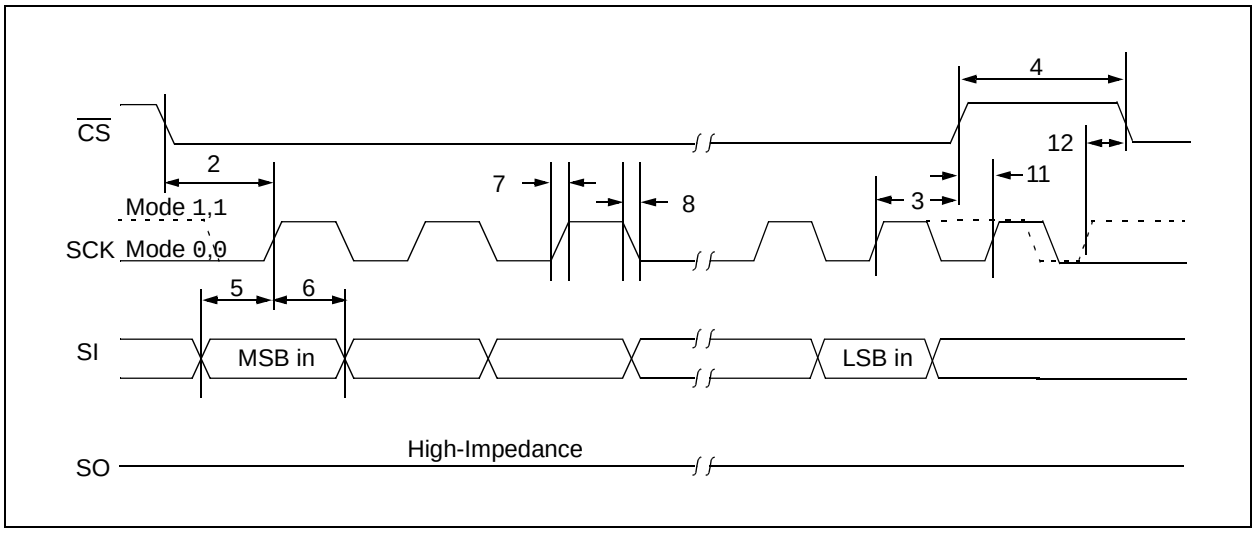
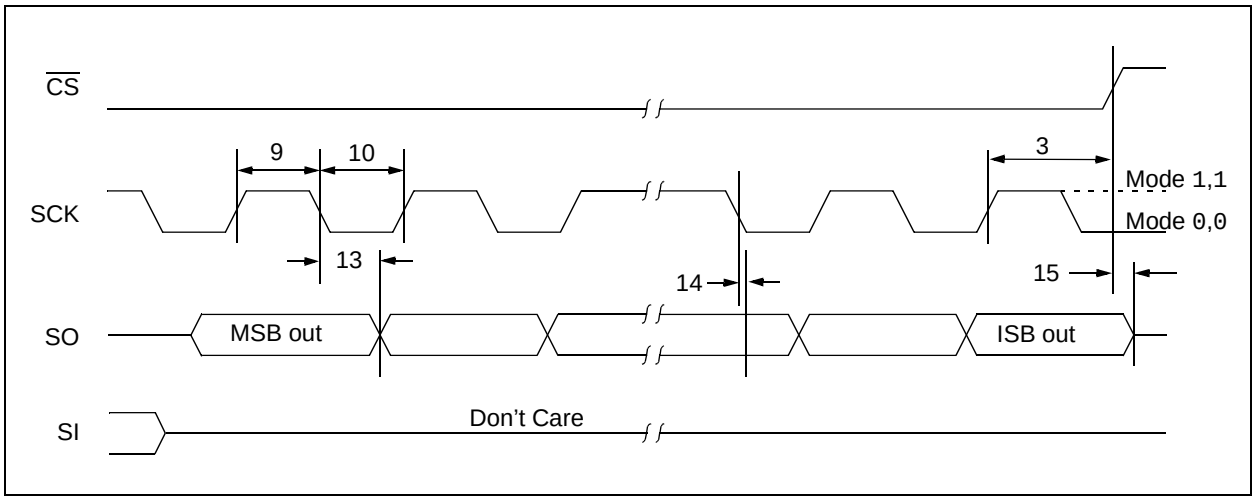


FIGURE 1-3: SERIAL OUTPUT TIMING

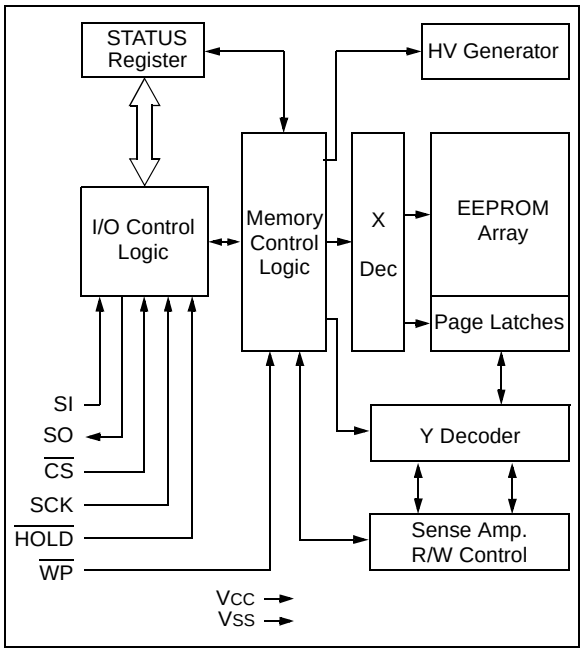


2.0 FUNCTIONAL DESCRIPTION

2.1 Principles of Operation

The 25AA02E48 is a 256-byte Serial EEPROM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in software to match the SPI protocol.

BLOCK DIAGRAM



Note:	This data sheet documents only the device's features and specifications that are in addition to the features and specifications of the 25AA020A device. For information on the features and specifications shared by the 25AA02E48 and 25AA020A devices, see the "*25AA020A Data Sheet*" (DS21833).

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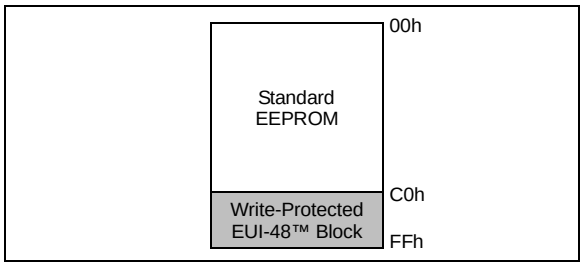
3.0 PRE-PROGRAMMED EUI-48™ NODE ADDRESS

The 25AA02E48 is programmed at the factory with a globally unique, EUI-48™ and EUI-64™ compatible node address stored in the upper 1/4 of the array and write-protected through the STATUS register. The remaining 1,536 bits are available for application use.

FIGURE 3-1: MEMORY ORGANIZATION



The 6-byte EUI-48™ node address value is stored in array locations 0xFA through 0xFF, as shown in Figure 3-2. The first 3 bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE Registration Authority. The remaining 3 bytes are the Extension Identifier, and are generated by Microchip to ensure a globally-unique, 48-bit value.

3.1 EUI-64™ Support

The pre-programmed EUI-48 node address can easily be encapsulated at the application level to form a globally unique, 64-bit node address for systems utilizing the EUI-64 standard. This is done by adding 0xFFFE between the OUI and the Extension Identifier, as shown below.

FIGURE 3-2: EUI-48 NODE ADDRESS PHYSICAL MEMORY MAP EXAMPLE

Description	24-bit Organizationally Unique Identifier			24-bit Extension Identifier		
Data	00h	04h	A3h	12h	34h	56h
Array Address	FAh					FFh

Corresponding EUI-48™ Node Address: 00-04-A3-12-34-56

Corresponding EUI-64™ Node Address: 00-04-A3-FF-FE-12-34-56

3.2 Factory-Programmed Write Protection

In order to help guard against accidental corruption of the EUI-48 node address, the BP1 and BP0 bits of the STATUS register are programmed at the factory to '0' and '1', respectively, as shown in the following table:

7	6	5	4	3	2	1	0
X	X	X	X	BP1	BP0	WEL	WIP
—	—	—	—	0	1	—	—

This protects the upper 1/4 of the array (0xC0 to 0xFF) from write operations. This array block can be utilized for writing by clearing the BP bits with a Write Status Register (WRSR) instruction. Note that if this is performed, care must be taken to prevent overwriting the EUI-48 value.

4.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 4-1.

TABLE 4-1: PIN FUNCTION TABLE

Name	SOIC	SOT-23	Function
$\overline{CS}$	1	5	Chip Select Input
SO	2	4	Serial Data Output
$\overline{WP}$	3	—	Write-Protect Pin
VSS	4	2	Ground
SI	5	3	Serial Data Input
SCK	6	1	Serial Clock Input
$\overline{HOLD}$	7	—	Hold Input
VCC	8	6	Supply Voltage

4.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

4.2 Serial Output (SO)

The SO pin is used to transfer data out of the 25AA02E48. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

4.3 Write-Protect ($\overline{WP}$)

The $\overline{WP}$ pin is a hardware write-protect input pin. When it is low, all writes to the array or STATUS register are disabled, but any other operations function normally. When $\overline{WP}$ is high, all functions, including nonvolatile writes operate normally. At any time, when $\overline{WP}$ is low, the write enable Reset latch will be reset and programming will be inhibited. However, if a write cycle is already in progress, $\overline{WP}$ going low will not change or disable the write cycle. See Table 2-4 for the Write-Protect Functionality Matrix.

4.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

4.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25AA02E48. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

4.6 Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used to suspend transmission to the 25AA02E48 while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{HOLD}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{HOLD}$ pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high-to-low transition. The 25AA02E48 must remain selected during this sequence. The SI, SCK and SO pins are in a high-impedance state during the time the device is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{HOLD}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the HOLD line at any time will tri-state the SO line.

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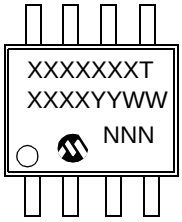
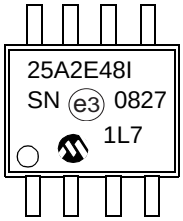
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

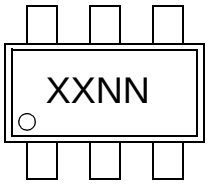
8-Lead SOIC



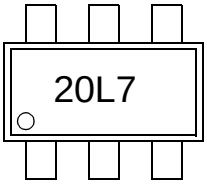
Example:



6-Lead SOT-23



Example:



Part Number	1st Line Marking Code
	SOT-23
	I Temp.
25AA02E48	20NN

Note: NN = Alphanumeric traceability code

Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

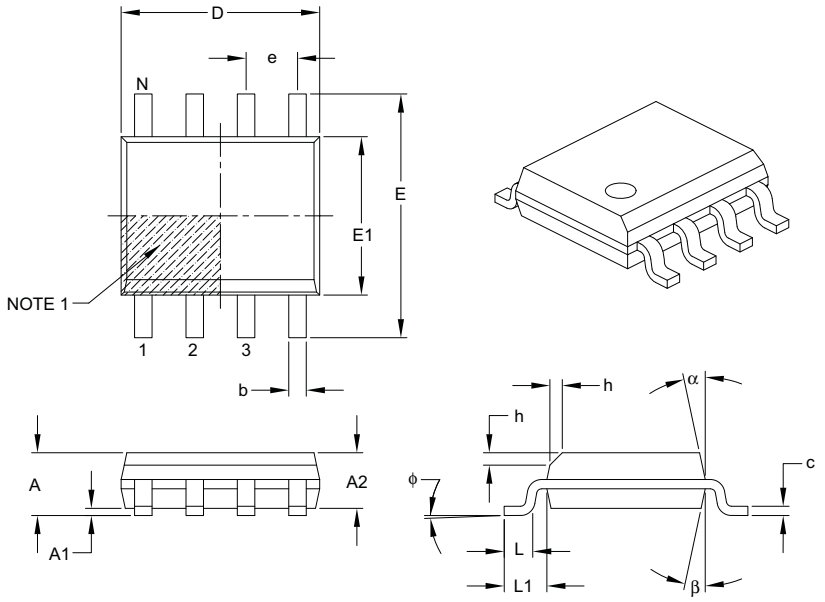
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Note: Please visit www.microchip.com/Pbfree for the latest information on Pb-free conversion.

*****Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

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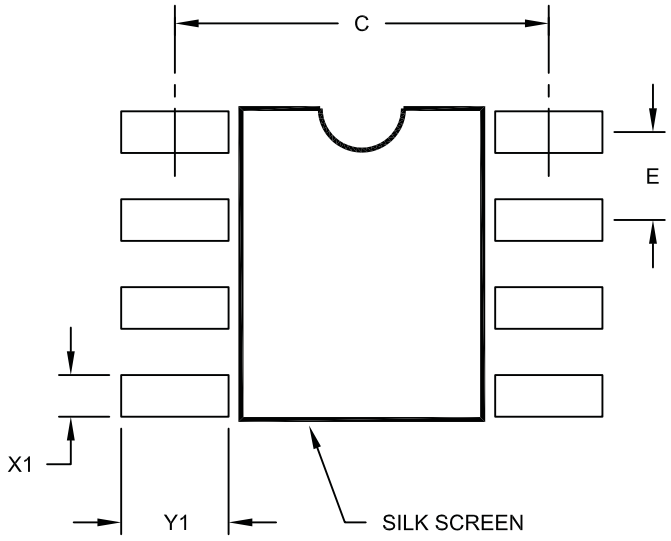
8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

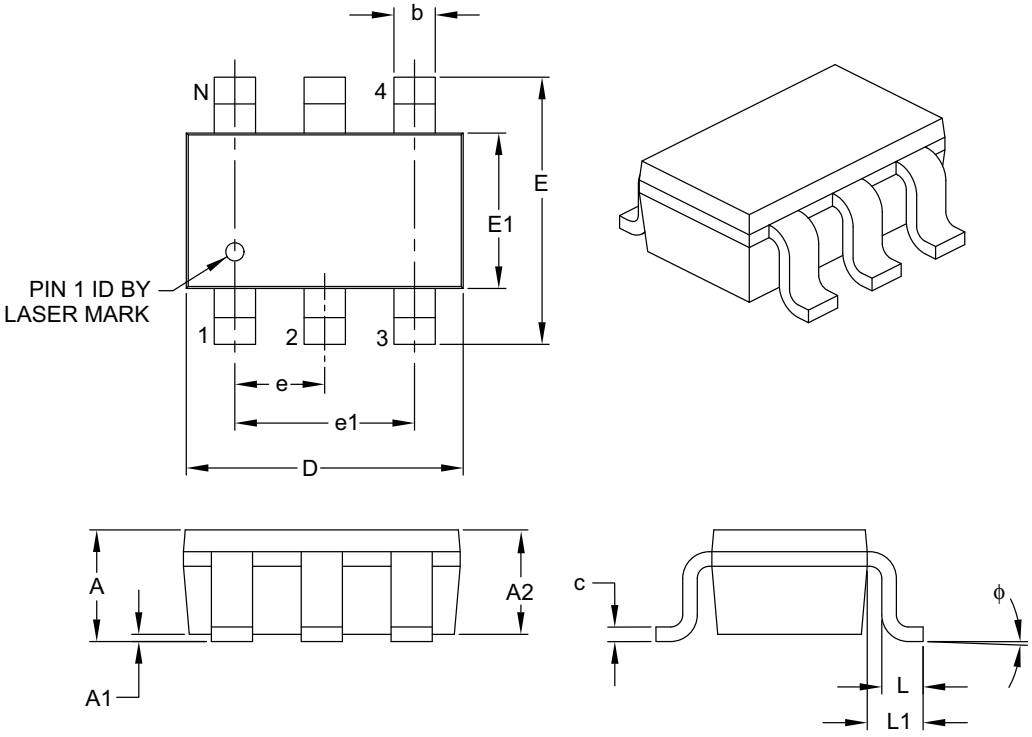
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

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APPENDIX A: REVISION HISTORY

Revision A (12/08)

Original release of this document.

NOTES:

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- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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Device: 25AA02E48 Literature Number: DS22123A

Questions:

1. What are the best features of this document?

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To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	–	X	/XX
Device	Tape & Reel		Temperature	Package

Device:	25AA02E48		2k-Bit, 1.8V, 16 Byte Page, SPI Serial EEPROM with EUI-48™ Node Identity
Tape & Reel:	Blank	=	Standard packaging
	T	=	Tape & Reel
Temperature Range:	I	=	-40°C to+85°C
Package:	SN	=	Plastic SOIC (3.90 mm body), 8-lead
	OT	=	SOT-23, 6-lead (Tape and Reel only)

Examples:

a) 25AA02E48-I/SN = 2k-bit, 16-byte page, 1.8V Serial EEPROM, Industrial temp., SOIC package

b) 25AA02E48T-I/SN = 2k-bit, 16-byte page, 1.8V Serial EEPROM, Industrial temp., Tape & Reel, SOIC package

c) 25AA02E48T-I/OT = 2k-bit, 16-byte page, 1.8V Serial EEPROM, Industrial temp., Tape & Reel, SOT-23 package

NOTES:

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