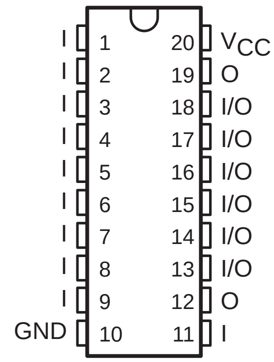
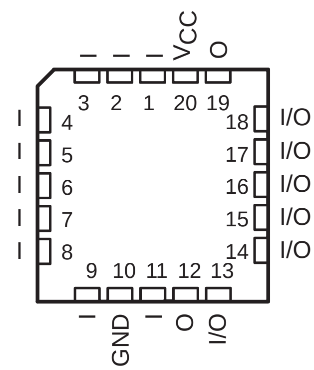
- **High-Performance Operation:**
  f_{max} (w/o feedback)
  TIBPAL16R’-10C Series . . . 62.5 MHz Min
  TIBPAL16R’-12M Series . . . 56 MHz Min
  f_{max} (with feedback)
  TIBPAL16R’-10C Series . . . 55.5 MHz Min
  TIBPAL16R’-12M Series . . . 48 MHz Min
  Propagation Delay
  TIBPAL16L’-10C Series . . . 10 ns Max
  TIBPAL16L’-12M Series . . . 12 ns Max
- **Functionally Equivalent, but Faster than, Existing 20-Pin PLDs**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Security Fuse Prevents Duplication**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state buffers)	4
PAL16R6	8	0	6 (3-state buffers)	2
PAL16R8	8	0	8 (3-state buffers)	0

TIBPAL16L8’
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE
(TOP VIEW)



TIBPAL16L8’
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for futher reduction in board space.

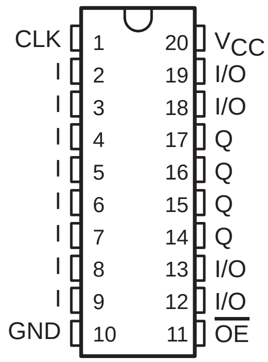
All of the register outputs are set to a low level during power up. Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL16’ C series is characterized from 0°C to 75°C. The TIBPAL16’ M series is characterized for operation over the full military temperature range of –55°C to 125°C.

These devices are covered by U.S. Patent 4,410,987.
IMPACT-X is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Advanced Micro Devices Inc.

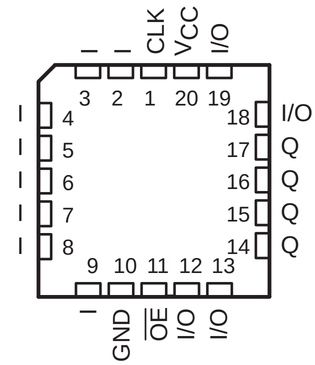
TIBPAL16R4’
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE

(TOP VIEW)



TIBPAL16R4’
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

(TOP VIEW)



TIBPAL16R6’
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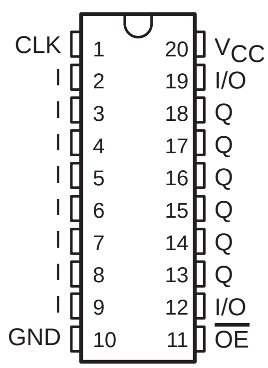
M SUFFIX . . . J PACKAGE

(TOP VIEW)



TIBPAL16R6’
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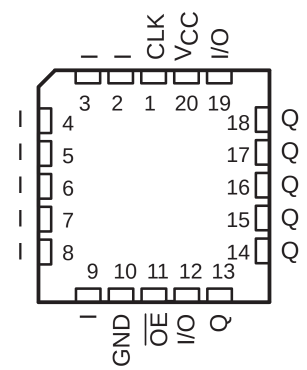
M SUFFIX . . . FK PACKAGE

(TOP VIEW)



TIBPAL16R8’
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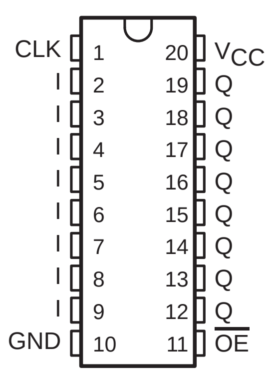
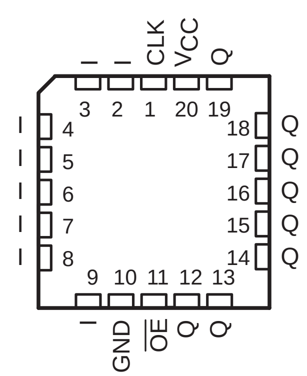
M SUFFIX . . . J PACKAGE

(TOP VIEW)



TIBPAL16R8’
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

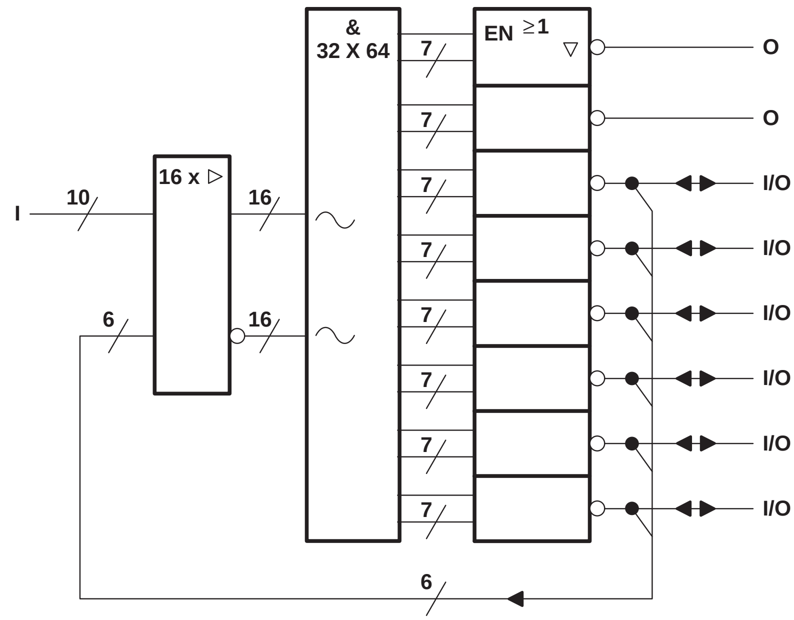
(TOP VIEW)



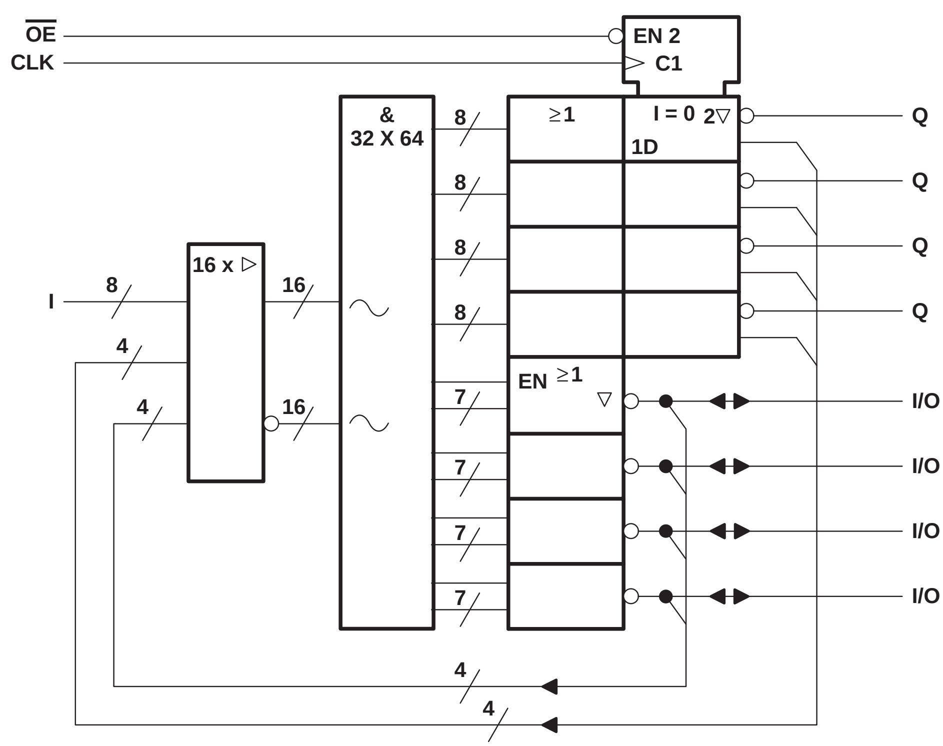
Pin assignments in operating mode

functional block diagrams (positive logic)

TIBPAL16L8’



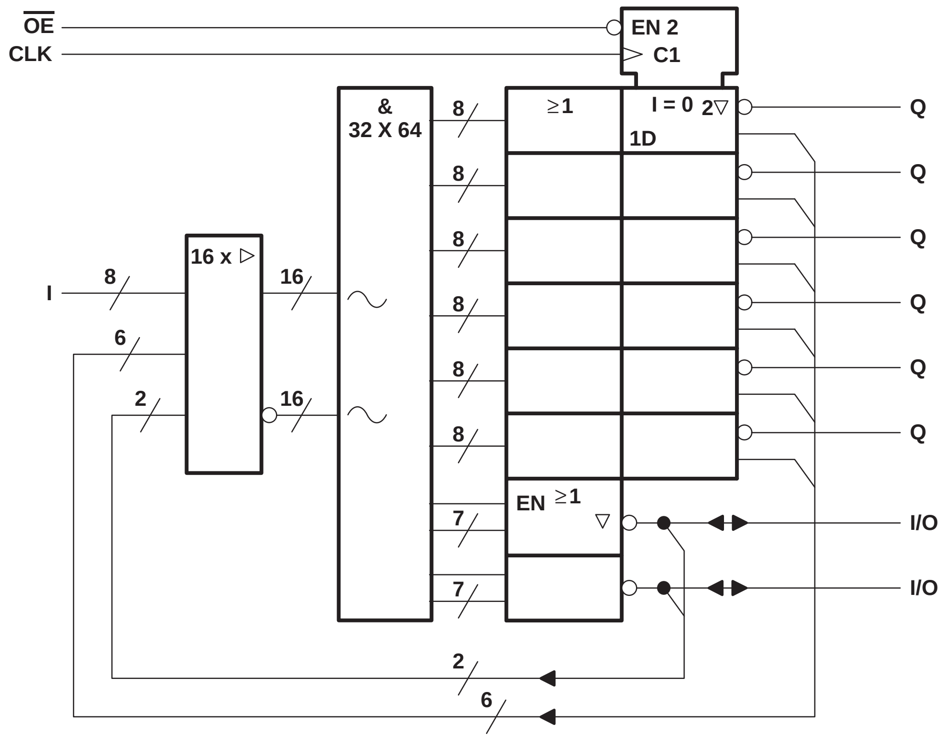
TIBPAL16R4’



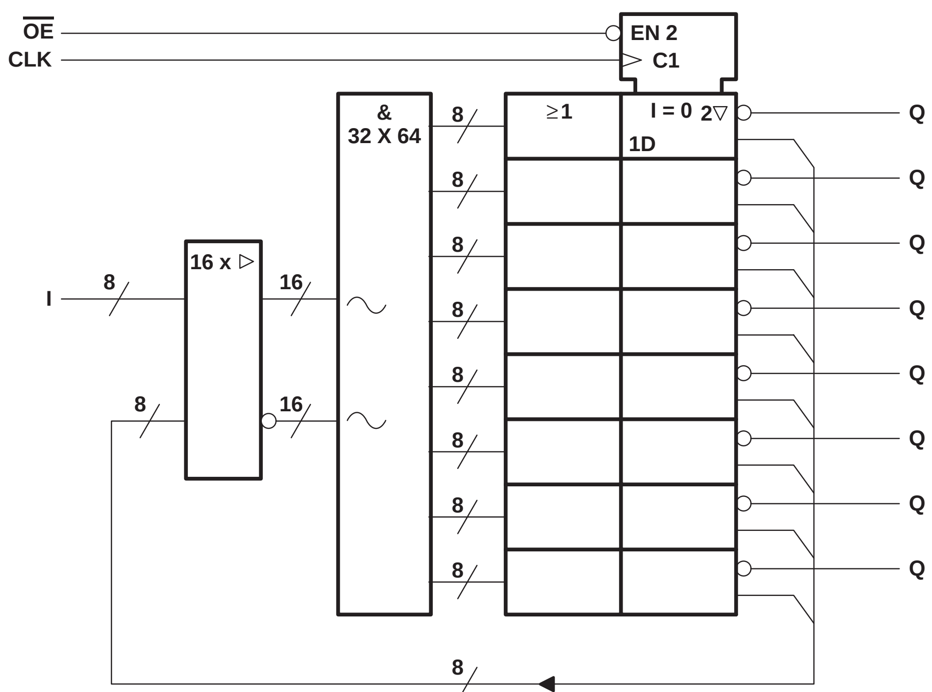
∿ denotes fused inputs

functional block diagrams (positive logic)

TIBPAL16R6’

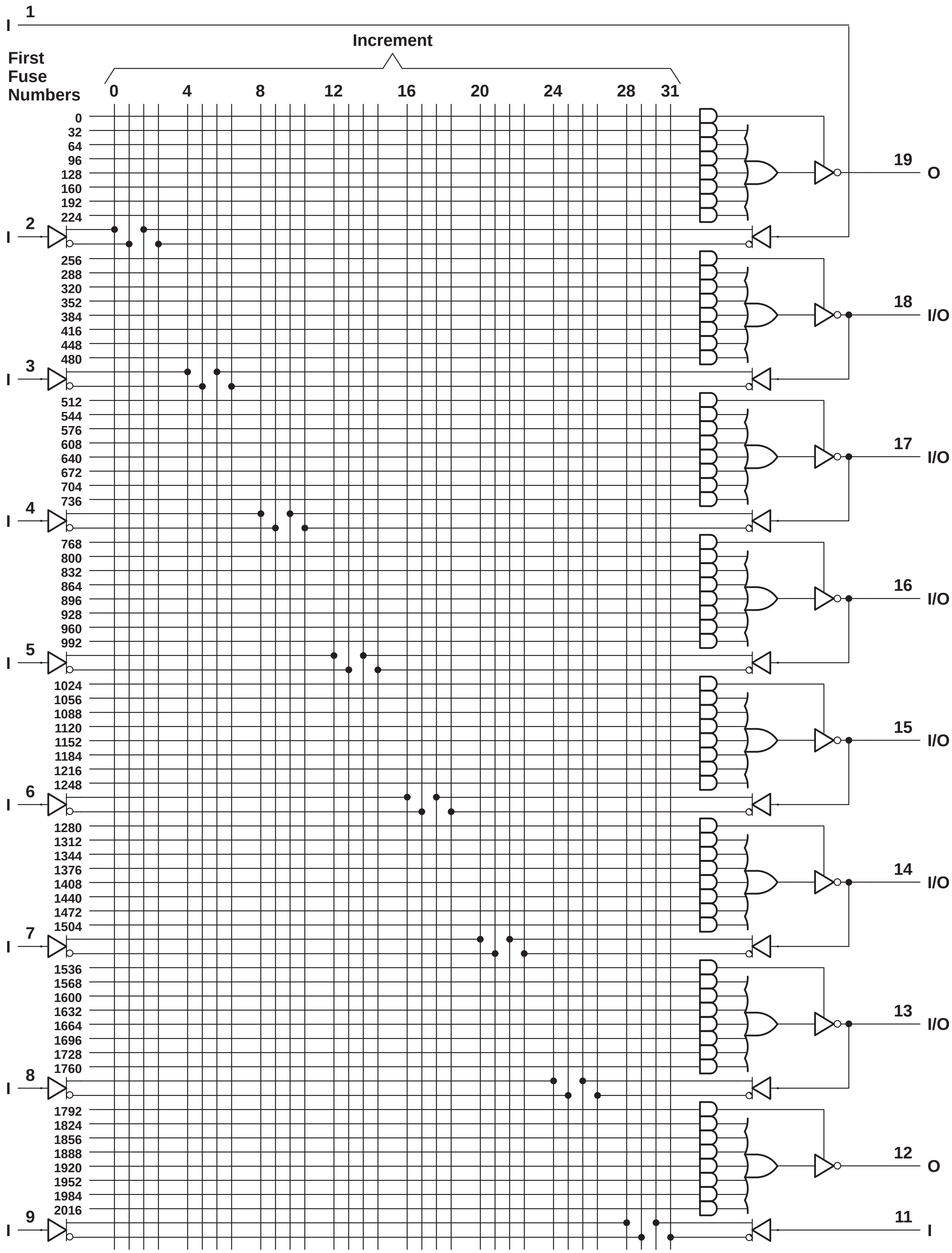


TIBPAL16R8’



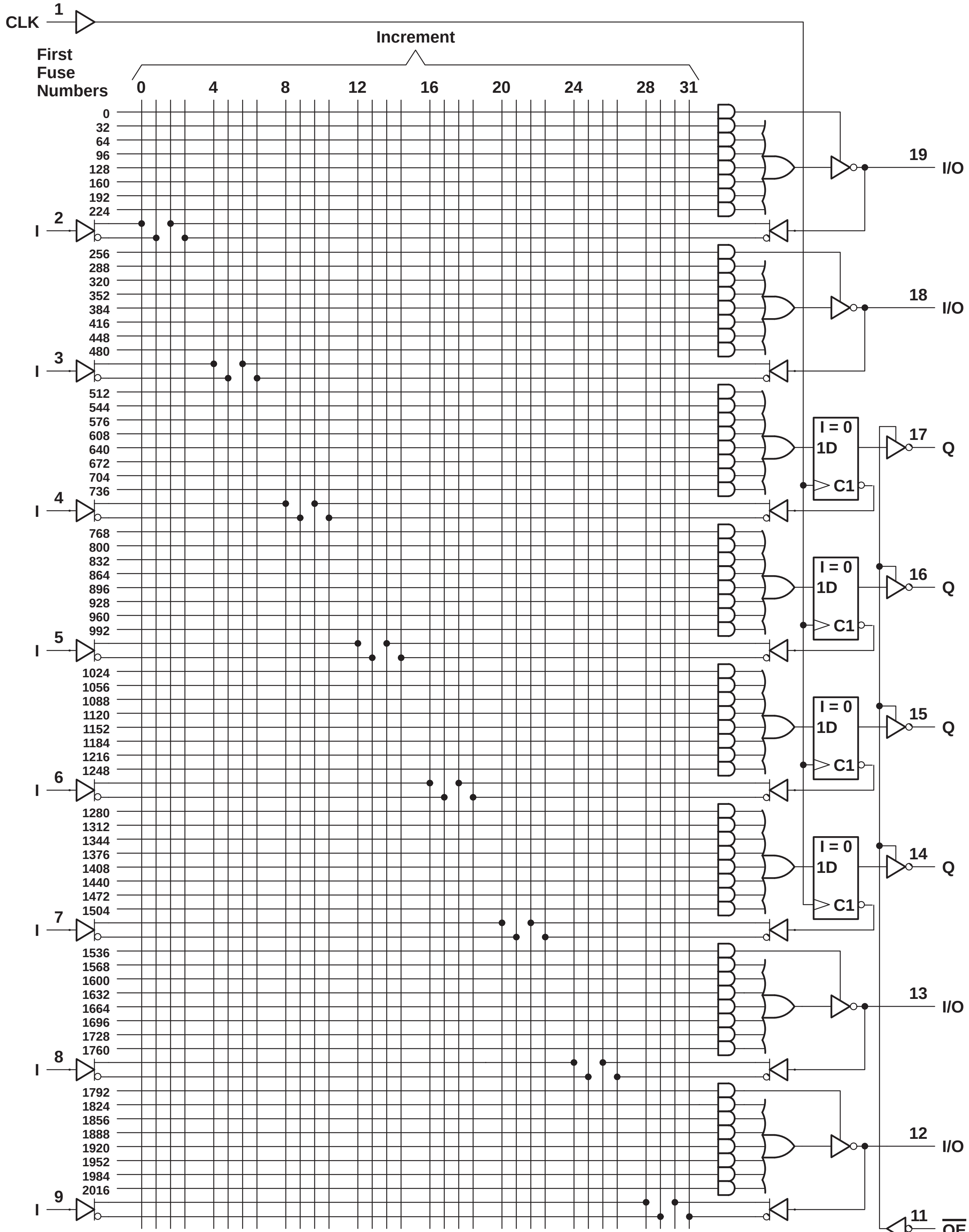
∼ denotes fused inputs

logic diagram (positive logic)



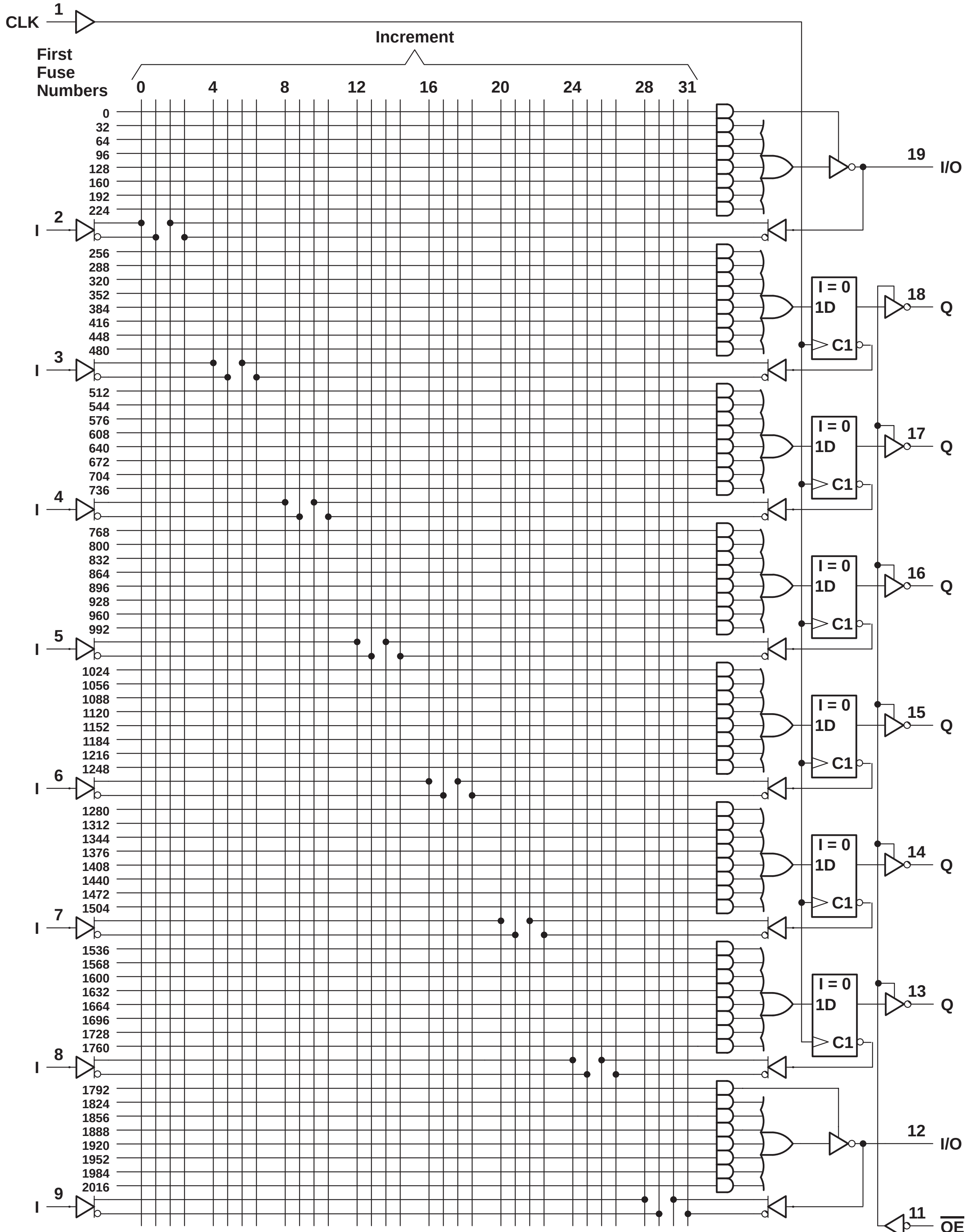
Fuse number = First fuse number + Increment

logic diagram (positive logic)



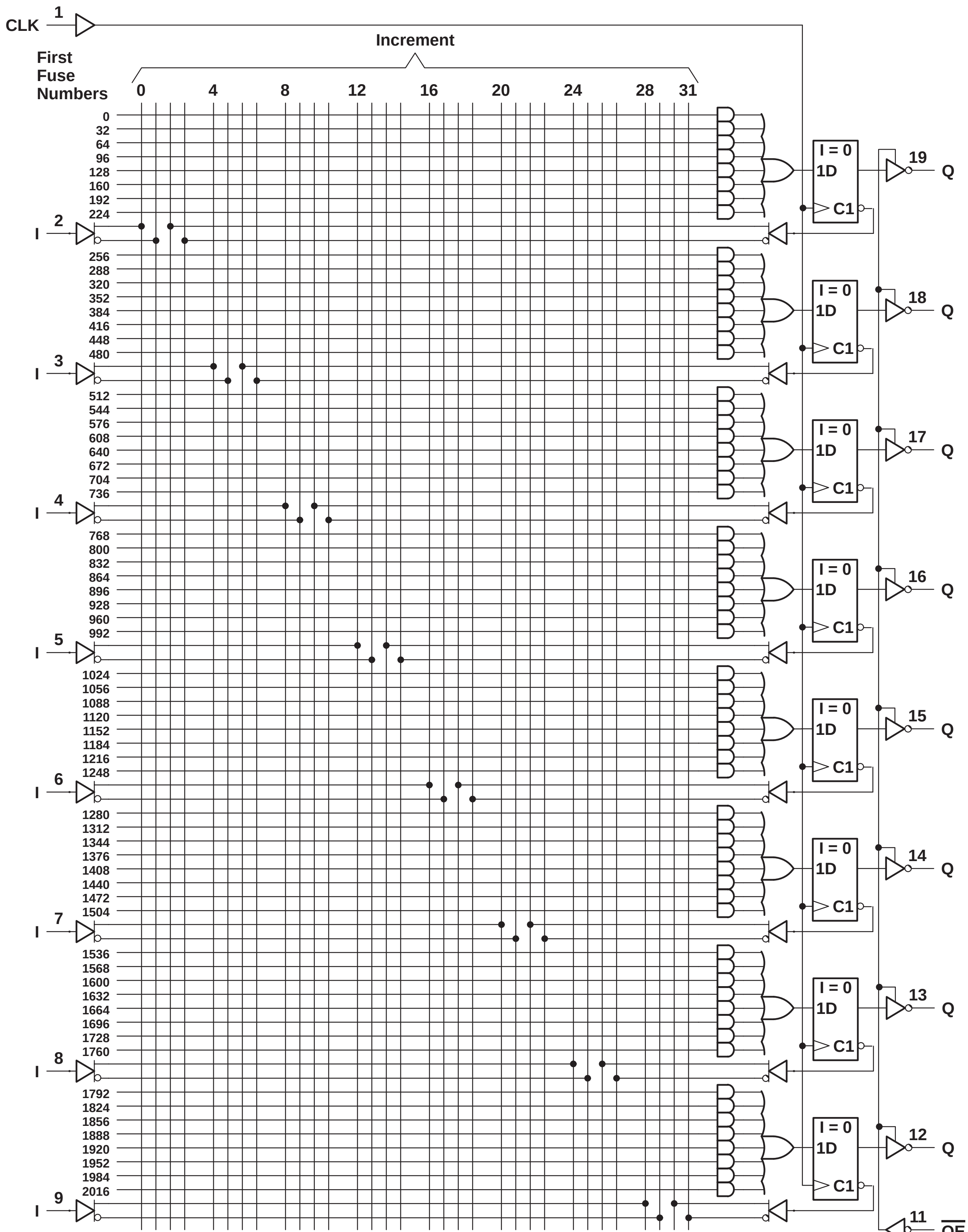
Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage (see Note 1) . . . . 5.5 V
Voltage applied to disabled output (see Note 1) . . . . 5.5 V
Operating free-air temperature range . . . . 0°C to 75°C
Storage temperature range . . . . –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				–3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		62.5	MHz
t_w	Pulse duration, clock (see Note 2)	High	8			ns
		Low	8			
t_{su}	Setup time, input or feedback before clock↑		10			ns
t_h	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA			–0.8	–1.5	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = –3.2 mA		2.4	3.2		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA			0.3	0.5	V
I_{OZH}‡	V_{CC} = 5.25 V,	V_O = 2.4 V				100	µA
I_{OZL}‡	V_{CC} = 5.25 V,	V_O = 0.4 V				–100	µA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V				0.2	mA
I_{IH}‡	V_{CC} = 5.25 V,	V_I = 2.4 V				25	µA
I_{IL}‡	V_{CC} = 5.25 V,	V_I = 0.4 V			–0.08	–0.25	mA
I_{OS}§	V_{CC} = 5.25 V,	V_O = 0		–30	–70	–130	mA
I_{CC}	V_{CC} = 5.25 V,	V_I = 0,	Outputs open		140	180	mA
C_i	f = 1 MHz,	V_I = 2 V			5		pF
C_o	f = 1 MHz,	V_O = 2 V			6		pF
$C_{i/o}$	f = 1 MHz,	$V_{I/O}$ = 2 V			7.5		pF
C_{clk}	f = 1 MHz,	V_{CLK} = 2 V			6		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH} respectively.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}‡	With feedback		R1 = 200 Ω, R2 = 390 Ω, See Figure 3	55.5	80		MHz
	Without feedback			62.5	85		
t_{pd}	I, I/O	O, I/O		3	7	10	ns
t_{pd}	CLK↑	Q		2	5	8	ns
t_{en}	OE↓	Q		1	4	10	ns
t_{dis}	OE↑	Q		1	4	10	ns
t_{en}	I, I/O	O, I/O		3	8	10	ns
t_{dis}	I, I/O	O, I/O		3	8	10	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ $f_{max}(\text{with feedback}) = \frac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, $f_{max}(\text{without feedback}) = \frac{1}{t_w\ \text{high} + t_w\ \text{low}}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage (see Note 1) . . . . 5.5 V
Voltage applied to disabled output (see Note 1) . . . . 5.5 V
Operating free-air temperature range . . . . –55°C to 125°C
Storage temperature range . . . . –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}†	Clock frequency		0		56	MHz
t_w	Pulse duration, clock (see Note 2)	High	9			ns
		Low	9			
t_{su}†	Setup time, input or feedback before clock↑		11			ns
t_h†	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		–55	25	125	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–0.8	–1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –2 mA		2.4	3.2		V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.3	0.5	V
I_{OZH}‡	V_{CC} = 5.5 V,	V_O = 2.4 V				100	µA
I_{OZL}‡	V_{CC} = 5.5 V,	V_O = 0.4 V				–100	µA
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V				0.2	mA
I_{IH}‡	V_{CC} = 5.5 V,	V_I = 2.4 V				25	µA
I_{IL}‡	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.08	–0.25	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0.5 V		–30	–70	–250	mA
I_{CC}	V_{CC} = 5.5 V,	V_I = GND,	Outputs open		140	220	mA
C_i	f = 1 MHz,	V_I = 2 V			5		pF
C_o	f = 1 MHz,	V_O = 2 V			6		pF
$C_{i/o}$	f = 1 MHz,	$V_{I/O}$ = 2 V			7.5		pF
C_{clk}	f = 1 MHz,	V_{CLK} = 2 V			6		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH} respectively.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}	With feedback		R1 = 390 Ω, R2 = 750 Ω, See Figure 3	48	80		MHz
	Without feedback			56	85		
t_{pd}	I, I/O	O, I/O		3	7	12	ns
t_{pd}	CLK↑	Q		2	5	10	ns
t_{en}	OE↓	Q		1	4	10	ns
t_{dis}	OE↑	Q		1	4	10	ns
t_{en}	I, I/O	O, I/O		3	8	14	ns
t_{dis}	I, I/O	O, I/O		2	8	12	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ $f_{max}(\text{with feedback}) = \frac{1}{t_{su} + t_{pd}\,(\text{CLK to Q})}$, $f_{max}(\text{without feedback}) = \frac{1}{t_w\,\text{high} + t_w\,\text{low}}$

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Figure 1 and Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 11 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 11 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

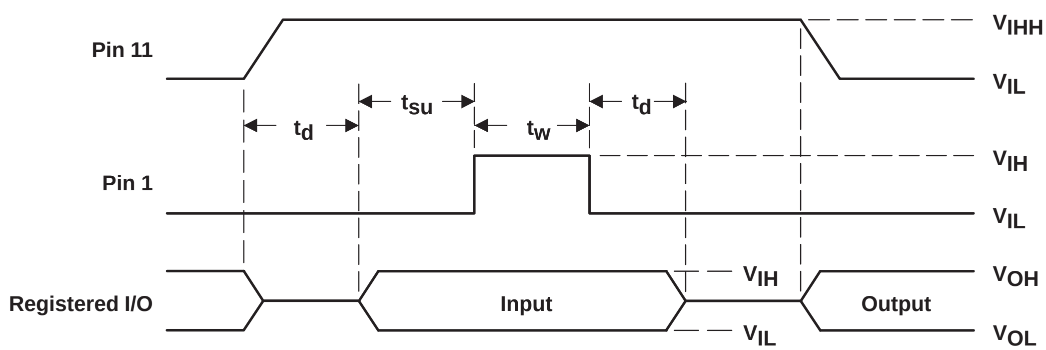
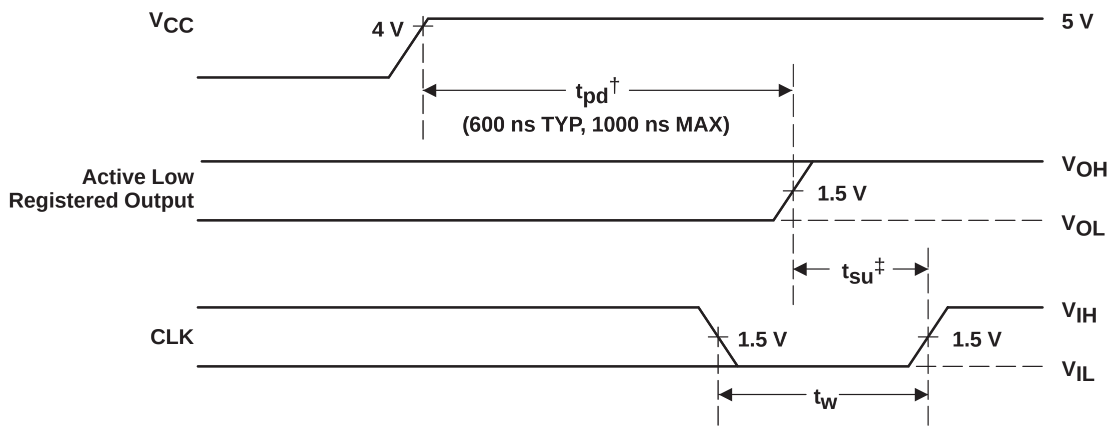


Figure 1. Preload Waveforms

NOTE 3: $t_d = t_{su} = t_h$ = 100 ns to 1000 ns V_{IHH} = 10.25 V to 10.75 v

power-up reset (see Figure 2)

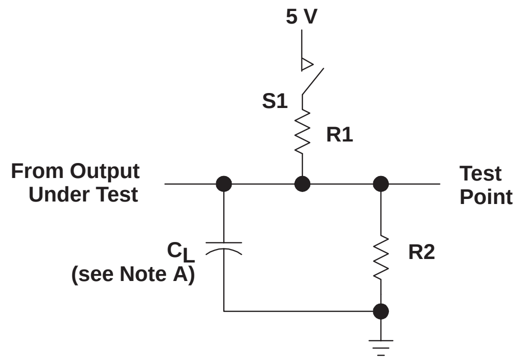
Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



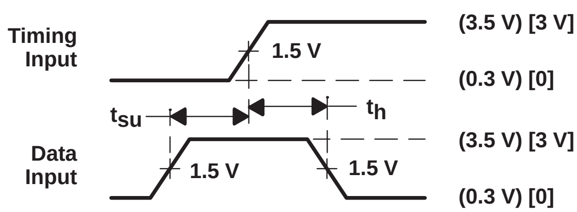
† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

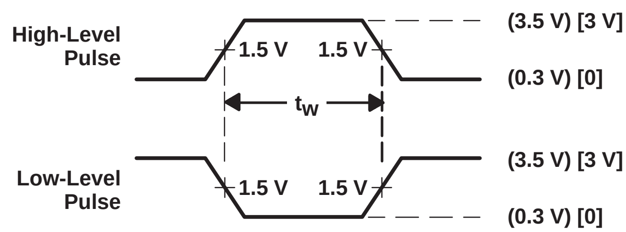
PARAMETER MEASUREMENT INFORMATION



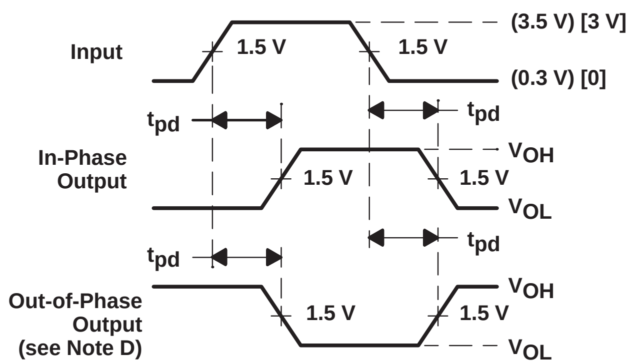
LOAD CIRCUIT FOR 3-STATE OUTPUTS



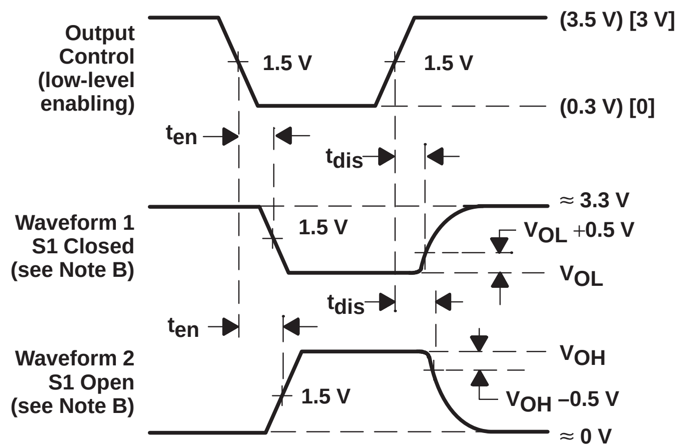
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses have the following characteristics: For C suffix, use the voltage levels indicated in parentheses ( ), PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%; For M suffix, use the voltage levels indicated in brackets [ ], PRR ≤ 10 MHz, t_r and $t_f \leq 2$ ns, duty cycle = 50%

D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

E. Equivalent loads may be used for testing.

Figure 3. Load Circuit and Voltage Waveforms

metastable characteristics of TIBPAL16R4-10C, TIBPAL16R6-10C, and TIBPAL16R8-10C

At some point a system designer is faced with the problem of synchronizing two digital signals operating at two different frequencies. This problem is typically overcome by synchronizing one of the signals to the local clock through use of a flip-flop. However, this solution presents an awkward dilemma since the setup and hold time specifications associated with the flip-flop are sure to be violated. The metastable characteristics of the flip-flop can influence overall system reliability.

Whenever the setup and hold times of a flip-flop are violated, its output response becomes uncertain and is said to be in the metastable state if the output hangs up in the region between V_{IL} and V_{IH}. This metastable condition lasts until the flip-flop falls into one of its two stable states, which takes longer than the specified maximum propagation delay time (CLK to Q max).

From a system engineering standpoint, a designer cannot use the specified data sheet maximum for propagation delay time when using the flip-flop as a data synchronizer – how long to wait after the specified data sheet maximum must be known before using the data in order to guarantee reliable system operation.

The circuit shown in Figure 4 can be used to evaluate MTBF (Mean Time Between Failure) and Δt for a selected flip-flop. Whenever the Q output of the DUT is between 0.8 V and 2 V, the comparators are in opposite states. When the Q output of the DUT is higher than 2 V or lower than 0.8 V, the comparators are at the same logic level. The outputs of the two comparators are sampled a selected time (Δt) after SCLK. The exclusive OR gate detects the occurrence of a failure and increments the failure counter.

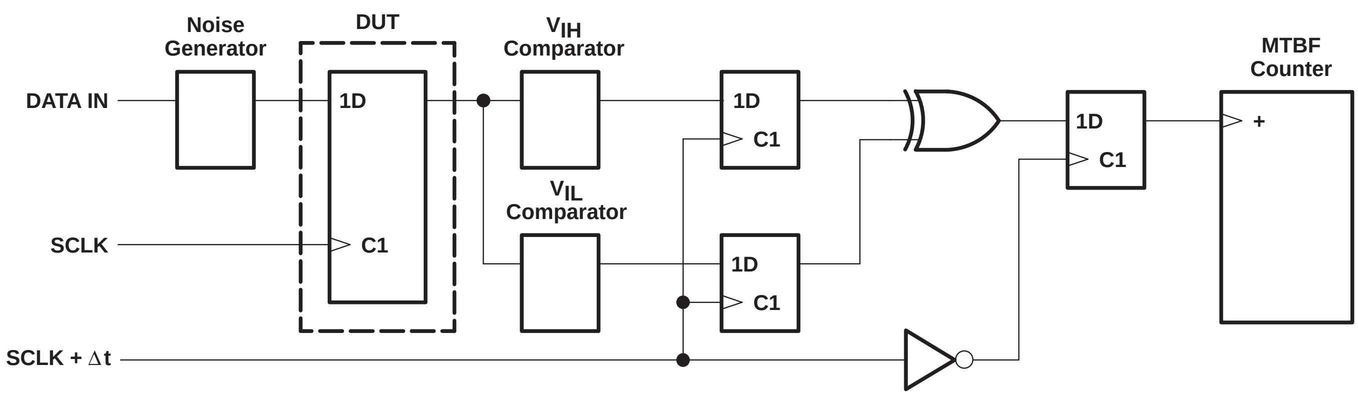
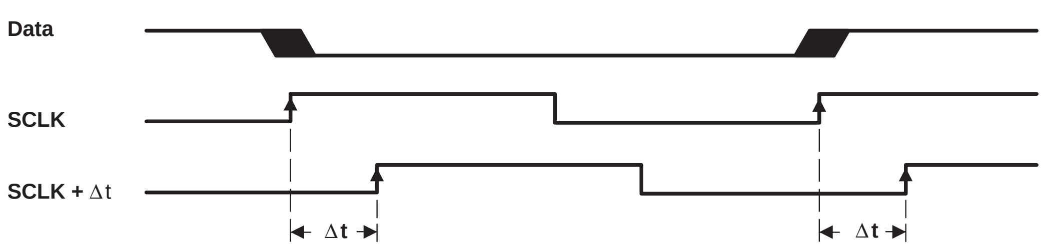


Figure 4. Metastable Evaluation Test Circuit

In order to maximize the possibility of forcing the DUT into a metastable state, the input data signal is applied so that it always violates the setup and hold time. This condition is illustrated in the timing diagram in Figure 5. Any other relationship of SCLK to data will provide less chance for the device to enter into the metastable state.



$$\text{MTBF} = \frac{\text{Time (sec)}}{\text{\# Failures}}$$

$$t_{rec} = \Delta t - \text{CLK to Q (max)}$$

Figure 5. Timing Diagram

By using the described test circuit, MTBF can be determined for several different values of Δt (see Figure 4). Plotting this information on semilog scale demonstrates the metastable characteristics of the selected flip-flop. Figure 6 shows the results for the TIBPAL16’-10C operating at 1 MHz.

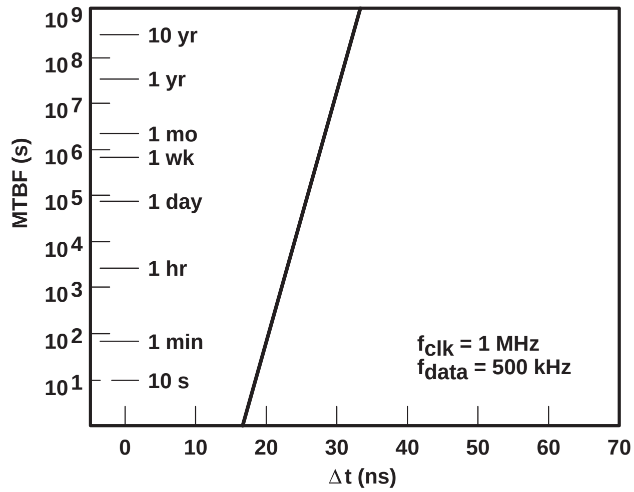


Figure 6. Metastable Characteristics

From the data taken in the above experiment, an equation can be derived for the metastable characteristics at other clock frequencies.

The metastable equation: $\frac{1}{MTBF} = f_{SCLK} \times f_{data} \times C1 \; e^{(-C2 \times \Delta t)}$

The constants C1 and C2 describe the metastable characteristics of the device. From the experimental data, these constants can be solved for: C1 = 9.15 X 10^{-7} and C2 = 0.959

Therefore

$$\frac{1}{MTBF} = f_{SCLK} \times f_{data} \times 9.15 \times 10^{-7} \; e^{(-0.959 \times \Delta t)}$$

definition of variables

DUT (Device Under Test): The DUT is a 10-ns registered PLD programmed with the equation Q : = D.

MTBF (Mean Time Between Failures): The average time (s) between metastable occurrences that cause a violation of the device specifications.

f_{SCLK} (system clock frequency): Actual clock frequency for the DUT.

f_{data} (data frequency): Actual data frequency for a specified input to the DUT.

C1: Calculated constant that defines the magnitude of the curve.

C2: Calculated constant that defines the slope of the curve.

t_{rec} (metastability recovery time): Minimum time required to guarantee recovery from metastability, at a given MTBF failure rate. $t_{rec} = \Delta t - t_{pd}$ (CLK to Q, max)

Δt: The time difference (ns) from when the synchronizing flip-flop is clocked to when its output is sampled.

The test described above has shown the metastable characteristics of the TIBPAL16R4/R6/R8-10C series. For additional information on metastable characteristics of Texas Instruments logic circuits, please refer to TI Applications publication SDAA004, ”Metastable Characteristics, Design Considerations for ALS, AS, and LS Circuits.’’

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

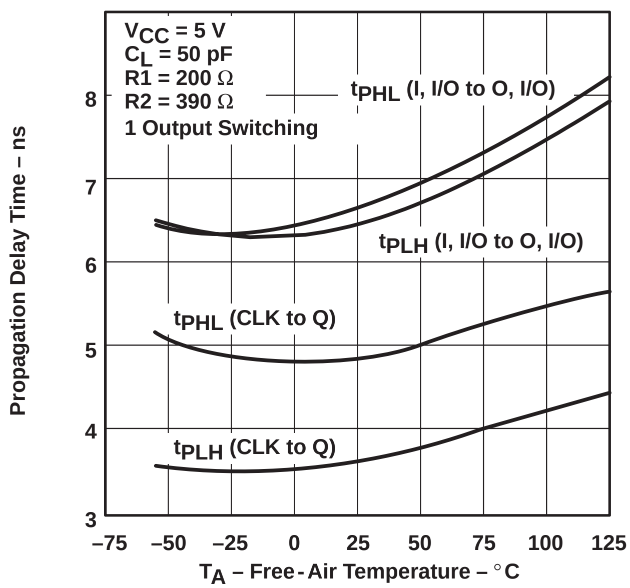


Figure 7

PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

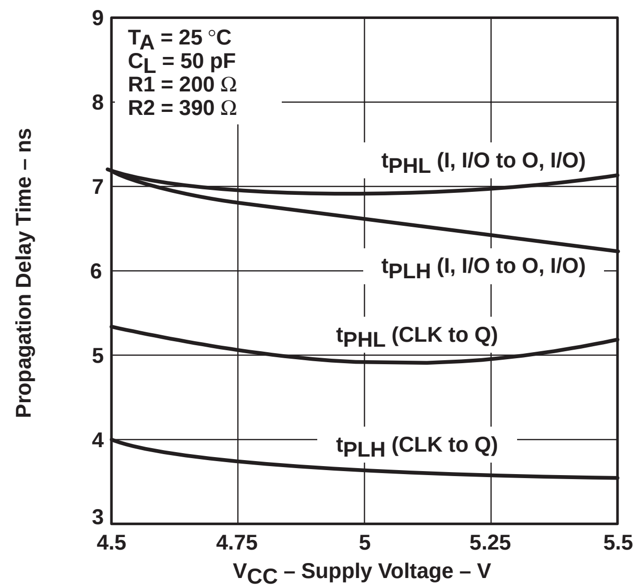


Figure 8

PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING

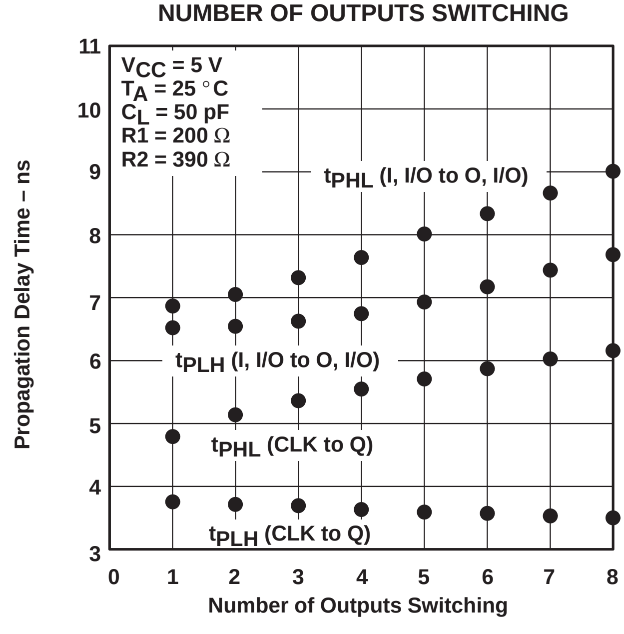


Figure 9

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

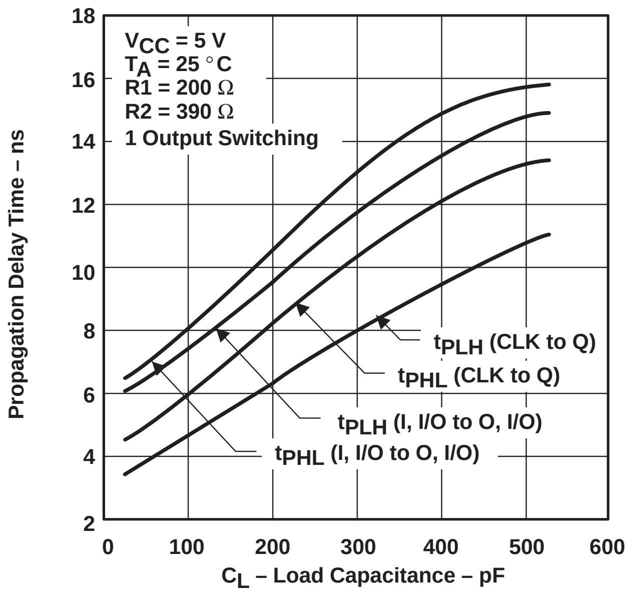


Figure 10

POWER DISSIPATION vs FREQUENCY 8-BIT COUNTER MODE

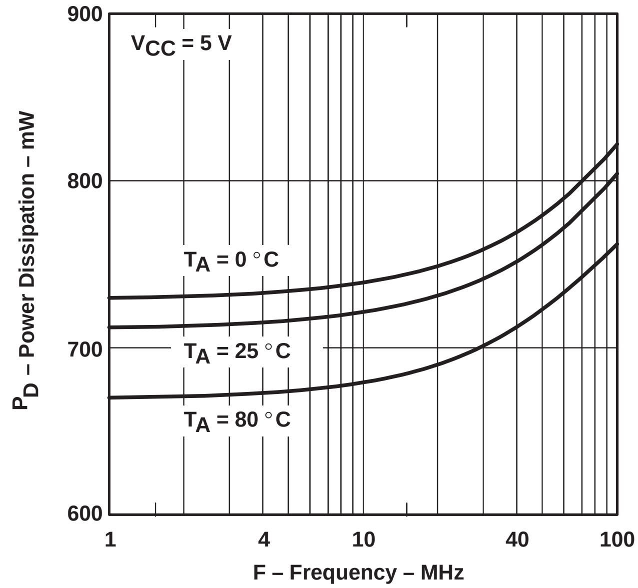


Figure 11

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

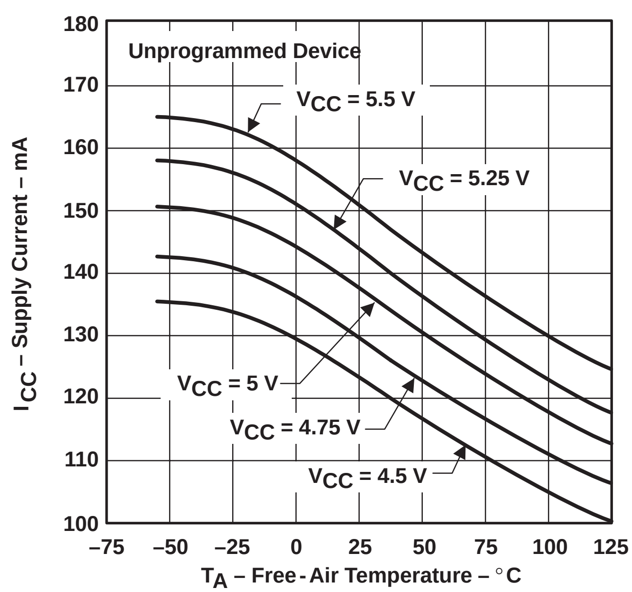


Figure 12

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TEXAS INSTRUMENTS

D0892

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-85155132A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-8515513RA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
5962-8515513SA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
5962-85155142A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-8515514RA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
5962-8515514SA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
5962-85155152A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-8515515RA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
5962-8515515SA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
5962-85155162A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-8515516RA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
5962-8515516SA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16L8-10CFN	ACTIVE	PLCC	FN	20	46	None	Call TI	Level-1-220-UNLIM
TIBPAL16L8-10CN	ACTIVE	PDIP	N	20	20	None	Call TI	Level-NC-NC-NC
TIBPAL16L8-12MFKB	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16L8-12MJ	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16L8-12MJB	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16L8-12MWB	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16R4-10CFN	ACTIVE	PLCC	FN	20	46	None	Call TI	Level-1-220-UNLIM
TIBPAL16R4-10CN	ACTIVE	PDIP	N	20	20	None	Call TI	Level-NC-NC-NC
TIBPAL16R4-12MFKB	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16R4-12MJ	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16R4-12MJB	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16R4-12MWB	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16R6-10CFN	ACTIVE	PLCC	FN	20	46	None	Call TI	Level-1-220-UNLIM
TIBPAL16R6-10CN	ACTIVE	PDIP	N	20	20	None	Call TI	Level-NC-NC-NC
TIBPAL16R6-12MFKB	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16R6-12MJ	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16R6-12MJB	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16R6-12MWB	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16R8-10CFN	OBSOLETE	PLCC	FN	20		None	Call TI	Call TI
TIBPAL16R8-10CN	OBSOLETE	PDIP	N	20		None	Call TI	Call TI
TIBPAL16R8-12MFKB	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16R8-12MJB	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16R8-12MWB	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC

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