

Power MOSFET

PRODUCT SUMMARY

| | | |
|---------------------------|------------------|------|
| V_{DS} (V) | - 60 | |
| $R_{DS(on)}$ (Ω) | $V_{GS} = -10$ V | 0.50 |
| Q_g (Max.) (nC) | 12 | |
| Q_{gs} (nC) | 3.8 | |
| Q_{gd} (nC) | 5.1 | |
| Configuration | Single | |

FEATURES

- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- P-Channel
- Fast Switching
- Ease of Paralleling
- Lead (Pb)-free Available



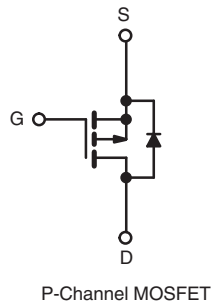
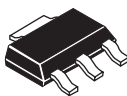
Available
RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mounting using vapor phase, infrared, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25 W is possible in a typical surface mount application.

SOT-223



ORDERING INFORMATION

| | | |
|----------------|--------------|----------------------------|
| Package | SOT-223 | SOT-223 |
| Lead (Pb)-free | IRFL9014PbF | IRFL9014TRPbF ^a |
| | SiHFL9014-E3 | SiHFL9014T-E3 ^a |
| SnPb | IRFL9014 | IRFL9014TR ^a |
| | SiHFL9014 | SiHFL9014T ^a |

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$, unless otherwise noted

| PARAMETER | SYMBOL | LIMIT | UNIT | |
|---|--------------------|---------------------------|-------|---------------------|
| Drain-Source Voltage | V_{DS} | - 60 | V | |
| Gate-Source Voltage | V_{GS} | ± 20 | | |
| Continuous Drain Current | V_{GS} at - 10 V | $T_C = 25^\circ\text{C}$ | - 1.8 | A |
| | | $T_C = 100^\circ\text{C}$ | - 1.1 | |
| Pulsed Drain Current ^a | | I_{DM} | - 14 | |
| Linear Derating Factor | | | 0.025 | W/ $^\circ\text{C}$ |
| Linear Derating Factor (PCB Mount) ^e | | | 0.017 | |
| Single Pulse Avalanche Energy ^b | E_{AS} | 140 | mJ | |
| Repetitive Avalanche Current ^a | I_{AR} | - 1.8 | A | |
| Repetitive Avalanche Energy ^a | E_{AR} | 0.31 | mJ | |

* Pb containing terminations are not RoHS compliant, exemptions may apply

| ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted | | | | |
|---|----------------------------------|----------------|------------------|------------------|
| PARAMETER | | SYMBOL | LIMIT | UNIT |
| Maximum Power Dissipation | $T_C = 25\text{ }^\circ\text{C}$ | P_D | 3.1 | W |
| Maximum Power Dissipation (PCB Mount) ^e | $T_A = 25\text{ }^\circ\text{C}$ | | 2.0 | |
| Peak Diode Recovery dV/dt^c | | dV/dt | - 4.5 | V/ns |
| Operating Junction and Storage Temperature Range | | T_J, T_{stg} | - 55 to + 150 | $^\circ\text{C}$ |
| Soldering Recommendations (Peak Temperature) | for 10 s | | 300 ^d | |

Notes

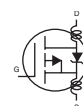
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. $V_{DD} = -25\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 50\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = -1.8\text{ A}$ (see fig. 12).
- c. $I_{SD} \leq -6.7\text{ A}$, $dI/dt \leq 90\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- d. 1.6 mm from case.
- e. When mounted on 1" square PCB (FR-4 or G-10 material).


| THERMAL RESISTANCE RATINGS | | | | |
|--|------------|------|------|---------------------------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient (PCB Mount) ^a | R_{thJA} | - | 60 | $^\circ\text{C}/\text{W}$ |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 40 | |

Note

- a. When mounted on 1" square PCB (FR-4 or G-10 material).

| SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted | | | | | | |
|---|---------------------|--|-------|---------|-----------|---------------------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$ | - 60 | - | - | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$ | - | - 0.059 | - | $\text{V}/^\circ\text{C}$ |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | - 2.0 | - | - 4.0 | V |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 20\text{ V}$ | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = -60\text{ V}$, $V_{GS} = 0\text{ V}$ | - | - | - 100 | μA |
| | | $V_{DS} = -48\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$ | - | - | - 500 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = -10\text{ V}$, $I_D = 1.1\text{ A}^b$ | - | - | 0.50 | Ω |
| Forward Transconductance | g_{fs} | $V_{DS} = -25\text{ V}$, $I_D = 1.1\text{ A}^b$ | 1.3 | - | - | S |
| Dynamic | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5 | - | 270 | - | pF |
| Output Capacitance | C_{oss} | | - | 170 | - | |
| Reverse Transfer Capacitance | C_{riss} | | - | 31 | - | |
| Total Gate Charge | Q_g | $V_{GS} = -10\text{ V}$, $I_D = -6.7\text{ A}$, $V_{DS} = -48\text{ V}$, see fig. 6 and 13 ^b | - | - | 12 | nC |
| Gate-Source Charge | Q_{gs} | | - | - | 3.8 | |
| Gate-Drain Charge | Q_{gd} | | - | - | 5.1 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = -30\text{ V}$, $I_D = -6.7\text{ A}$, $R_G = 24\text{ }\Omega$, $R_D = 4.0\text{ }\Omega$, see fig. 10 ^b | - | 11 | - | ns |
| Rise Time | t_r | | - | 63 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 9.6 | - | |
| Fall Time | t_f | | - | 31 | - | |
| Internal Drain Inductance | L_D | Between lead, 6 mm (0.25") from package and center of die contact | - | 4.0 | - | nH |
| Internal Source Inductance | L_S | | - | 6.0 | - | |



| SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted | | | | | | |
|--|----------|---|------|-------|-------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | - 1.8 | A |
| Pulsed Diode Forward Current ^a | I_{SM} | | - | - | - 14 | |
| Body Diode Voltage | V_{SD} | $T_J = 25\text{ }^\circ\text{C}$, $I_S = -1.8\text{ A}$, $V_{GS} = 0\text{ V}^b$ | - | - | - 5.5 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^\circ\text{C}$, $I_F = -6.7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}^b$ | - | 80 | 160 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | - | 0.096 | 0.19 | μC |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D) | | | | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS $25\text{ }^\circ\text{C}$, unless otherwise noted

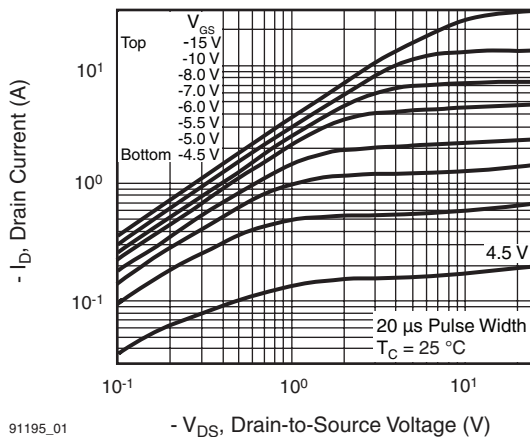


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

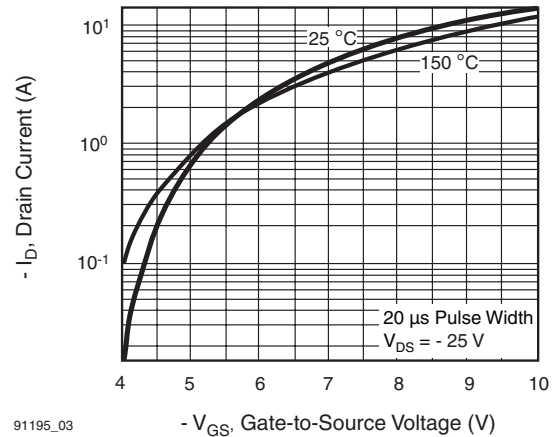


Fig. 3 - Typical Transfer Characteristics

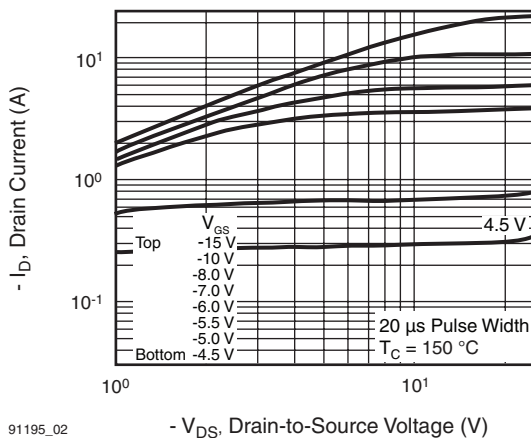


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

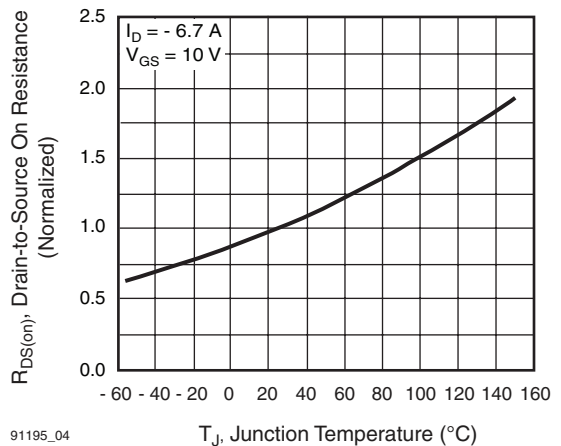
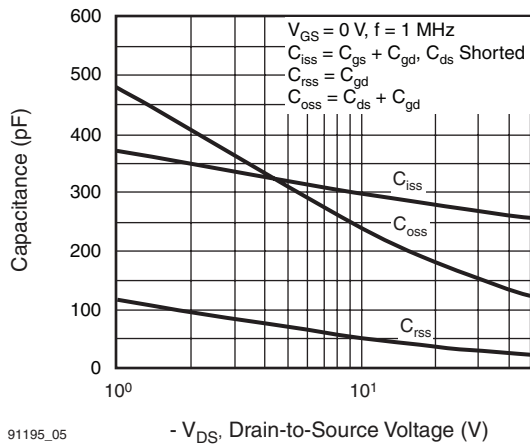
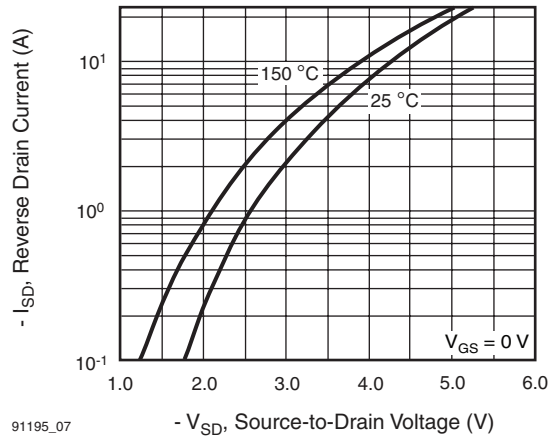


Fig. 4 - Normalized On-Resistance vs. Temperature



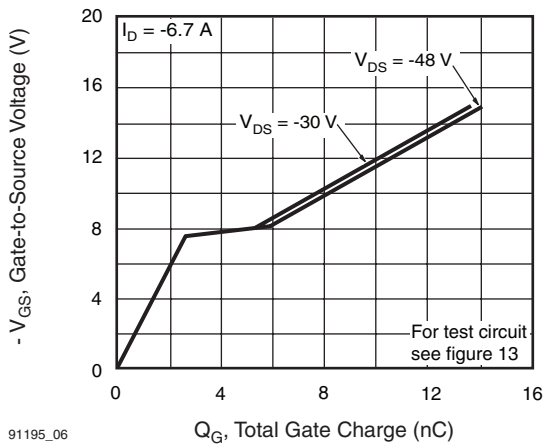
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Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



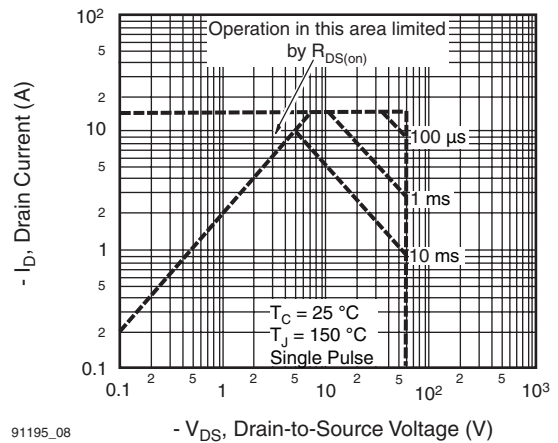
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



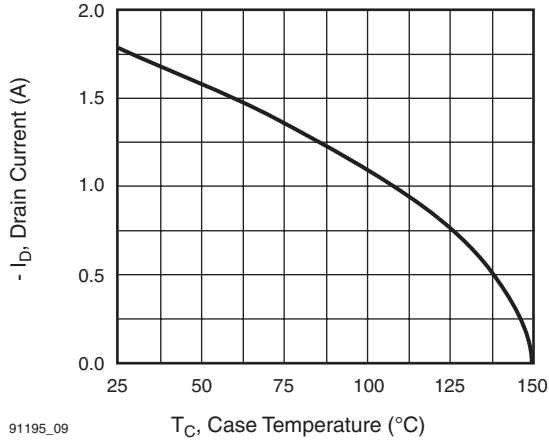
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Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



91195_08

Fig. 8 - Maximum Safe Operating Area



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Fig. 9 - Maximum Drain Current vs. Case Temperature

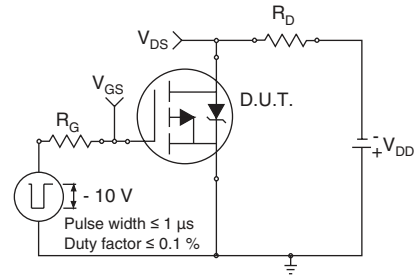


Fig. 10a - Switching Time Test Circuit

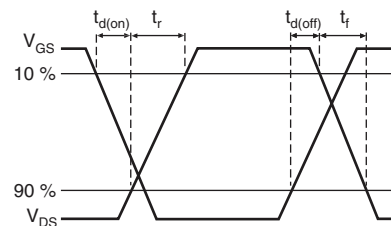
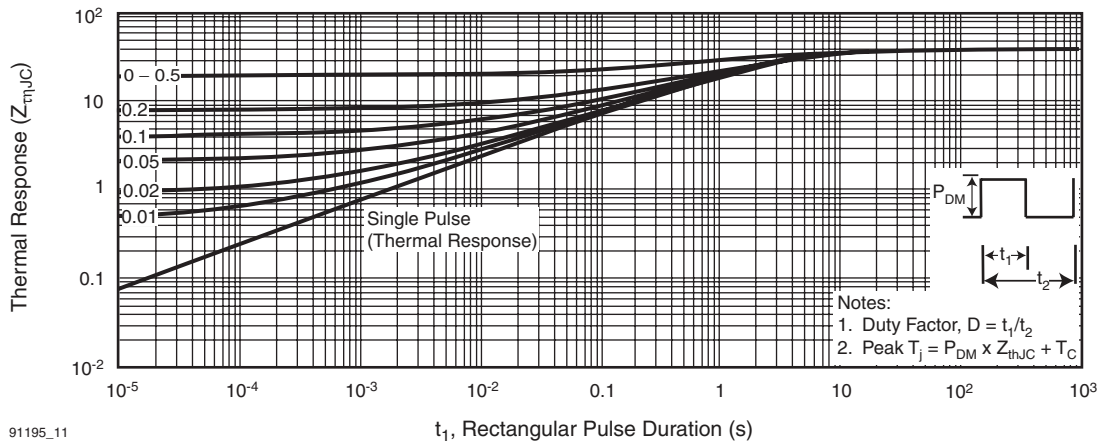


Fig. 10b - Switching Time Waveforms



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Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

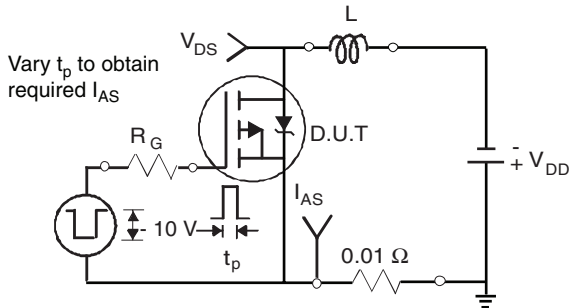


Fig. 12a - Unclamped Inductive Test Circuit

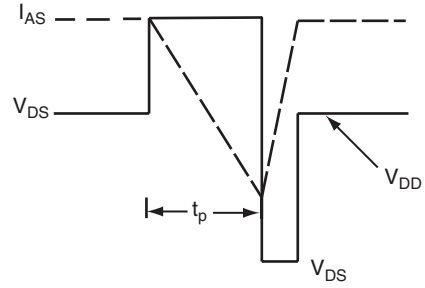


Fig. 12b - Unclamped Inductive Waveforms

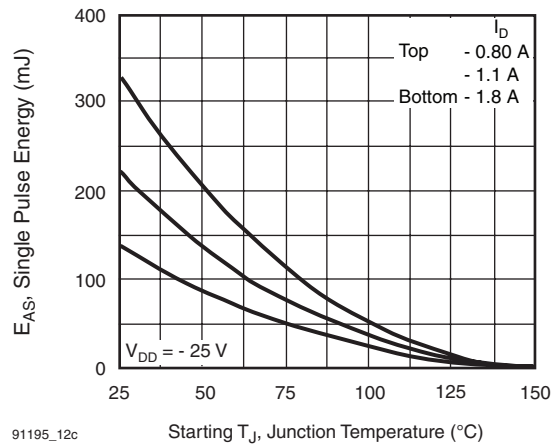


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

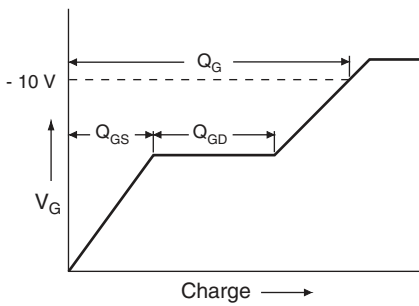


Fig. 13a - Basic Gate Charge Waveform

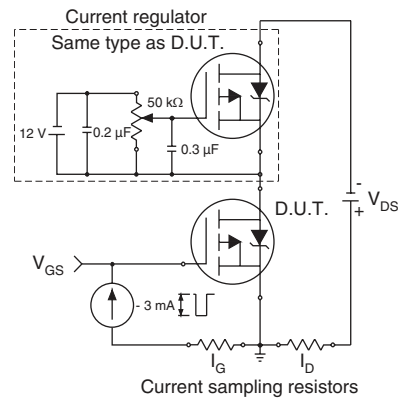
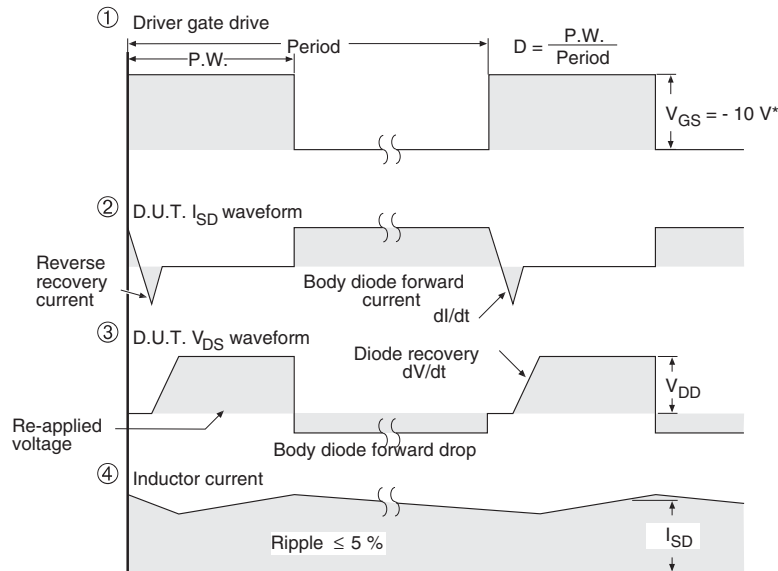
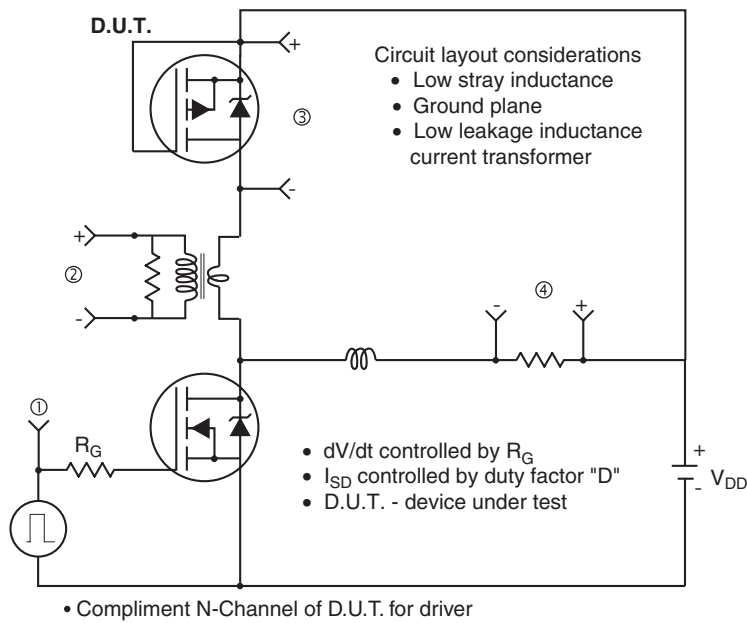


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = -5\text{ V}$ for logic level and -3 V drive devices

Fig.14 - For P-Channel

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