



Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

MAX512/MAX513

General Description

The MAX512/MAX513 contain three 8-bit, voltage-output digital-to-analog converters (DAC A, DAC B, and DAC C). Output buffer amplifiers for DACs A and B provide voltage outputs while reducing external component count. The output buffer for DAC A can source or sink 5mA to within 0.5V of V_{DD} or V_{SS} . The buffer for DAC B can source or sink 0.5mA to within 0.5V of V_{DD} or V_{SS} . DAC C is unbuffered, providing a third voltage output with increased accuracy. The MAX512 operates with a single +5V $\pm 10\%$ supply, and the MAX513 operates with a +2.7V to +3.6V supply. Both devices can also operate with split supplies.

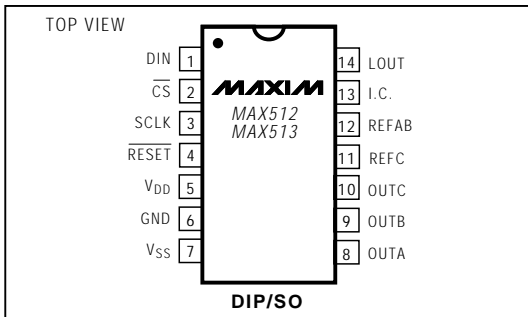
The 3-wire serial interface has a maximum operating frequency of 5MHz and is compatible with SPI™, QSPI™, and Microwire™. The serial input shift register is 16 bits long and consists of 8 bits of DAC input data and 8 bits for DAC selection and shutdown. DAC registers can be loaded independently or in parallel at the positive edge of \overline{CS} . A latched logic output is also available for auxiliary control.

Ultra-low power consumption and small packages (14-pin DIP/SO) make the MAX512/MAX513 ideal for portable and battery-powered applications. Supply current is only 1mA, dropping to less than 1 μ A in shutdown. Any of the three DACs can be independently shut down. In shutdown mode, the DAC's R-2R ladder network is disconnected from the reference input, minimizing system power consumption.

Applications

- Digital Gain and Offset Adjustment
- Programmable Attenuators
- Programmable Current Sources
- Programmable Voltage Sources
- RF Digitally Adjustable Bias Circuits
- VCO Tuning

Pin Configuration



Microwire is a trademark of National Semiconductor Corp. SPI and QSPI are trademarks of Motorola Inc.

Features

- ◆ Operate from a Single +5V (MAX512) or +3V (MAX513) Supply, or from Bipolar Supplies
- ◆ Low Power Consumption
1mA Operating Current
<1 μ A Shutdown Current
- ◆ Unipolar or Bipolar Outputs
- ◆ 5MHz, 3-Wire Serial Interface
- ◆ SPI, QSPI, and Microwire Compatible
- ◆ Two Buffered, Bipolar-Output DACs (DACs A/B)
- ◆ Independently Programmable Shutdown Mode
- ◆ Space-Saving 14-Pin SO/DIP Packages
- ◆ Pin and Software Reset

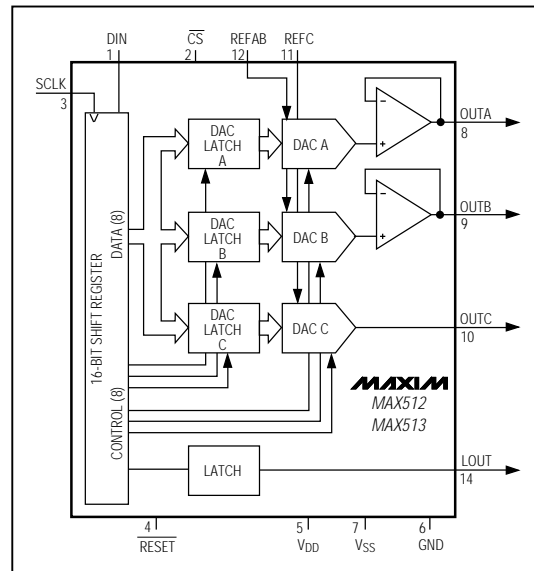
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX512CPD	0°C to +70°C	14 Plastic DIP
MAX512CSD	0°C to +70°C	14 SO
MAX512C/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

* Contact factory for dice specifications.

Functional Diagram



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ABSOLUTE MAXIMUM RATINGS

V _{DD} to GND	-0.3V, +6V	Continuous Power Dissipation (T _A = +70°C)	
V _{SS} to GND	-6V, +0.3V	Plastic DIP (derate 10.00mW/°C above +70°C)	800mW
V _{DD} to V _{SS}	-0.3V, +12V	SO (derate 8.33mW/°C above +70°C)	667mW
Digital Inputs and Outputs to GND	-0.3V, (V _{DD} + 0.3V)	CERDIP (derate 9.09mW/°C above +70°C)	727mW
REFAB	(V _{SS} - 0.3V), (V _{DD} + 0.3V)	Operating Temperature Ranges	
OUTA, OUTB (Note 1)	V _{SS} , V _{DD}	MAX51_C_	0°C to +70°C
OUTC	-0.3V, (V _{DD} + 0.3V)	MAX51_E_	-40°C to +85°C
REFC	-0.3V, (V _{DD} + 0.3V)	MAX51_MJD	-55°C to +125°C
		Storage Temperature Range	-65°C to +165°C
		Lead Temperature (soldering, 10sec)	+300°C

Note 1: The outputs may be shorted to V_{DD}, V_{SS}, or GND if the package power dissipation is not exceeded. Typical short-circuit current to GND is 50mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +4.5V to +5.5V for MAX512, V_{DD} = +2.7V to +3.6V for MAX513, V_{SS} = GND = 0V, REFAB = REFC = V_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		8			Bits
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Integral Nonlinearity	INL	DAC A/B (Note 2)			±1.5	LSB
		DAC C			±1	
Total Unadjusted Error	TUE	(Note 2)		±1		LSB
Zero-Code Temperature Coefficient		DAC A/B		100		µV/°C
		DAC C		5		
Power-Supply Rejection Ratio	PSRR	MAX512, 4.5V ≤ V _{DD} ≤ 5.5V, REFAB = REFC = 4.096V		0.01		%/%
		MAX513, 2.7V ≤ V _{DD} ≤ 3.6V, REFAB = REFC = 2.4V		0.015		
REFERENCE INPUTS						
Reference Input Voltage Range		REFAB	V _{SS}		V _{DD}	V
		REFC	GND		V _{DD}	
Reference Input Capacitance				25		pF
Reference Input Resistance	R _{REF}	REFAB (Note 3)		8		kΩ
		REFC (Note 3)		12		
Reference Input Resistance (shutdown mode)		REFAB, REFC		2		MΩ

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +4.5V$ to $+5.5V$ for MAX512, $V_{DD} = +2.7V$ to $+3.6V$ for MAX513, $V_{SS} = GND = 0V$, $REF_{AB} = REF_C = V_{DD}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC OUTPUTS						
Output Voltage Range			0		REF_{-}	V
Capacitive Load		DAC A	0.10			μF
		DAC B	0.01			
		DAC C	0			
Output Resistance		DAC A		0.050		$k\Omega$
		DAC B		0.500		
		DAC C		24		
DIGITAL INPUTS						
Input High Voltage	V_{IH}		(0.7)(V_{DD})			V
Input Low Voltage	V_{IL}			(0.3)(V_{DD})		V
Input Current	I_{IN}	$V_{IN} = 0V$ or V_{DD}		0.1	± 10	μA
Input Capacitance	C_{IN}	(Notes 4, 5)			10	pF
DIGITAL OUTPUT						
Output High Voltage	V_{OH}	$I_{SOURCE} \leq 1.6mA$	$V_{DD} - 0.4$			V
Output Low Voltage	V_{OL}	$I_{SINK} \leq 1.6mA$			0.4	V
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR	$C_L = 0.1\mu F$ (DAC A), $C_L = 0.01\mu F$ (DAC B)		0.1		V/ μs
Voltage-Output Settling Time		$T_o \pm 1/2LSB$	$C_L = 0.1\mu F$ (DAC A)	70		μs
			$C_L = 0.01\mu F$ (DAC B)	70		
			$C_L = 0.1nF$ (DAC C)	35		
Digital Feedthrough and Crosstalk		All 0s to all 1s		10		nV-s
POWER SUPPLIES						
Positive Supply Voltage Range	V_{DD}	MAX512	4.5		5.5	V
		MAX513	2.7		3.6	
Negative Supply Voltage Range (Note 6)	V_{SS}	MAX512	-5.5		-4.5	V
		MAX513	-3.6		-2.7	
Positive Supply Current	I_{DD}	All inputs = 0V	MAX512 ($V_{DD} = 5.5V$)	1.3	2.8	mA
			MAX513 ($V_{DD} = 3.6V$)	0.9	2.5	
Negative Supply Current	I_{SS}	All inputs = 0V, $V_{SS} = -5.5V$		-1.3		mA
Shutdown Supply Current				0.1		μA

Note 2: Digital code from 24 through 232 are due to swing limitations of output amplifiers on DAC A and DAC B. See *Typical Operating Characteristics*.

Note 3: Reference input resistance is code dependent. The lowest input resistance occurs at code 55hex. Refer to the reference input section in the *Detailed Description*.

Note 4: Guaranteed by design. Not production tested.

Note 5: Input capacitance is code dependent. The highest capacitance occurs at code 00hex.

Note 6: For single-supply mode, tie V_{SS} to GND.

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TIMING CHARACTERISTICS (Note 4)

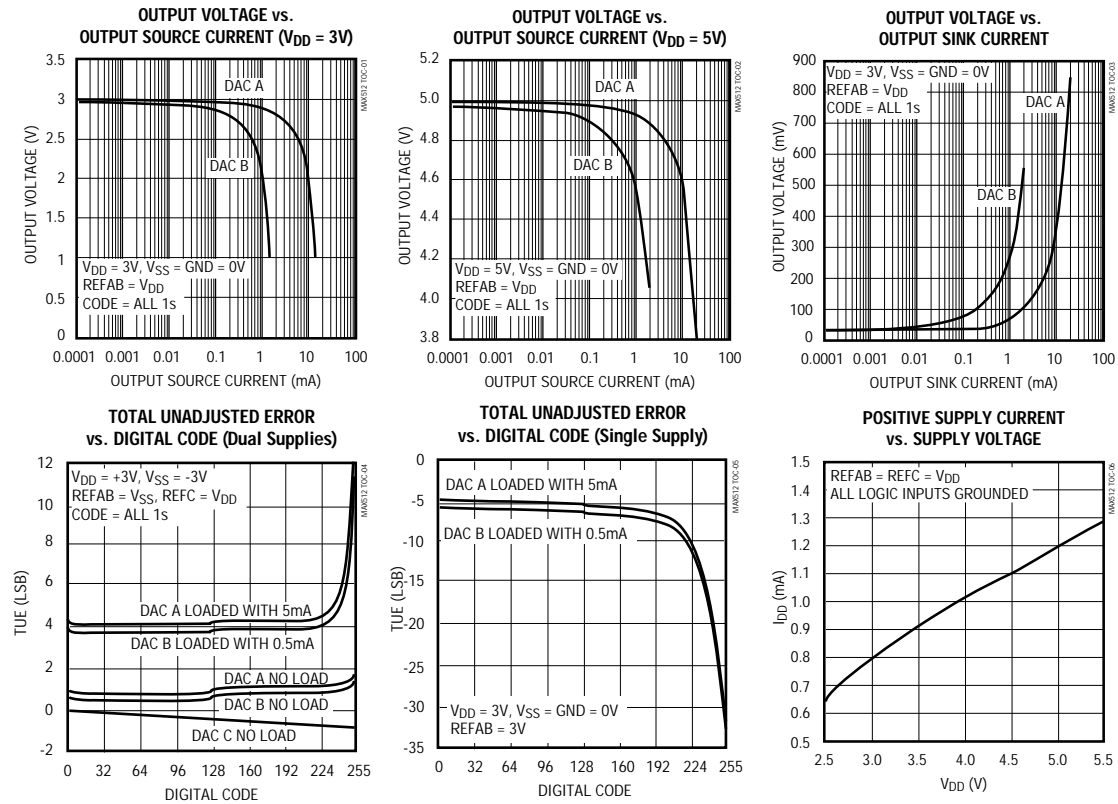
($V_{DD} = +4.5V$ to $+5.5V$ for MAX512, $V_{DD} = +2.7V$ to $+3.6V$ for MAX513, $V_{SS} = GND = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL INTERFACE TIMING						
\overline{CS} Fall to SCLK Rise Setup Time	t_{CSS}		150			ns
SCLK Rise to \overline{CS} Rise Setup Time	t_{CSH}		150			ns
DIN to SCLK Rise Setup Time	t_{DS}		50			ns
DIN to SCLK Rise Hold Time	t_{DH}		50			ns
SCLK Pulse Width High	t_{CH}		100			ns
SCLK Pulse Width Low	t_{CL}		100			ns
Output Delay LOUT	t_{OD}	$C_L = 100pF$			150	ns
\overline{CS} Pulse Width High	t_{CSPWH}		200			ns

Note 4: Guaranteed by design. Not production tested.

Typical Operating Characteristics

($T_A = +25^\circ C$, unless otherwise noted.)

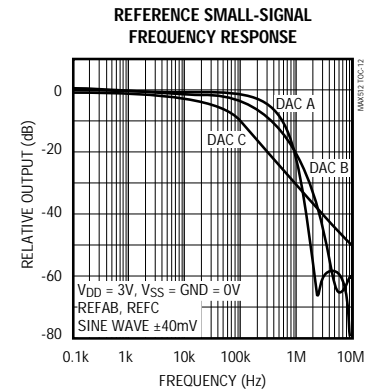
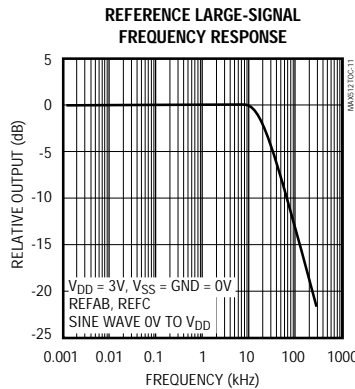
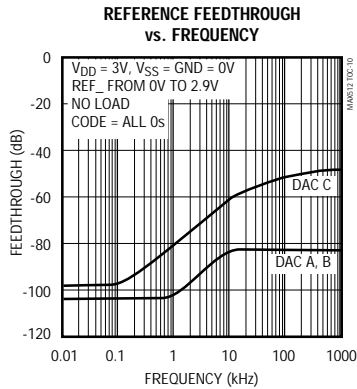
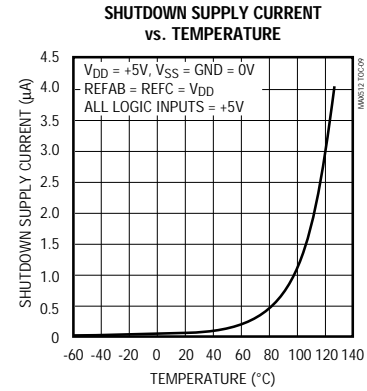
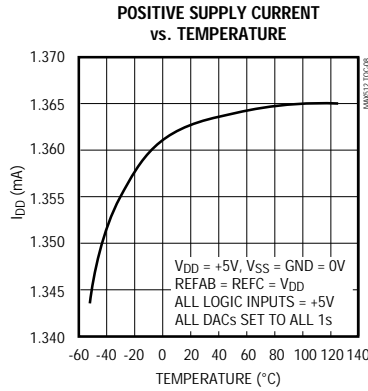
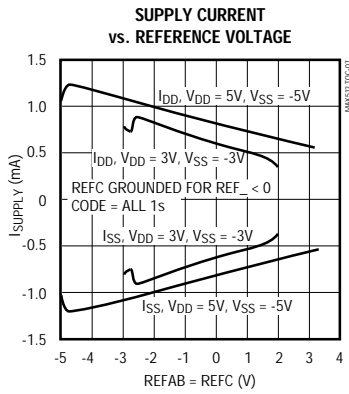


Low-Cost, Triple, 8-Bit Voltage Output DACs with Serial Interface

Typical Operating Characteristics (continued)

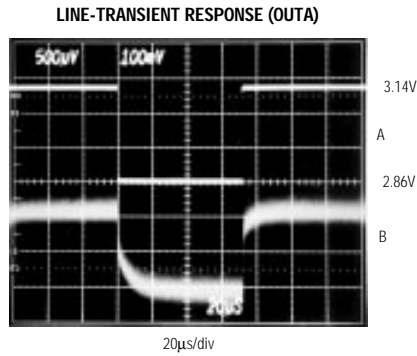
($T_A = +25^\circ\text{C}$, unless otherwise noted.)

MAX512/MAX513

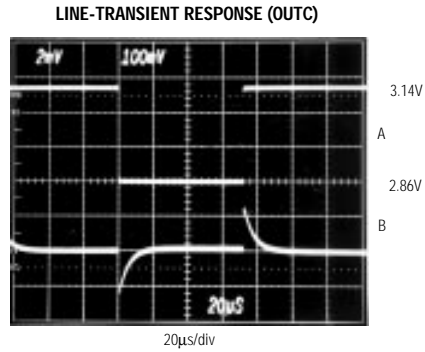


Low-Cost, Triple, 8-Bit Voltage Output DACs with Serial Interface

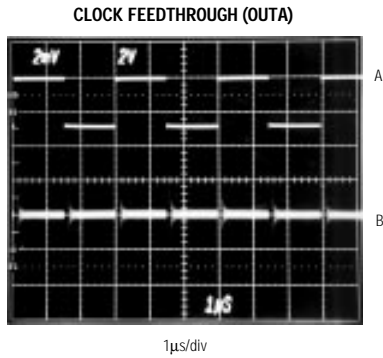
Typical Operating Characteristics (continued)
 (T_A = +25°C, unless otherwise noted.)



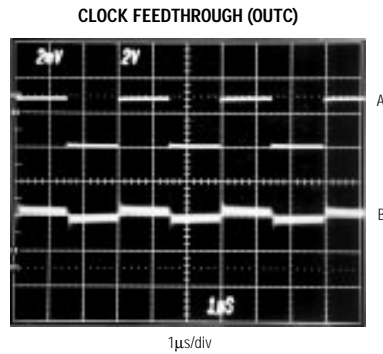
REFAB = 2.56V, NO LOAD, CODE = ALL 1s
 A: V_{DD}, 100mV/div
 B: OUTA, 500µV/div



REFC = 2.56V, NO LOAD, CODE = ALL 1s
 A: V_{DD}, 100mV/div
 B: OUTC, 2mV/div



V_{SS} = 0V, \overline{CS} = HIGH
 A: SCLK, 333kHz, 0V TO 2.9V, 2V/div
 B: OUTA, 2mV/div



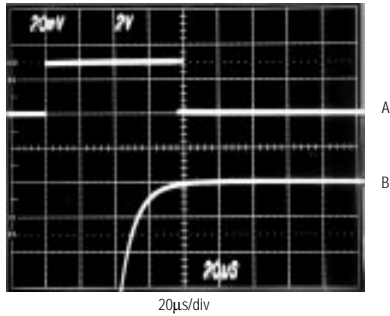
V_{SS} = 0V, \overline{CS} = HIGH
 A: SCLK, 333kHz, 0V TO 2.9V, 2V/div
 B: OUTC, 2mV/div

Low-Cost, Triple, 8-Bit Voltage Output DACs with Serial Interface

MAX512/MAX513

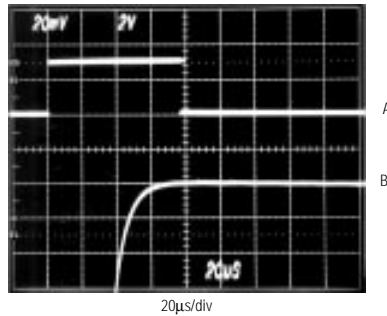
Typical Operating Characteristics (continued)
 (TA = +25°C, unless otherwise noted.)

POSITIVE SETTLING TIME (DAC A)



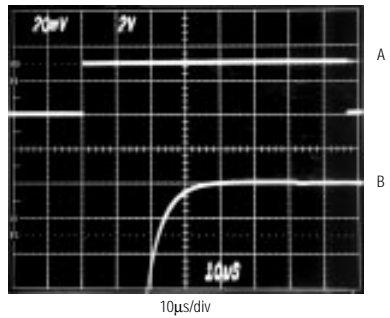
V_{DD} = 3V, V_{SS} = 0V, REFAB = V_{DD}, R_L = 1k Ω, C_L = 0.1µF
 ALL BITS OFF TO ALL BITS ON
 A: $\overline{\text{CS}}$, 2V/div
 B: OUTA, 20mV/div

POSITIVE SETTLING TIME (DAC B)



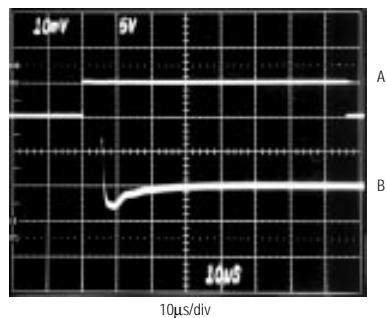
V_{DD} = 3V, V_{SS} = 0V, REFAB = V_{DD}, R_L = 10k Ω, C_L = 0.01µF
 ALL BITS OFF TO ALL BITS ON
 A: $\overline{\text{CS}}$, 2V/div
 B: OUTB, 20mV/div

POSITIVE SETTLING TIME (DAC C)



V_{DD} = 3V, V_{SS} = 0V, REFC = V_{DD}, R_L = ∞, C_L = 122pF
 ALL BITS OFF TO ALL BITS ON
 A: $\overline{\text{CS}}$, 2V/div
 B: OUTC, 20mV/div

POSITIVE SETTLING TIME WITH DUAL SUPPLIES



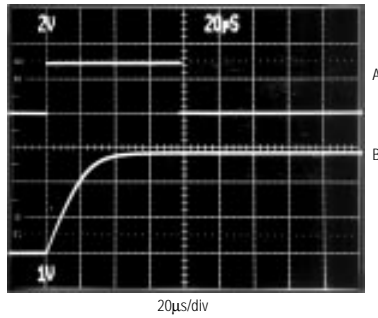
V_{DD} = 5V, V_{SS} = -5V, REFAB = 2.56V, R_L = 1k Ω, C_L = 0.1µF
 ALL BITS OFF TO ALL BITS ON
 A: $\overline{\text{CS}}$, 5V/div
 B: OUTA, 10mV/div

Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

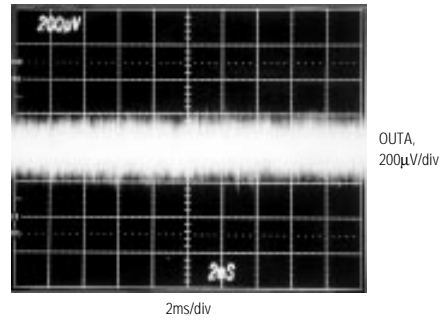
TIME EXITING SHUTDOWN MODE



$V_{DD} = 3\text{V}$, $V_{SS} = 0\text{V}$, $\text{REFAB} = V_{DD}$, $R_L = 1\text{k}\Omega$, $C_L = 0.1\mu\text{F}$
DAC LOADED WITH ALL 1s

A: $\overline{\text{CS}}$, 2V/div
B: OUTA, 1V/div

OUTPUT VOLTAGE NOISE DC TO 1MHz



DIGITAL CODE = 80, $\text{REFAB} = V_{DD}$, NO LOAD

Pin Description

PIN	NAME	FUNCTION
1	DIN	Serial Data Input of the 16-bit shift register. Data is clocked into the register on the rising edge of SCLK.
2	$\overline{\text{CS}}$	Chip Select (active low). Enables data to be shifted into the 16-bit shift register. Programming commands are executed at the rising edge of $\overline{\text{CS}}$.
3	SCLK	Serial Clock Input. Data is clocked in on the rising edge of SCLK.
4	$\overline{\text{RESET}}$	Asynchronous reset input (active low). Clears all registers to their default state (FFhex for DAC A and DAC B registers); all other registers are reset to 0 (including the input shift register).
5	V_{DD}	Positive Power Supply (2.7V to 5.5V). Bypass with 0.22 μF to GND.
6	GND	Ground
7	V_{SS}	Negative Power Supply 0V or (-1.5V to -5.5V). Tie to GND for single supply operation. If a negative supply is applied, bypass with 0.22 μF to GND.
8	OUTA	DAC A Output Voltage (Buffered). Resets to full scale. Connect 0.1μF capacitor or greater to GND.
9	OUTB	DAC B Output Voltage (Buffered). Resets to full scale. Connect 0.01μF capacitor or greater to GND.
10	OUTC	DAC C Output Voltage (Unbuffered). Resets to zero.
11	REFC	DAC C Reference Voltage
12	REFAB	DAC A/B Reference Voltage
13	I.C.	Internally connected. Do not make connections to this pin.
14	LOUT	Logic Output (latched)

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MAX512/MAX513

Detailed Description

Analog Section

The MAX512/MAX513 contain three 8-bit, voltage-output, digital-to-analog converters (DACs). The DACs are “inverted” R-2R ladder networks using complementary switches that convert 8-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltages.

The MAX512/MAX513 have two reference inputs: one is shared by DAC A and DAC B and the other is used by DAC C. These inputs allow different full-scale output voltages and different output voltage polarities for the DAC pair A/B and DAC C.

The MAX512/MAX513 include output buffer amplifiers for DACs A and B and input logic for simple micro-processor (μP) and CMOS interfaces.

The MAX512/MAX513 operate in either single-supply or dual-supply mode, as determined by V_{SS} . If V_{SS} is within approximately -0.5V of GND, single-supply mode is assumed. If V_{SS} is below -1.5V , the devices are in dual-supply mode.

Reference Inputs and DAC Output Range

The voltage at REF₋ sets the full-scale output of the DACs. The input impedance of the REF₋ inputs is code dependent. The lowest value, approximately $12\text{k}\Omega$ for REFC ($8\text{k}\Omega$ for REFAB), occurs when the input code is 01010101 (55hex). The maximum value of infinity occurs when the input code is zero.

In shutdown mode, the selected DAC output is set to zero while the value stored in the DAC register remains unchanged. This removes the load from the reference input to save power. Bringing the MAX512/MAX513 out of shutdown mode restores the DAC output voltage. Because the input resistance at REF₋ is code dependent, the DAC's reference sources should have an output impedance of no more than 5Ω . The input capacitance at the REF₋ pins is also code dependent and typically does not exceed 25pF .

The reference voltage on REFAB can range anywhere between the supply rails. In dual-supply mode, a positive reference input voltage on REFAB should be less than $(V_{DD} - 1.5\text{V})$ to avoid saturating the buffer amplifiers. The reference voltage includes the negative supply rail. See the *Output Buffer Amplifier* section for more information. The REFC input accepts positive voltages up to V_{DD} and should not be forced below ground.

The absolute difference between any reference voltage and GND should not exceed 6V .

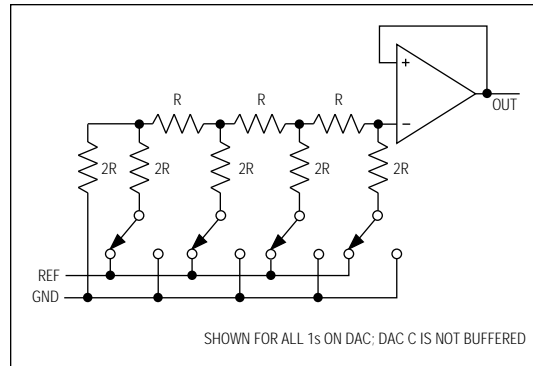


Figure 1. DAC Simplified Circuit Diagram

Output Buffer Amplifiers (DAC A / DAC B)

DAC A and DAC B voltage outputs are internally buffered. The buffer amplifiers have a rail-to-rail (V_{SS} to V_{DD}) output voltage range.

In single-supply mode, the DAC outputs A and B are internally divided by two and the buffer is set to a gain of two, eliminating the need for a buffer input voltage range to the positive supply rail.

In dual-supply mode, the DAC outputs are not attenuated and the buffer is set to unity gain.

Although only necessary for negative output voltages, the dual-supply mode may be used even if the desired DAC output voltage is positive. Possible errors associated with the divide-by-two attenuator and gain-of-two buffers in single-supply mode are eliminated in dual-supply mode. In this case, do not use reference voltages higher than $(V_{DD} - 1.5\text{V})$.

DAC A's output amplifier can source and sink up to 5mA of current (0.5mA for DAC B buffer). See the Total Unadjusted Error vs. Digital Code graph in the *Typical Operating Characteristics* for dual and single supplies. The amplifier is unity-gain stable with a capacitive load of $0.05\mu\text{F}$ ($0.01\mu\text{F}$ for DAC B buffer) or greater. The slew rate is limited by the load capacitor and is typically $0.1\text{V}/\mu\text{s}$ with a $0.1\mu\text{F}$ load ($0.01\mu\text{F}$ for DAC B buffer).

Unbuffered Output (DAC C)

The output of DAC C is unbuffered and has a typical output impedance of $24\text{k}\Omega$. It can be used to drive a high-impedance load, such as an op amp or comparator, and has $35\mu\text{s}$ typical settling time to $1/2\text{LSB}$ with a single 3V supply. Use DAC C if a quick dynamic response is required.

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Shutdown Mode

When programmed to shutdown mode, the outputs of DAC A and B go into a high-impedance state. Virtually no current flows into or out of the buffer amplifiers in that state. The output of DAC C goes to 0V when shut down. In shutdown mode, the REF_ inputs are high impedance (2MΩ typ) to conserve current drain from the system reference; therefore, the system reference does not have to be powered down. The logic output LOUT remains active in shutdown.

Coming out of shutdown, the DAC outputs return to the values kept in the registers. The recovery time is equivalent to the DAC settling time.

Reset

The RESET input is active low. When asserted (RESET = 0), DACs A and B are set to full scale (FFhex) and active, while DAC C is set to zero code (00hex) and active. The 16-bit serial register is cleared to 0000hex. LOUT is reset to zero.

Serial Interface

An active-low chip select (\overline{CS}) enables the shift register to receive data from the serial data input. Data is clocked into the shift register on every rising edge of the serial clock signal (SCLK). The clock frequency can be as high as 5MHz.

Data is sent MSB first and can be transmitted in one 16-bit word. The write cycle can be interrupted at any time when \overline{CS} is kept active (low) to allow, for example, two 8-bit-wide transfers. After clocking all 16 bits into

Table 1. Input Shift Register

DATA BITS	B0*	DAC Data Bit 0 (LSB)
	B1	DAC Data Bit 1
	B2	DAC Data Bit 2
	B3	DAC Data Bit 3
	B4	DAC Data Bit 4
	B5	DAC Data Bit 5
	B6	DAC Data Bit 6
	B7	DAC Data Bit 7 (MSB)
CONTROL BITS	LA	Load Reg DAC A, Active High
	LB	Load Reg DAC B, Active High
	LC	Load Reg DAC C, Active High
	SA	Shut Down DAC A, Active High
	SB	Shut Down DAC B, Active High
	SC	Shut Down DAC C, Active High
	Q1	Logic Output
	Q2**	Uncommitted Bit

* Clocked in last.

**Clocked in first.

the input shift register, the rising edge of \overline{CS} updates the DAC outputs, the shutdown status, and the status of the logic output. Because of their single buffered structure, DACs cannot be simultaneously updated to different digital values.

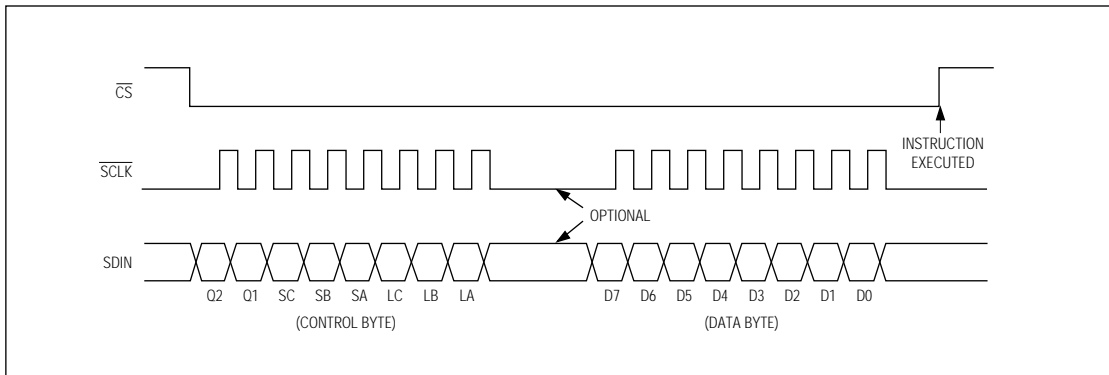


Figure 2. MAX512/MAX513 3-Wire Serial-Interface Timing Diagram

Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

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Table 2. Serial-Interface Programming Commands

CONTROL									DATA								FUNCTION
Q2	Q1	SC	SB	SA	LC	LB	LA	MSB				LSB					
								B7	B6	B5	B4	B3	B2	B1	B0		
*	*	*	*	*	0	0	0	X	X	X	X	X	X	X	X	X	No Operation to DAC Registers
*	*	*	*	*	1	0	0	8-Bit DAC Data								Load Register to DAC C	
*	*	*	*	*	0	1	0	8-Bit DAC Data								Load Register to DAC B	
*	*	*	*	*	0	0	1	8-Bit DAC Data								Load Register to DAC A	
*	*	*	*	*	1	1	1	8-Bit DAC Data								Load All DAC Registers	
*	*	0	0	0	*	*	*	X	X	X	X	X	X	X	X	X	All DACs Active
*	*	1	0	0	*	*	*	X	X	X	X	X	X	X	X	X	Shut Down DAC C
*	*	0	1	0	*	*	*	X	X	X	X	X	X	X	X	X	Shut Down DAC B
*	*	0	0	1	*	*	*	X	X	X	X	X	X	X	X	X	Shut Down DAC A
*	*	1	1	1	*	*	*	X	X	X	X	X	X	X	X	X	Shut Down All DACs
X	0	*	*	*	*	*	*	X	X	X	X	X	X	X	X	X	Reset LOUT
X	1	*	*	*	*	*	*	X	X	X	X	X	X	X	X	X	Set LOUT

X Don't care.

* Not shown for clarity. The functions of loading and shutting down the DACs and programming the logic can be combined in a single command.

Serial-Input Data Format and Control Codes

Table 2 lists the serial-input data format. The 16-bit input word consists of an 8-bit control byte and an 8-bit data byte. The 8-bit control byte is not decoded internally. Every control bit performs one function. Data is clocked in starting with Q2 (uncommitted bit), followed by the remaining control bits and the data byte. The LSB of the data byte (B0) is the last bit clocked into the shift register (Figure 2).

Example of a 16-bit input word:

Loaded in First								Loaded in Last							
Q2	Q1	SC	SB	SA	LC	LB	LA	B7	B6	B5	B4	B3	B2	B1	B0
X	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0

The example above performs the following functions:

- 80hex (128 decimal) loaded into DAC registers A and B.
- Content of the DAC C register remains unchanged.
- DAC A and DAC B are active.
- DAC C is shut down.
- LOUT is reset to 0.

Digital Inputs

The digital inputs are compatible with CMOS logic. Supply current increases slightly when toggling the logic inputs through the transition zone between $(0.3)(V_{DD})$ and $(0.7)(V_{DD})$.

Digital Output

The latched digital output (LOUT) has a 1.6mA source capability while maintaining a $(V_{DD} - 0.4V)$ output level. With a 1.6mA sink current, the output voltage is guaranteed to be no more than 0.4V. The output can be used for digital auxiliary control. Please note that the digital output remains fully active during shutdown mode.

Microprocessor Interfacing

The MAX512/MAX513 serial interface is compatible with Microwire, SPI, and QSPI. For SPI and QSPI, clear the CPOL and CPHA bits (CPOL = 0 and CPHA = 0). CPOL = 0 sets the inactive state of clock to zero and CPHA = 0 changes data at the falling edge of SCLK. This setting allows both SPI and QSPI to run at full clock speeds (0.5MHz and 4MHz, respectively). If a serial port is not available on your μP , three bits of a parallel port can be used to emulate a serial port by bit manipulation. Minimize digital feedthrough at the voltage outputs by operating the serial clock only when necessary.

Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

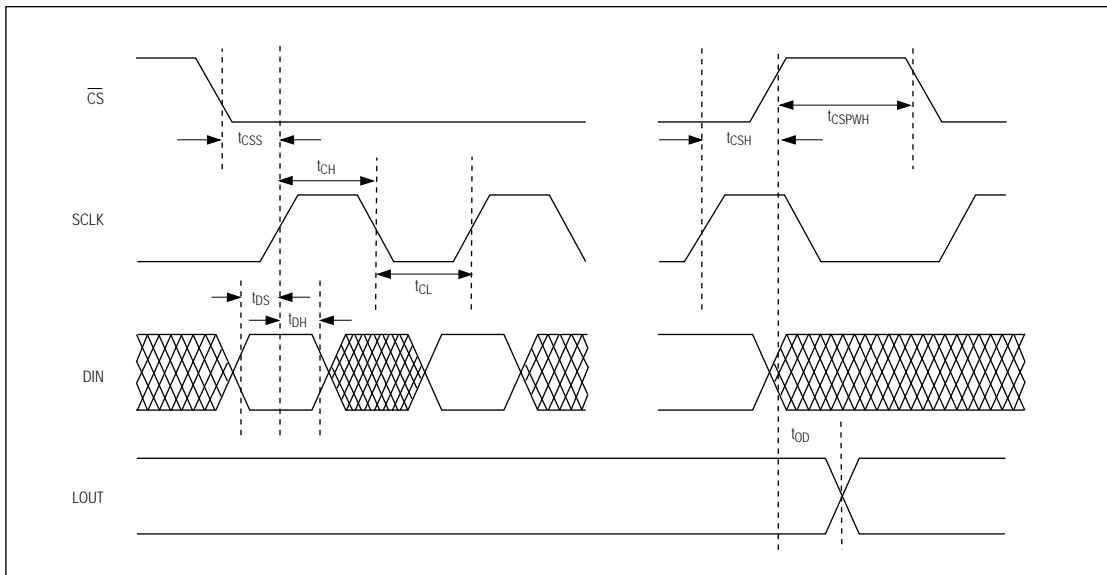


Figure 3. MAX512/MAX513 Detailed Serial-Interface Timing Diagram

Applications Information

Power-Supply and Reference Operating Ranges

The MAX512 is fully specified to operate with $V_{DD} = 5V \pm 10\%$ and $V_{SS} = GND = 0V$. The MAX513 is specified for single-supply operation with V_{DD} ranging from 2.7V to 3.6V, covering all commonly used supply voltages in 3V systems. The MAX512/MAX513 can also be used with a negative supply ranging from -1.5V to -5.5V. Using a negative supply typically improves zero-code error and settling time (as shown in the *Typical Operating Characteristics* graphs).

The two separate reference inputs for the DAC pair A/B and the unbuffered output C allow different full-scale output voltages and, if a negative supply is used, also allow different polarity. In dual-supply mode, REFAB can vary from V_{SS} to $(V_{DD} - 1.5V)$. In single-supply mode, the specified range for REFAB is 0V to V_{DD} . REFC can range from GND to V_{DD} . Do not force REFC below ground.

Power-supply sequencing is not critical. If a negative supply is used, make sure V_{SS} is never more than 0.3V above ground. Do not apply signals to the digital inputs until the device is powered-up. If this is not possible, add current-limiting resistors to the digital inputs.

Power-Supply Bypassing and Ground Management

In single-supply operation ($V_{SS} = GND$), GND and V_{SS} should be connected to the highest quality ground available. Bypass V_{DD} with a 0.1 μ F to 0.22 μ F capacitor to GND. For dual-supply operation, bypass V_{SS} with a 0.1 μ F to 0.22 μ F capacitor to GND. Reference inputs can be used without bypassing. For optimum line/load-transient response and noise performance, bypass the reference inputs with 0.1 μ F to 4.7 μ F to GND. Careful PC board layout minimizes crosstalk among DAC outputs, reference inputs, and digital inputs. Separate analog lines with ground traces between them. Make sure that high-frequency digital lines are not routed in parallel to analog lines.

Unipolar Output

With unipolar output, the output voltage and the reference voltage are the same polarity. The MAX512/MAX513 can be used with a single supply if the reference voltages are positive. With a negative supply, the REFAB voltage can vary from V_{SS} to approximately $(V_{DD} - 1.5V)$, allowing two-quadrant multiplication.

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Table 3. Unipolar Code Table

DAC CONTENTS								ANALOG OUTPUT
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	1	1	1	1	1	1	$+REF_- \times \left(\frac{255}{256}\right)$
1	0	0	0	0	0	0	1	$+REF_- \times \left(\frac{129}{256}\right)$
1	0	0	0	0	0	0	0	$+REF_- \times \left(\frac{128}{256}\right) = +\frac{REF_-}{2}$
0	1	1	1	1	1	1	1	$+REF_- \times \left(\frac{127}{256}\right)$
0	0	0	0	0	0	0	1	$+REF_- \times \left(\frac{1}{256}\right)$
0	0	0	0	0	0	0	0	0V

Note :

$$1\text{LSB} = REF_- \times 2^{-8} = REF_- \times \left(\frac{1}{256}\right)$$

$$\text{ANALOG OUTPUT} = REF_- \times \left(\frac{D}{256}\right)$$

Bipolar Output

Using Figure 4's circuit, the MAX512/MAX13 can be configured for bipolar outputs. Table 4 lists the bipolar codes and corresponding output voltages. There are two ways to achieve rail-to-rail outputs: 1) Operate the MAX512/MAX513 with a single supply and positive reference voltages or 2) Use dual supplies with a positive or negative voltage at REFAB and a positive voltage at REFC. In either case, the op amps need dual supplies. When using the dual-supply mode, possible errors associated with the divide-by-two attenuator and gain-of-two buffer are eliminated (see the *Output Buffer Amplifier* section). For maximum output swing of all outputs in dual-supply mode, connect REFAB to V_{SS} and REFC to V_{DD} . In single-supply mode, connect REFAB, REFC, and V_{DD} together.

With dual supplies, DACs A and B can perform four-quadrant multiplication. Please note that in dual-supply mode, the REFAB input ranges from V_{SS} to ($V_{DD} - 1.5V$). Because REFC accepts only positive inputs, DAC C performs two-quadrant multiplication.

Figure 4 shows Maxim's ICL7612A with rail-to-rail input common-mode range and rail-to-rail output voltage swing—ideal for a high output voltage swing from low supply voltages.

Table 4. Bipolar Code Table

DAC CONTENTS								ANALOG OUTPUT
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	1	1	1	1	1	1	$+REF_- \times \left(\frac{127}{128}\right)$
1	0	0	0	0	0	0	1	$+REF_- \times \left(\frac{1}{128}\right)$
1	0	0	0	0	0	0	0	0V
0	1	1	1	1	1	1	1	$-REF_- \times \left(\frac{1}{128}\right)$
0	0	0	0	0	0	0	1	$-REF_- \times \left(\frac{127}{128}\right)$
0	0	0	0	0	0	0	0	$-REF_- \times \left(\frac{128}{128}\right) = -REF_-$

Note :

$$1\text{LSB} = REF_- \times 2^{-(8-1)} = REF_- \times \left(\frac{1}{128}\right)$$

$$\text{ANALOG OUTPUT} = REF_- \times \left(\frac{D}{128} - 1\right)$$

RF Applications

Both the MAX512 and MAX513 can bias GaAs FETs, where the gate of the FETs must be negatively biased to ensure that there is no drain current. In a typical application, power to the RF amplifiers should not be turned on until the bias voltages provided by DAC A and DAC B are fully established; likewise, the supply should be turned off before the bias voltage is switched off. Figure 5 shows how DAC B supplies the negative bias V_{GG1} for the driver stage and DAC A provides the negative bias V_{GG2} for the output stage [1].

The DAC A and DAC B outputs are also ideal for controlling VCOs in mobile radios or cellular phones. Other applications include varactor and PIN diode circuits.

The unbuffered DAC C provides a span within GND and V_{DD} and is individually set at REF C. DAC C typically adjusts offset and gain in the system.

1 [John Wachsmann. "A High-Efficiency GaAs MMIC Power Amplifier for 1.9GHz PCS Applications," Proceedings of the First Annual Wireless Symposium, pp. 375, Penton Publishing, Jan. 1993.]

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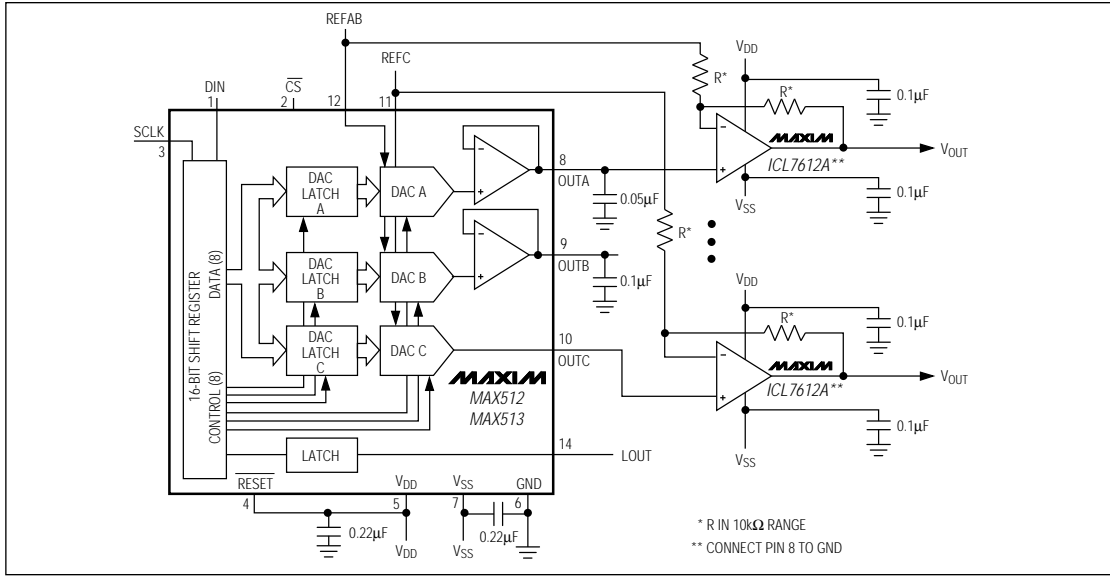


Figure 4. Bipolar Output Circuit

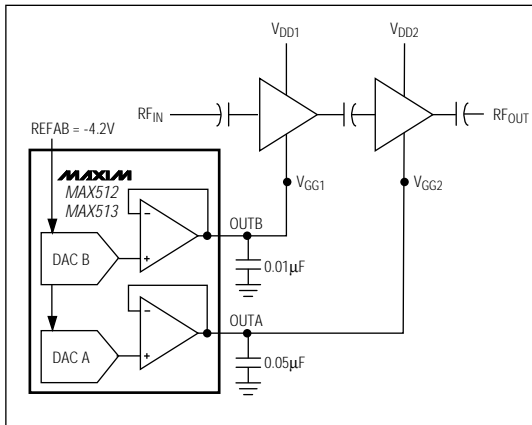


Figure 5. RF Bias Circuit

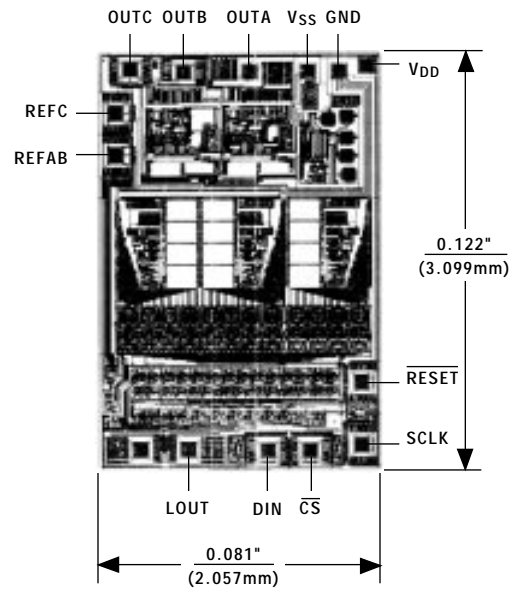
Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX512EPD	-40°C to +85°C	14 Plastic DIP
MAX512ESD	-40°C to +85°C	14 SO
MAX512MJD	-55°C to +125°C	14 CERDIP
MAX513 CPD	0°C to +70°C	14 Plastic DIP
MAX513CSD	0°C to +70°C	14 SO
MAX513C/D	0°C to +70°C	Dice*
MAX513EPD	-40°C to +85°C	14 Plastic DIP
MAX513ESD	-40°C to +85°C	14 SO
MAX513MJD	-55°C to +125°C	14 CERDIP

* Contact factory for dice specifications.

Chip Topography

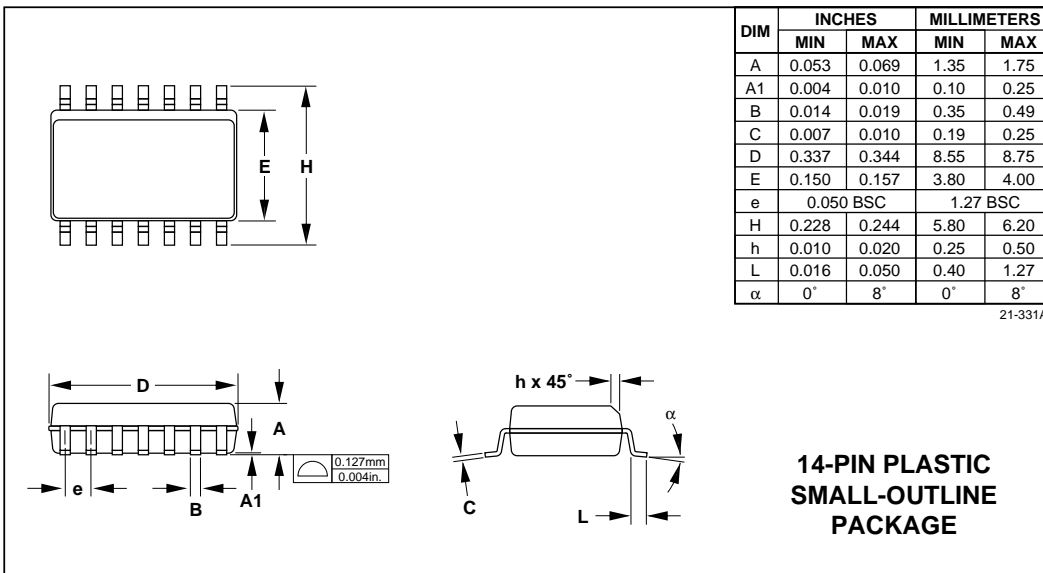
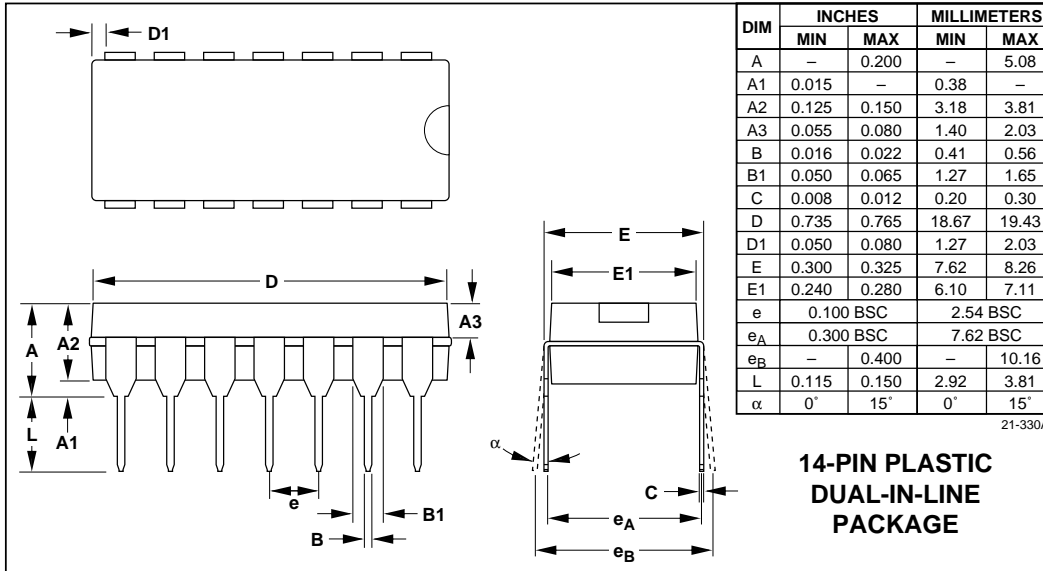


MAX512/MAX513

TRANSISTOR COUNT: 1910
SUBSTRATE CONNECTED TO V_{DD}

Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

Package Information



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