TPS61252 Tiny 1.5-A Boost Converter With Adjustable Input Current Limit

1 Features

- Resistor Programmable Input Current Limit
  - ±20% Current Accuracy at 500 mA over Full Temperature Range
  - Programmable from 100 mA up to 1500 mA
- Up to 92% Efficiency
- V_{IN} Range from 2.3 V to 6.0 V
- Power Good Indicates Appropriate Output Voltage Level
- Adjustable Output Voltage up to 6.5 V
- 100% Duty-Cycle Mode When $V_{IN} > V_{OUT}$
- Load Disconnect and Reverse Current Protection
- Short Circuit Protection
- Typical Operating Frequency 3.25 MHz
- Available in a 2-mm × 2-mm WSON-8 Package

2 Applications

- USB Host Supplies from a Single Li-Ion Battery
- Current Limited Applications
- Li-Ion Applications
- Audio Applications
- RF-PA Buffer

3 Description

The TPS61252 device provides a power supply solution for products powered by either a three-cell alkaline, NiCd or NiMH battery, or an one-cell Li-Ion or Li-polymer battery. The wide input voltage range is ideal to power portable applications like mobile phones or computer peripherals. The device has a resistor programmable (R_{ILIM}) input current limit and is suitable for a wide variety of applications.

During light loads, the device automatically enters skip mode (PFM), which allows the converter to maintain the required output voltage, while only drawing 30 µA quiescent current from the battery. This allows maximum efficiency at lowest quiescent currents.

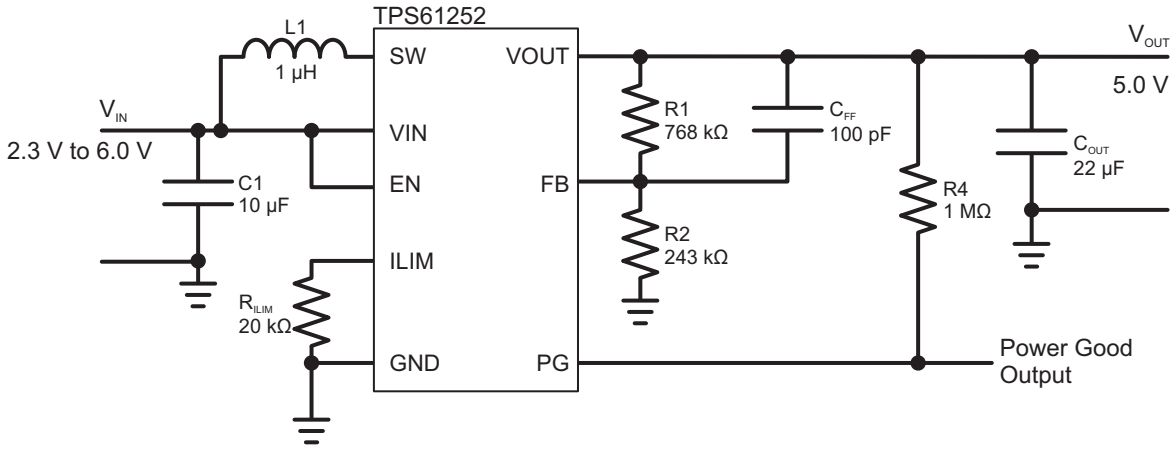
TPS61252 allows the use of small inductors and capacitors to achieve a small solution size. The possibility to reduce the current limit by a external resistor offers the potential use of physically even smaller inductors with lower rated currents to further reduce total solution sizes of the power supply. During shutdown, the load is completely disconnected from the battery. The TPS61252 is available in a 8-pin WSON package measuring 2 mm × 2 mm (DSG).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61252	WSON (8)	2.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Typical Application Schematic



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5 Revision History

Changes from Original (September 2010) to Revision A **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

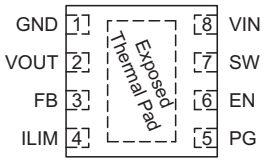
6 Device Options

T_A	OUTPUT VOLTAGE(1)	PACKAGE MARKING	PACKAGE	PART NUMBER(2)
–40°C to 85°C	Adjustable	QTI	8-Pin SON	TPS61252DSG

(1) Contact TI for other fixed output voltage options
(2) For detailed ordering information please check the *Mechanical, Packaging, and Orderable Information*.

7 Pin Configuration and Functions

DSG Package
8 Pins
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	6	I	Enable input. (1 enabled, 0 disabled). This pin must not be left floating and must be terminated
FB	3	I	Voltage feedback pin
GND	1		Ground
ILIM	4	I	Adjustable input valley current limit. A resistor to ground programs the current limit. Can be connected to V_{IN} for maximum current.
PG	5	O	Output power good (1 good, 0 failure; open drain).If unused, connect to ground or leave floating
SW	7	I	Connection for Inductor
VIN	8	I	Supply voltage for control stage
VOUT	2	O	Boost converter output
Exposed Thermal Pad	—	—	Must be soldered to achieve appropriate power dissipation and for mechanical reasons. Must be connected to GND.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN, VOUT, SW, EN, PG, FB, ILIM	–0.3	7	V
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

8.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage at VIN	2.3		6.0	V
Output voltage at VOUT	3.0		6.5	V
Programmable valley switch current limit set by R_{ILIM}	100		1500	mA
Operating free air temperature range, T_A	–40		85	°C
Operating junction temperature range, T_J	–40		125	°C

8.4 Thermal Information

THERMAL METRIC(1)		TPS61252 DSG 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	54.2	
ψ_{JT}	Junction-to-top characterization parameter	0.9	
ψ_{JB}	Junction-to-board characterization parameter	59.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	20	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

Over recommended free air temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6 V, V_{OUT} = 5.0 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC-DC STAGE						
V_{IN}	Input voltage		2.3		6	V
V_{FB}	Feedback voltage		1.182	1.2	1.218	V
	Lline regulation				0.5%	
	Load regulation				0.5%	
f	Oscillator frequency			3250		kHz
$r_{DS(on)}$	High side switch on resistance			200		mΩ
	Low side switch on resistance			130		mΩ
	Reverse leakage current into V_{OUT}	EN = GND			3.5	µA
I_{LIM}	Programmable valley switch current limit	ILIM pin set to V_{IN}		1500		mA
		R_{ILIM} = 20 kΩ (500mA)	-20%		+20%	
I_Q	Quiescent current	I_{OUT} = 0 mA, device not switching		30		µA
I_{SD}	Shutdown current			0.85	3.5	µA
OVP	Input over voltage protection threshold	Falling		6.4		V
		Rising		6.5		V
CONTROL STAGE						
V_{UVLO}	Under voltage lockout threshold	Falling		2.0	2.1	V
		Hysteresis		0.1		V
V_{IL}	EN input low voltage	2.3 V ≤ V_{IN} ≤ 6.0 V			0.4	V
V_{IH}	EN input high voltage	2.3 V ≤ V_{IN} ≤ 6.0 V	1.0			V
	EN, PG input leakage current	Clamped to GND or V_{IN}			0.5	µA
	Power Good threshold voltage	Rising (% V_{OUT})	92.5%	95%	97.5%	
		Falling (% V_{OUT})	87.5%	90%	92.5%	
	Power good delay			10		µs
	Overtemperature protection	Rising		140		°C
	Overtemperature hysteresis			20		°C

8.6 Typical Characteristics

Table 1. Table of Graphs

DESCRIPTION		FIGURE
Efficiency	vs Output current (V_{OUT} = 5.0 V, I_{LIM} = 1.5 A)	Figure 1
	vs Output current in 100% Duty-Cycle Mode (V_{OUT} = 5.0 V, I_{LIM} = 1.5 A)	Figure 2
	vs Input voltage (V_{OUT} = 5.0 V, I_{Load} = {10; 100; 1000 mA}) , I_{LIM} = 1.5 A	Figure 3
Maximum output current	vs Input voltage (V_{OUT} = 5.0 V)	Figure 4
Output voltage	vs Output current (V_{OUT} = 5.0V, I_{LIM} = 1.5 A)	Figure 5

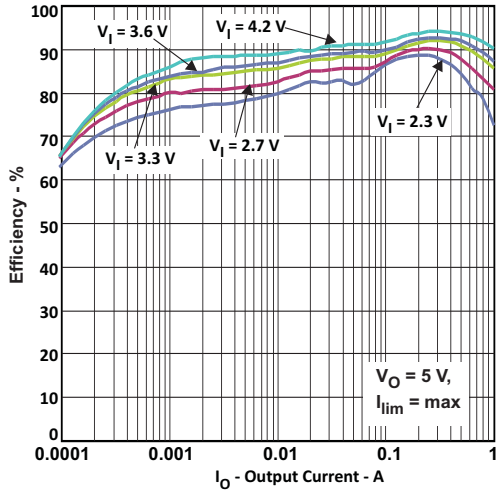


Figure 1. Efficiency vs Output Current

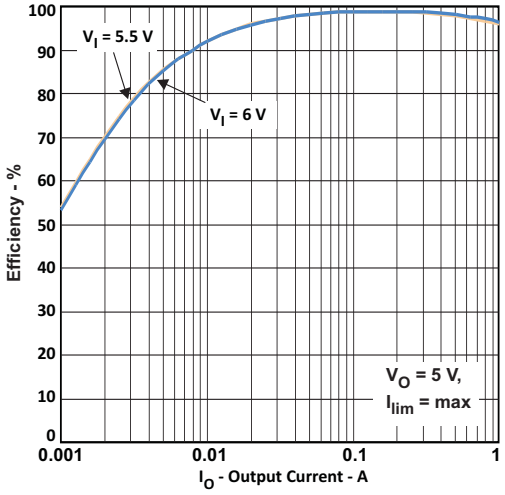


Figure 2. Efficiency vs Output Current In 100% Duty Cycle Mode

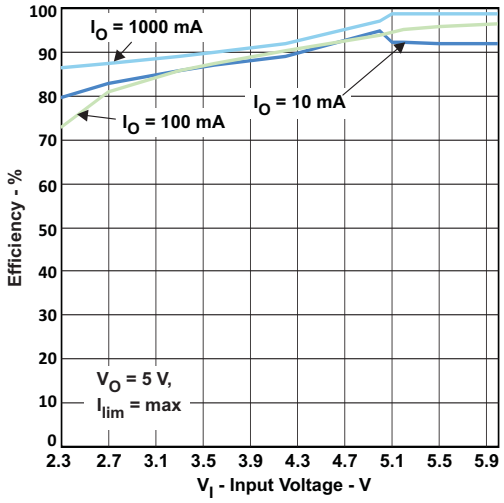


Figure 3. Efficiency vs Input Voltage

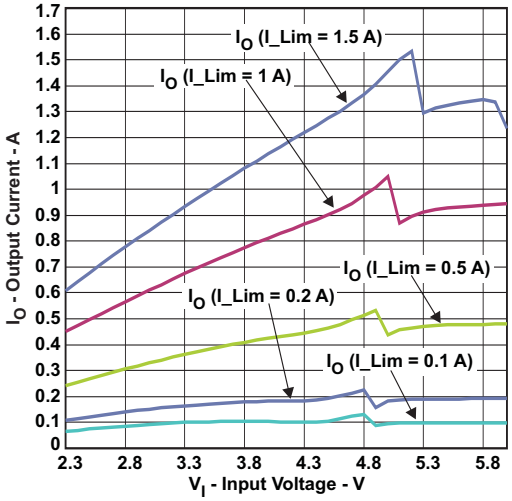


Figure 4. Maximum Output Current vs Input Voltage

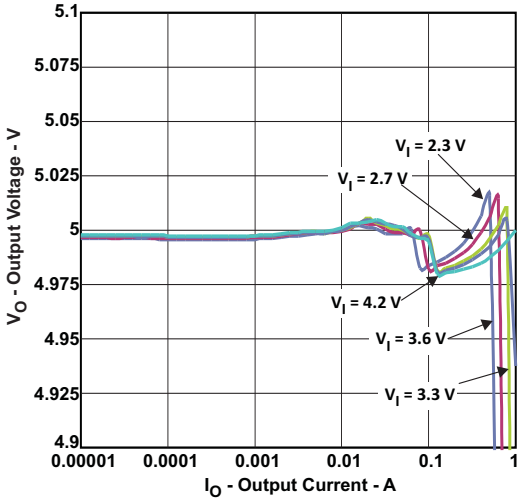


Figure 5. Output Voltage vs Output Current

9 Parameter Measurement Information

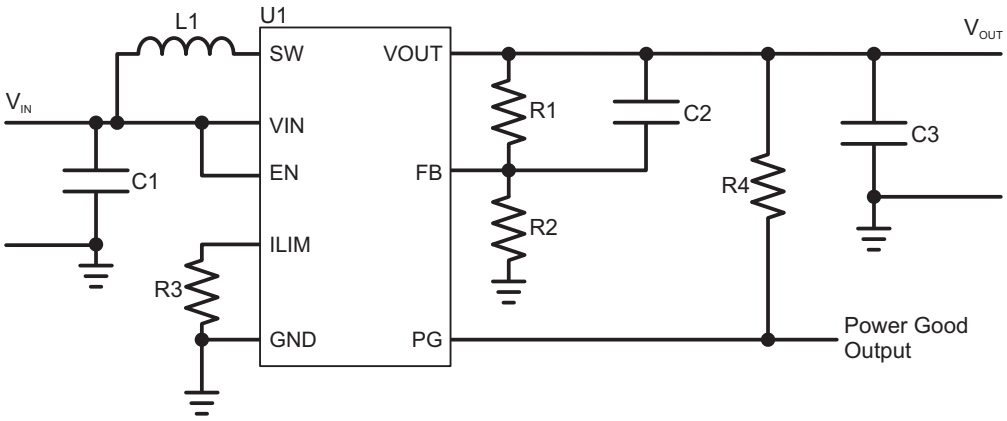


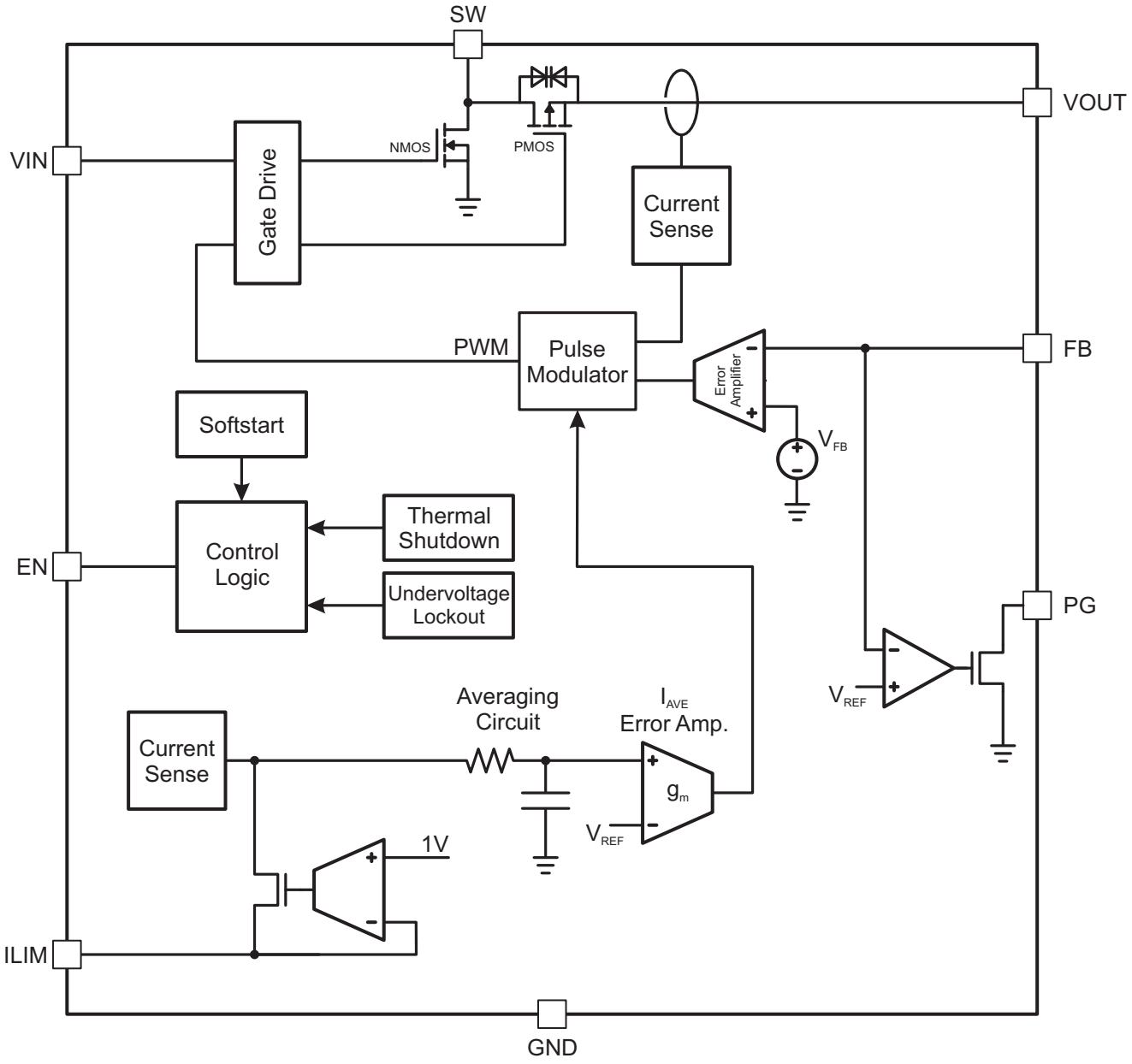
Figure 6. Parameter Measurement Schematic

10 Detailed Description

10.1 Overview

The TPS61252 device provides a power supply solution for products powered by either a three-cell alkaline, NiCd or NiMH battery, or an one-cell Li-Ion or Li-polymer battery. It has a resistor programmable (RILIM) input current limit. During light loads the device will automatically enter skip mode (PFM). During shutdown, the load is completely disconnected from the battery.

10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 Operation

The TPS61252 boost converter operates as a quasi-constant frequency adaptive on-time controller. In a typical application, the frequency is 3.25 MHz and is defined by the input to output voltage ratio and does not vary from moderate to heavy load currents. At light load currents, the converter automatically enters Power Save Mode and operates in PFM (Pulse Frequency Modulation) mode. During pulse-width-modulation (PWM) operation, the converter uses a unique fast response quasi-constant on-time valley current mode controller scheme which offers very good line and load regulation allowing the use of small ceramic input and output capacitors.

Based on the V_{IN}/V_{OUT} ratio, a simple circuit predicts the required on-time. At the beginning of the switching cycle, the low-side N-MOS switch is turned-on and the inductor current ramps up to a peak current that is defined by the on-time and the inductance. In the second phase, once the on-timer has expired, the rectifier is turned-on and the inductor current decays to a preset valley current threshold. Finally, the switching cycle repeats by setting the on-timer again and activating the low-side N-MOS switch.

The TPS61252 controls the input current through an intelligent adjustment of a valley current limit that corrects the value in a way that it almost turns out as an average input current limit. The current can be adjusted with an accuracy of ±20%.

This architecture with adaptive slope compensation provides excellent transient load response and requires minimal output filtering. Internal softstart and loop compensation simplifies the design process, while minimizing the number of external components.

10.3.2 Current Limit Operation

The current limit circuit employs a valley current sensing scheme. Current limit detection occurs during the off time, through sensing of the voltage drop across the synchronous rectifier.

The output voltage is reduced when the power stage of the device operates in a constant current mode. The maximum continuous output current ($I_{OUT(CL)}$), before entering current limit (CL) operation, can be defined by Equation 1.

$$I_{OUT(CL)} = (1 - D) \cdot \left(I_{LIM} + \frac{1}{2} \Delta I_L\right) \quad (1)$$

The duty cycle (D) can be estimated by Equation 2:

$$D = 1 - \frac{V_{IN} \cdot \eta}{V_{OUT}} \quad (2)$$

and the peak-to-peak current ripple (ΔI_L) is calculated by Equation 3:

$$\Delta I_L = \frac{V_{IN} \cdot D}{L \cdot f} \quad (3)$$

The output current, $I_{OUT(LIM)}$, is the average of the rectifier current waveform. When the load current is increased such that the lower peak is above the current limit threshold, the off-time is increased to allow the current to decrease to this threshold before the next on-time begins. When the current limit is reached, the output voltage decreases if the load is further increased.

10.3.3 Softstart

The TPS61252 has an internal softstart circuit that controls the ramp-up of the current during start-up and prevents the converter from inrush current that exceeds the set current limit. The current is ramped to the set current limit in typical 100 µs . After reaching the current limit threshold, it stays there until $V_{IN} = V_{OUT}$ then the converter starts switching and boosting up the voltage to its nominal output voltage. During the complete start-up, the input current does not exceed the current limit that is set by resistor R_{ILIM}.

10.3.4 Enable

The device is enabled by setting the EN pin to a voltage above 1 V. At first, the internal reference is activated and the internal analog circuits are settled. After typically 50 µs, the output voltage ramps up, controlled by the softstart circuitry. The output voltage reaches its nominal value as fast as the current limit settings and the load condition allows it.

Feature Description (continued)

The EN input can be used to control power sequencing in a system with several DC-DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and get a sequencing of supply rails. With EN = GND, the device enters shutdown mode. Do not leave the enable pin floating.

10.3.5 Under-Voltage Lockout (UVLO)

The under voltage lockout circuit prevents the device from malfunctioning at low input voltages and the battery from excessive discharge. It disables the output stage of the converter once the falling V_{IN} trips the under-voltage lockout threshold V_{UVLO} which is typically 2.0V. The device starts operation again once the rising V_{IN} trips the V_{UVLO} threshold plus its hysteresis of typically 100 mV.

10.3.6 Power Good

The device has a built in power good function to indicate whether the output voltage operates within appropriate levels. The PG pin is an open drain output, requiring a pull-up resistor. If the PG pin is not used, it may be left floating or connected to GND. The power good output (PG) is set floating after the FB pin voltage reaches 95% of its nominal value and stays there until the feedback voltage falls below 90 % of the nominal value. The power good is operable as long as the converter is enabled and V_{IN} is present. If the converter is disabled by pulling the EN pin low the PG open drain output is high impedance. That means it follows the voltage it is connected to via the pull-up resistor. If the converter is controlled by an external enable signal and the power good should indicate that the output is turned off the application circuit below should be used. In the following circuit, the EN pin voltage provides the high level for the PG pin pull-up resistor R4.

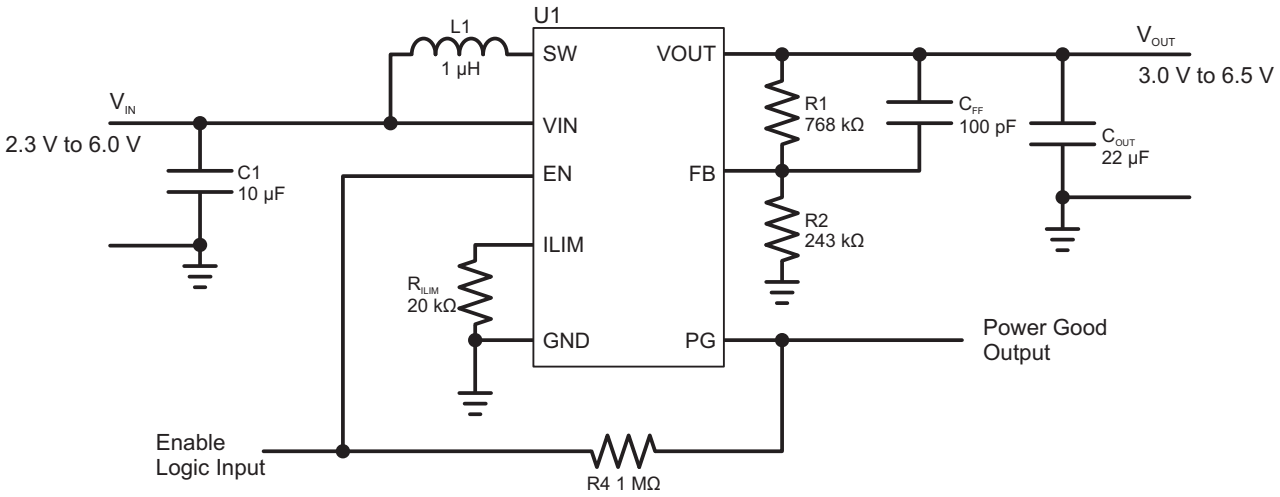


Figure 7. Power Good Schematic

10.3.7 Input Over Voltage Protection

This converter has input over voltage protection that protects the device from damage due to a voltage higher than the absolute maximum rating on the V_{IN} pin. If 6.5 V (typical) at the input is exceeded, the converter completely shuts down to protect its inner circuitry. If the input voltage drops below 6.4 V (typical), it turns on the device again and enters normal start up.

10.3.8 Load Disconnect and Reverse Current Protection

Regular boost converters do not disconnect the load from the input supply and therefore a connected battery is discharged during shutdown. The advantage of the TPS61252 is that this converter disconnects the output from the input of the power supply when it is disabled. In case of a connected battery, it prevents it from being discharged during shutdown of the converter. Furthermore, the output is not allowed to pass current to the input (battery).

Feature Description (continued)

10.3.9 Thermal Regulation

The TPS61252 contains a thermal regulation loop that monitors the die temperature. If the die temperature rises to values above 110 °C, the device automatically reduces the current limit to prevent the die temperature from further increasing. Once the die temperature drops about 10 °C below the threshold, the device automatically increases the current to the set value. This function also reduces the current during a short-circuit-condition.

10.3.10 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 140°C (typical), the device enters thermal shutdown. In this mode, the High Side and Low Side MOSFETs are turned-off. When the junction temperature falls about 20 °C below the thermal shutdown, the device resumes operation.

10.4 Device Functional Modes

10.4.1 Power Save Mode

The TPS61252 integrates a power save mode to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses and goes into power save mode again once the output voltage exceeds the set threshold voltage. During the power save operation when the output voltage is above the set threshold, the converter turns off some of the inner circuits to save energy.

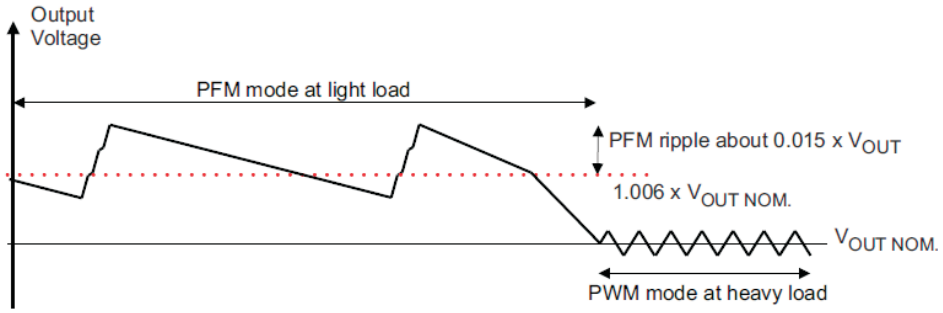


Figure 8. Power Save Mode

The PFM mode is left and PWM mode entered, in case the output current can no longer be supported in PFM mode.

10.4.2 100% Duty-Cycle Mode

If $V_{IN} > V_{OUT}$, the TPS61252 offers the lowest possible input-to-output voltage difference while still maintaining current limit operation with the use of the 100% duty-cycle mode. In this mode, the high-side switch is constantly turned on. During this operation, the output voltage follows the input voltage and will not fall below the programmed value if the input voltage decreases below V_{OUT}. The output voltage drop during 100% mode depends on the load current and input voltage, and is calculated as:

$$V_{OUT} = V_{IN} - \left(DCR + r_{DS(on)}\right) \bullet I_{OUT} \quad (4)$$

where

- DCR is the DC resistance of the inductor
- $r_{DS(on)}$ is the typical on-resistance of the high-side switch

If the load current exceeds the set current limit, the resistance of the high-side switch increases to limit the current and the output voltage drops.

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The TPS61252 device provides a power supply solution for products powered by either a three-cell alkaline, NiCd or NiMH battery, or an one-cell Li-Ion or Li-polymer battery. The wide input voltage range is ideal to power portable applications like mobile phones or for computer peripherals. TPS61252 allows the use of small inductors and input capacitors to achieve a small solution size. The possibility to reduce the current limit by a external resistor offers the potential use of physically even smaller inductors with lower rated current to further reduce total solution sizes of the power supply.

11.2 Typical Application

Typical application for 5-V output voltage with input current limit.

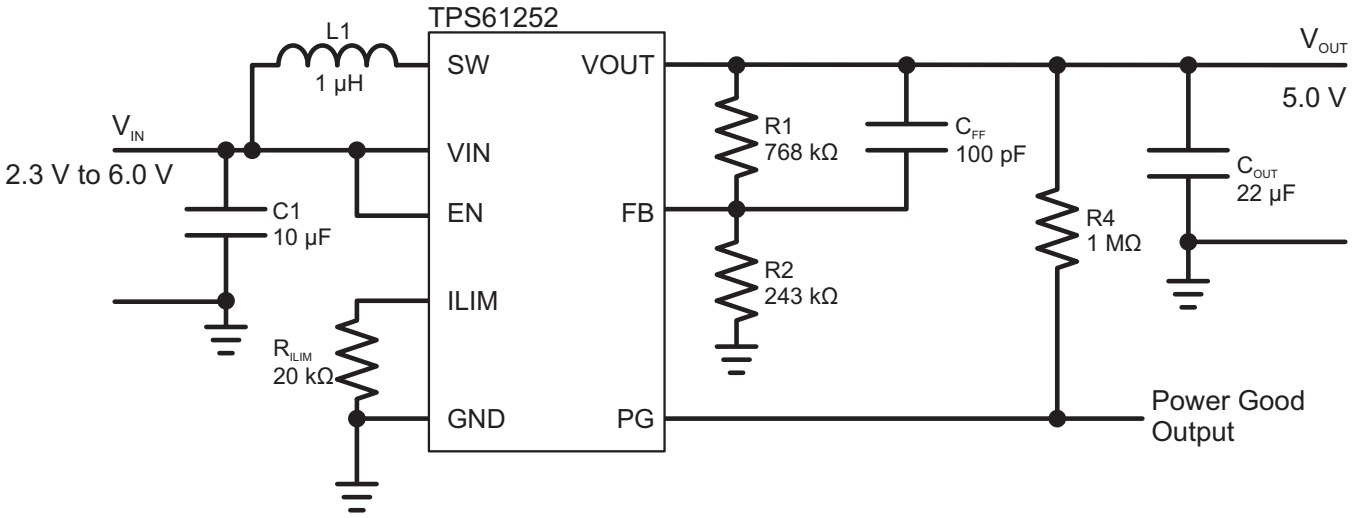


Figure 9. Typical Application Circuit for 5-V Output Voltage

11.2.1 Design Requirements

In this example, use the TPS61252 to design a 5-V output power supply supporting customer required input current limit, input voltage range and output driving capability. Below specific example will be used to define and work with the different equations.

Table 2. Design Parameters

PARAMETER		VALUE	UNIT
V_{IN}	Input Voltage	3.6	V
$V_{IN(min)}$	Minimum Input Voltage	2.6	V
V_{OUT}	Output Voltage	5.0	V
I_{LIM}	Input Current Limit set by R_{ILIM}	1000	mA
V_{FB}	Feedback Voltage	1.2	V
f	Switching Frequency	3.25	MHz
η	Estimated Efficiency	90	%
L1	Inductor Value of Choice	1.0	µH

11.2.2 Detailed Design Procedure

Table 3. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
U1	TPS61252	Texas Instruments
L1	1.0 µH, 2.1 A, 27 mΩ, 2.8 mm x 2.8 mm x 1.5 mm	DEM2815C, TOKO
C1	1 x 4.7 µF, 10 V, 0805, X7R ceramic	GRM21BR71A475KA73, Murata
C2	1 x 100 pF, 50 V, 0603, COG ceramic	GRM1885C1H101JA01B, Murata
C3	2 × 22 µF, 10 V, 0805, X7R ceramic	GRM21BR61A226ME51, Murata
R1	Depending on the output voltage of TPS61252, 1%, (all measurements with 5 V output voltage uses 768 kΩ)	
R2	Depending on the output voltage of TPS61252, 1%, (all measurements with 5 V output voltage uses 243 kΩ)	
R3	Depending on the input current limit of TPS61252, 1%	
R4	1 MΩ, 1%	any

11.2.2.1 Output Voltage Setting

The output voltage is calculated by Equation 5:

$$V_{OUT} = V_{FB} \cdot \left(1 + \frac{R_1}{R_2}\right) \quad (5)$$

To minimize the current through the feedback divider network, R2 should be between 180 kΩ and 360 kΩ. The sum of R1 and R2 should not exceed ~1 MΩ, to keep the network robust against noise. For the example, R1 is 768 kΩ and R2 is 243 kΩ.

An external feed forward capacitor C1 is required for optimum load transient response. The value of C1 should be 100 pF. The connection from the FB pin to the resistor divider should be kept short and away from noise sources, such as the inductor or the SW line.

11.2.2.2 Input Current Limit

The input current limit is set by selecting the correct external resistor value. Equation 6 is a guideline for selecting the correct resistor value:

$$R_{ILIM} = \frac{1.0V}{I_{LIM}} \cdot 10{,}000 \quad (6)$$

For a current limit of 1 A, the resistor value is 10 kΩ.

To allow maximum current limit the ILIM pin can be directly connected to V_{IN}.

11.2.2.3 Maximum Output Current

The maximum output current is set by R_{ILIM} and the input to output voltage ratio and can be calculated by Equation 7:

$$I_{OUT(max)} \approx I_{LIM} \bullet \frac{V_{IN} \bullet \eta}{V_{OUT}} \quad (7)$$

Following the example $I_{OUT(max)}$ is 648 mA at 3.6 V input voltage and decreases, with lower input voltage values.

11.2.2.4 Inductor Selection

As for all switching power supplies two main passive components are required for storing the energy during operation: an inductor and an output capacitor. The inductor must be connected between the VIN pin and SW pin to make sure that the TPS61252 device operates. To select the right inductor current rating, the programmed input current limit as well as the current ripple through the inductor should be calculated. An estimation of the maximum peak inductor current can be done using Equation 8.

$$I_{L(max)} = I_{LIM} + \Delta I_L = I_{LIM} + \frac{V_{IN(min)} \bullet D}{L \bullet f} \quad \text{with} \quad D = 1 - \frac{V_{IN(min)} \bullet \eta}{V_{OUT}} \quad (8)$$

Regarding the above example the current ripple (ΔI_L) is 426 mA and therefore an inductor with a rated current of about 1.5 A should be used.

The TPS61252 is designed to work with inductor values between 1.0 µH and 2.2 µH. For typical applications, a 1.5 µH inductor is recommended. In space constrained applications, it might be possible to consider smaller inductor values depending on the targeted inductor ripple current. Therefore the inductor value can be reduced down to 1.0 µH without degrading the stability.

In regular boost converter designs the current through the inductor is defined by the fixed switch current limit of the converter's switches and therefore bigger inductors have to be chosen. The TPS61252 allows the design engineer to reduce the current limit to the needs of the application regardless the maximum switch current limit of the converter. Programming a lower current value allows the use of smaller inductors without the danger of saturation.

11.2.2.5 Output Capacitor

For the output capacitor, it is recommended to use small X5R or X7R ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which cannot be placed close to the IC, a smaller ceramic capacitor in parallel to the large one is required. This small capacitor should be placed as close as possible to the converter's VOUT and GND pins.

To maintain control loop stability of the boost converter, a minimum effective output capacitance of at least 8 µF is recommended. That means due to DC Bias effect (see NOTE) a 22 µF capacitor with 0805 case size and a voltage rating of 10 V is necessary. In height restricted application two 10 µF capacitors with 0603 case size and 6.3 V voltage rating can also be used.

In addition to the minimum C_{OUT} the application might need more capacitance. To get an estimate of the minimum output capacitance necessary for the application, Equation 9 is used:

$$C_{MIN} = \frac{I_{OUT} \bullet (V_{OUT} - V_{IN})}{f \bullet \Delta V \bullet V_{OUT}} \quad (9)$$

Where ΔV is the maximum allowed output ripple.

With a chosen ripple voltage of 10 mV, a minimum effective capacitance of 9.6 µF is needed regarding the example. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 10:

$$V_{ESR} = I_{OUT} \bullet R_{ESR} \quad (10)$$

11.2.2.6 Input Capacitor

Multilayer X5R or X7R ceramic capacitors are an excellent choice for input decoupling of the step-up converter as they have extremely low ESR and are available in small form factors. The input capacitors should be located as close as possible to the device. While a 10µF input capacitor is sufficient for most applications, larger values may be used to reduce input current ripple. Also, low ESR tantalum capacitors may be used.

NOTE

DC Bias effect: High capacitance ceramic capacitors have a DC Bias effect, which has a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen very carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance. A 10 V rated 0805 capacitor with 10 µF can have a effective capacitance of less than 5 µF at an output voltage of 5 V.

11.2.2.7 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switch node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As the next step in the evaluation of the regulation loop, the load transient response is tested. During the time between when the load transient takes place and the turn on of the high side switch, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of C_{OUT}. $\Delta I_{(LOAD)}$ begins to charge or discharge C_{OUT}, generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 60° of phase margin. Because the damping factor of the circuitry is directly related to several resistive parameters (for example, MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

11.2.3 Application Curves

	FIGURE
Load transient response (V_{IN} = 3.6 V, V_{OUT} = 5.0V, I_{LIM} = 500mA, Load change from 20 mA to 300 mA)	Figure 10
Load transient response (V_{IN} = 3.6 V, V_{OUT} = 5.0V, V_{IN} > V_{OUT}, I_{LIM} = 1000mA, Load change from 50 mA to 550 mA)	Figure 11
Startup after enable (V_{OUT} = 5.0 V, V_{IN} = 3.6 V, I_{LIM} = 500mA)	Figure 12
Startup after enable (V_{OUT} = 5.0 V, V_{IN} = 3.6 V, I_{LIM} = 1000mA)	Figure 13
Startup after enable in 500 mA load (V_{OUT} = 5.0 V, V_{IN} = 3.6 V, I_{LIM} = 1000mA)	Figure 14

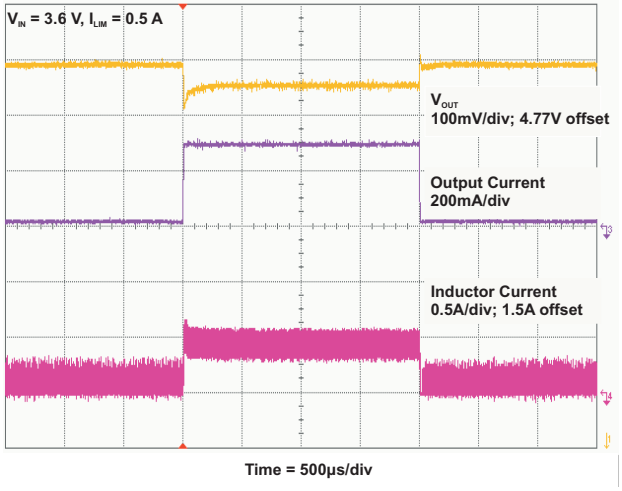


Figure 10. Load Transient Response I_{LIM} = 500 mA (20 to 300 mA)

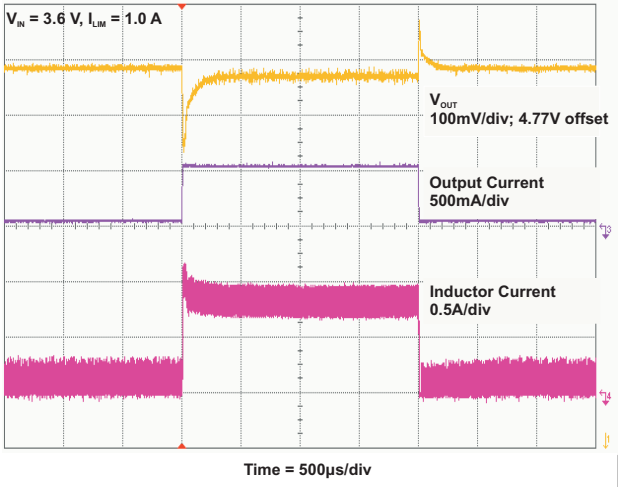


Figure 11. Load Transient Response I_{LIM} = 1000 mA (50 to 550 mA)

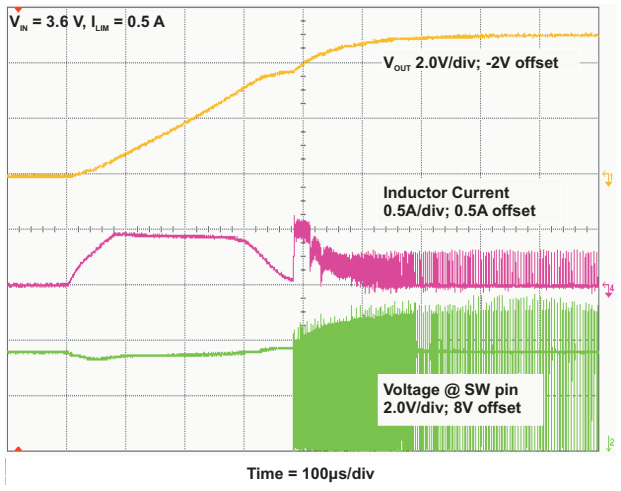


Figure 12. Startup After Enable I_{LIM} = 500mA, No Load

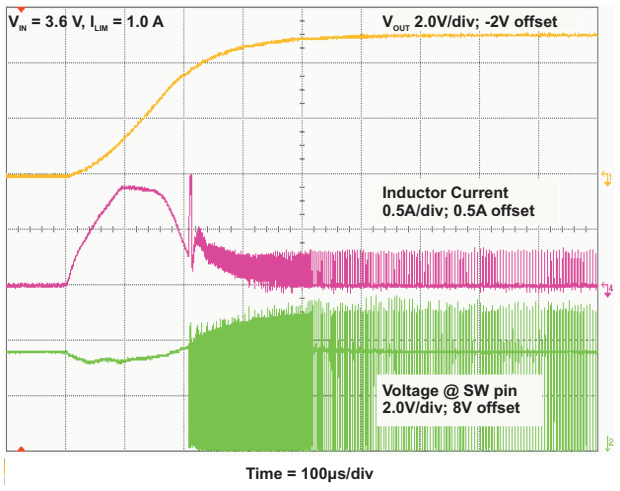


Figure 13. Startup After Enable I_{LIM} = 1000mA, NO Load

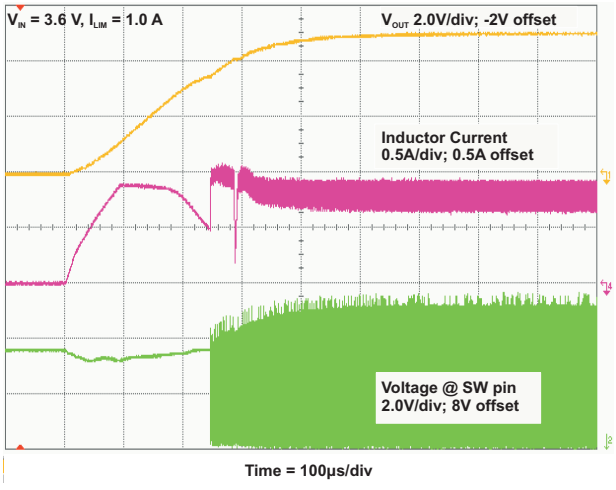


Figure 14. Startup After Enable I_{LIM} = 1000mA, 500 mA Load

12 Power Supply Recommendations

The power supply can be a three-cell alkaline, NiCd or NiMH battery, or an one-cell Li-Ion or Li-polymer battery. The input supply should be well regulated with the rating of TPS61252. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

13 Layout

13.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed close to the IC to keep the feedback connection short. To lay out the ground, short and wide traces are recommended. This avoids ground shift problems, which can occur due to superimposition of power ground current onto the feedback divider. Figure 15 shows the recommended board layout.

13.2 Layout Example

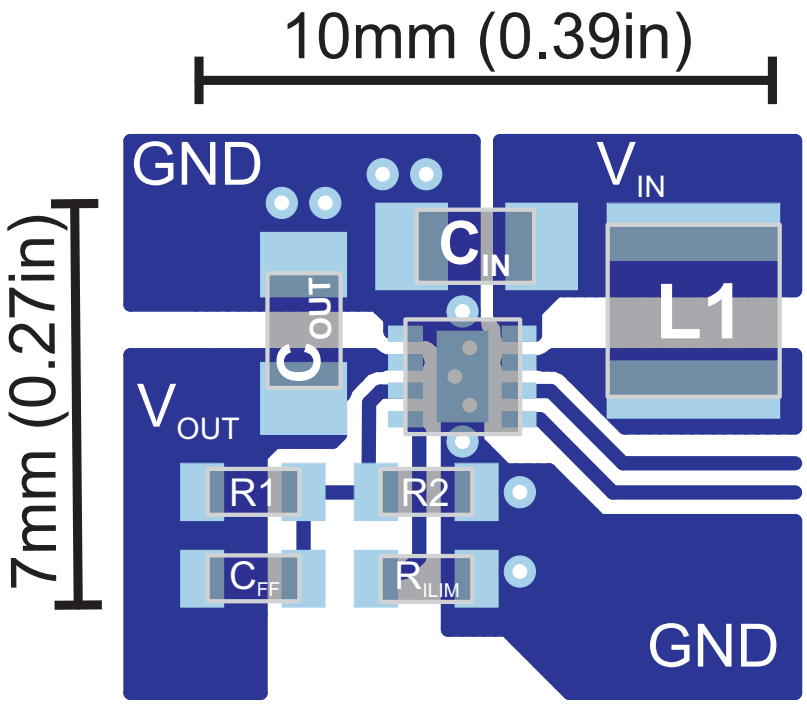


Figure 15. Suggested Layout

13.3 Thermal Considerations

The implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
  - For example, increase of the GND plane on the top layer which is connected to the exposed thermal pad
  - Use thicker copper layer
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. The maximum junction temperature (T_J) of the TPS61252 is 150°C.

14 Device and Documentation Support

14.1 Device Support

14.1.1 Third-Party Products Disclaimer

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14.2 Trademarks

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14.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61252DGST	PREVIEW	WSON	DSG	8		TBD	Call TI	Call TI	-40 to 85		
TPS61252DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QTI	Samples
TPS61252DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		QTI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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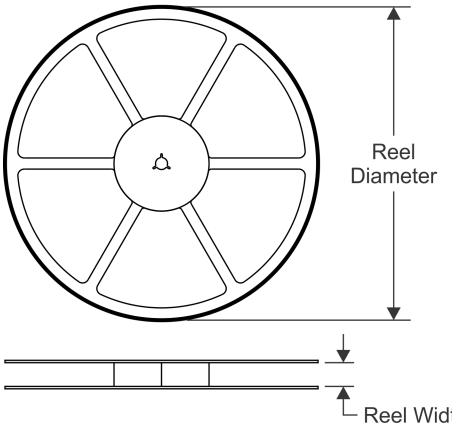
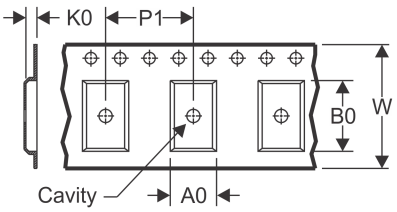
TAPE AND REEL INFORMATION

REEL DIMENSIONS

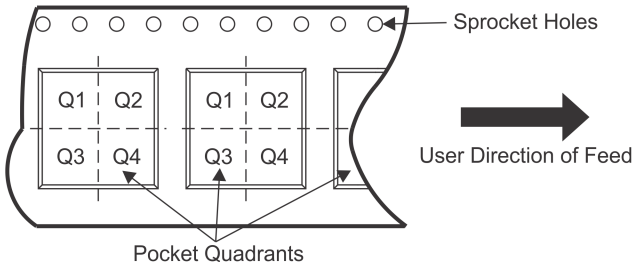


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

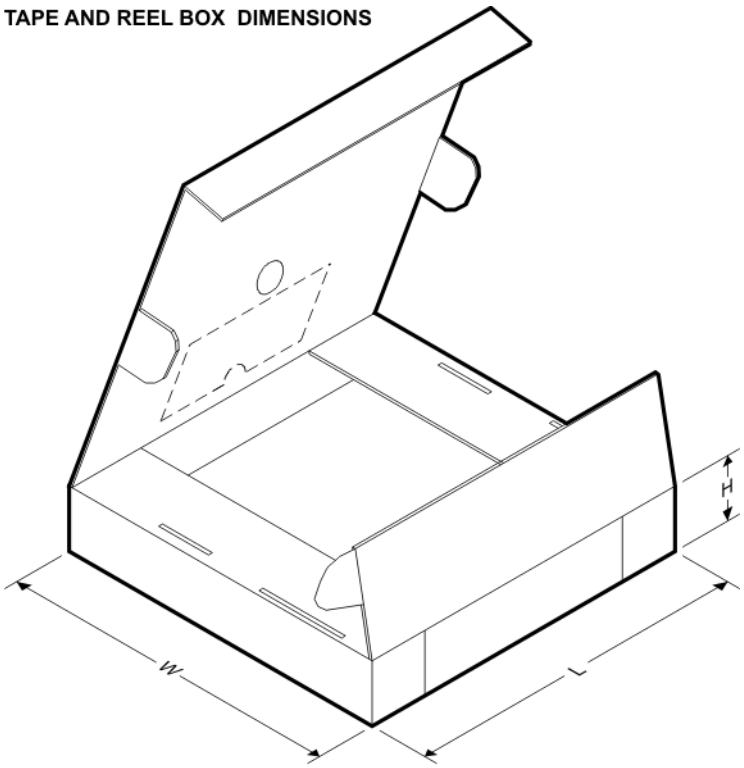
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61252DSGR	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS61252DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

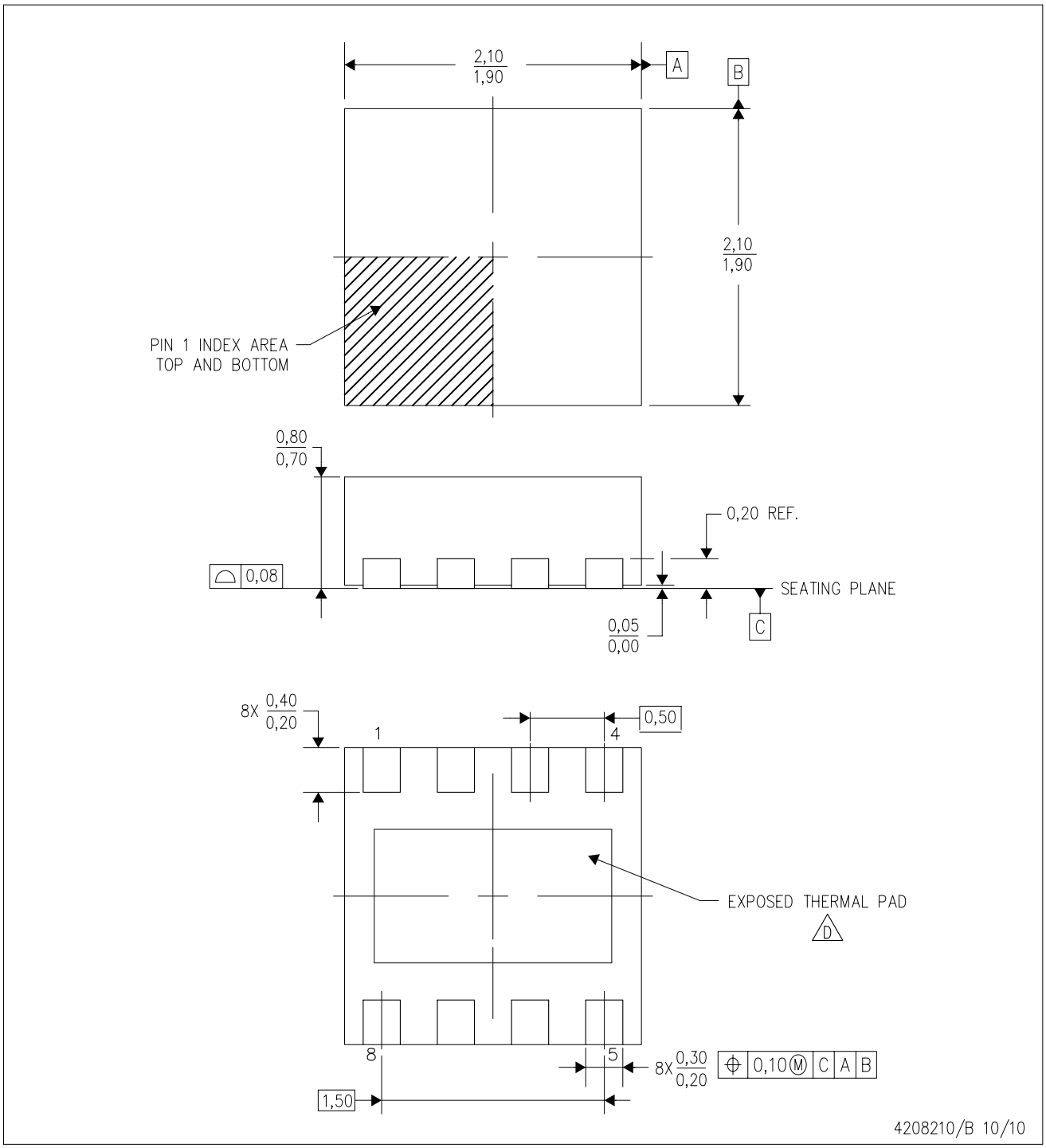
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61252DSGR	WSON	DSG	8	3000	195.0	200.0	45.0
TPS61252DSGT	WSON	DSG	8	250	195.0	200.0	45.0

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

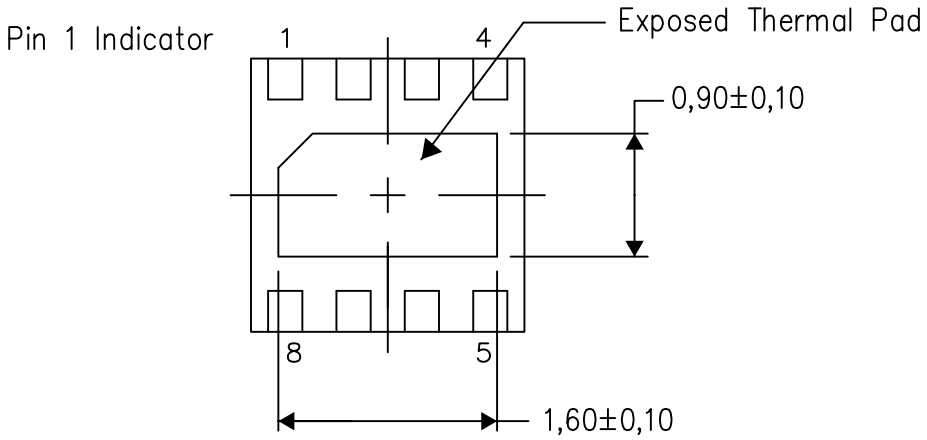
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



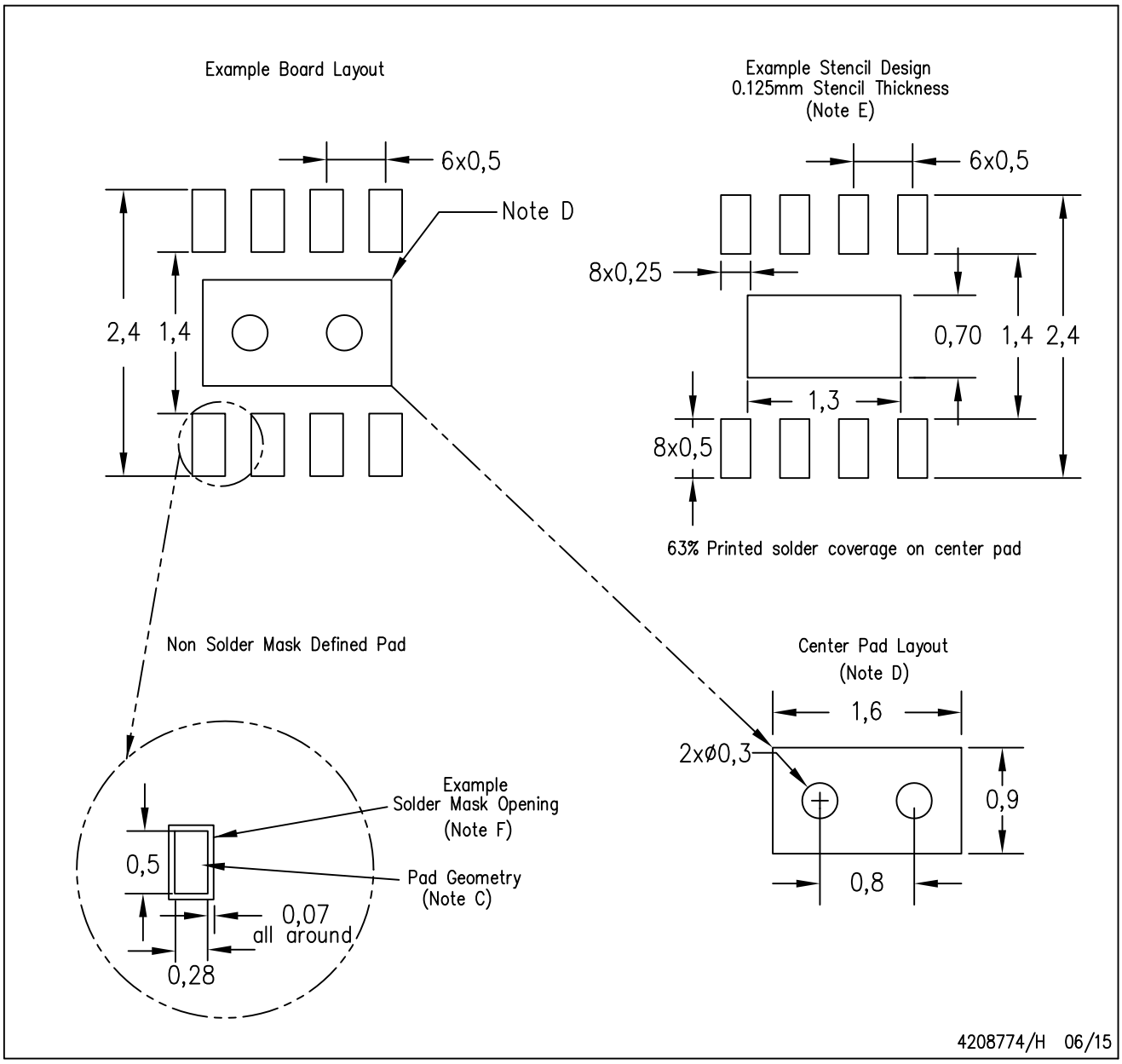
Bottom View

Exposed Thermal Pad Dimensions

4208347/I 06/15

NOTE: All linear dimensions are in millimeters

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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