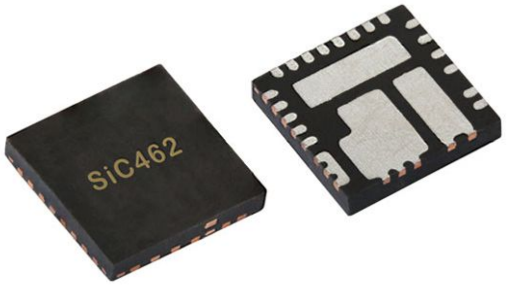
4.5 V to 60 V Input, 6 A Synchronous Buck Regulator



DESCRIPTION

The SiC462 is a wide input voltage high efficiency synchronous buck regulator with integrated high-side and low-side power MOSFETs. Its power stage is capable of supplying 6 A continuous current at up to 2 MHz switching frequency. This regulator produces an adjustable output voltage down to 0.8 V from 4.5 V to 60 V input rail to accommodate a variety of applications, including computing, consumer electronics, telecom, and industrial.

SiC462's architecture delivers ultra-fast transient response with minimum output capacitance and tight ripple regulation at very light load. The device is stable with any capacitor and no external ESR network is required for loop stability. The device also incorporates a power saving scheme that significantly increases light load efficiency.

The regulators integrates a full protection feature set, including over current protection (OCP), output overvoltage protection (OVP), short circuit protection (SCP), output undervoltage protection (UVP) and thermal shutdown (OTP). It also has UVLO for input rail and a user programmable soft start.

The SiC462 is available in lead (Pb)-free power enhanced MLP55-27L package.

FEATURES

- Single supply operation from 4.5 V to 60 V input voltage
- Adjustable output voltage down to 0.8 V
- 6 A continuous output current
- Adjustable switching frequency from 100 kHz to 2 MHz
- Adjustable current limit and soft start
- 98 % peak efficiency
- Ultra-fast transient response
- ± 1 % output voltage accuracy
- Normal, ultrasonic or pulse skipping operation
- 5 μA shutdown current
- 250 μA operating current
- Cycle-by-cycle current limit
- Output overvoltage protection
- Output undervoltage / short circuit protection
- Output voltage tracking and sequencing
- Scalable family of output current:
  3 A (SiC463), 6 A (SiC462), 10 A (SiC461)

APPLICATIONS

- POLs for telecom
- Industrial and automation
- Industrial computing
- Consumer electronics

TYPICAL APPLICATION CIRCUIT AND PACKAGE OPTIONS

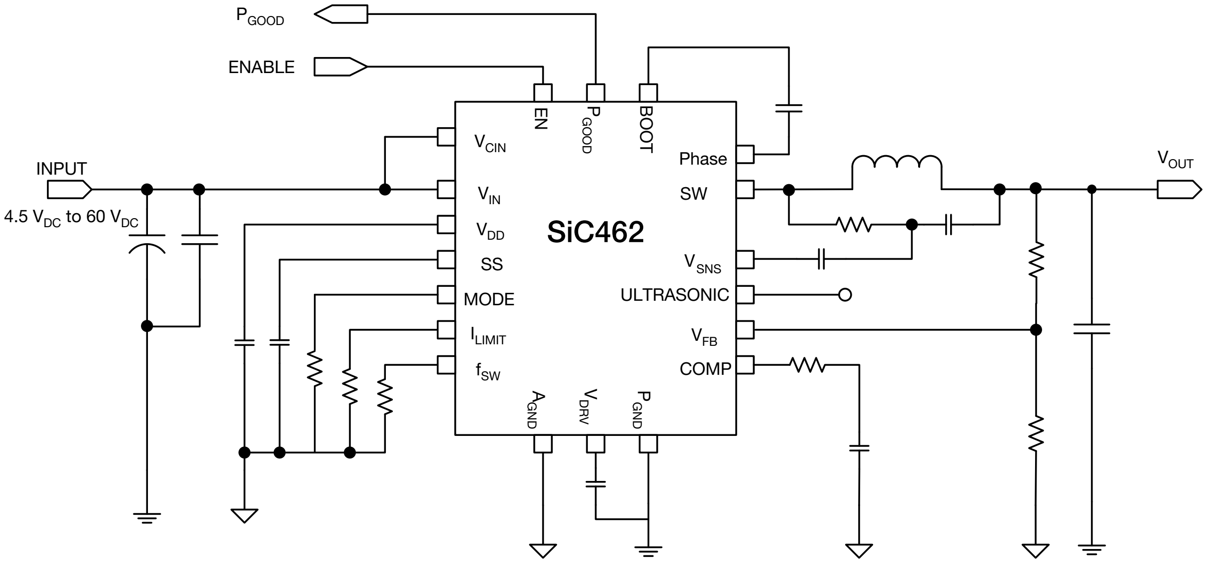


Fig. 1 - Typical Application Circuit for SiC462

PIN CONFIGURATION

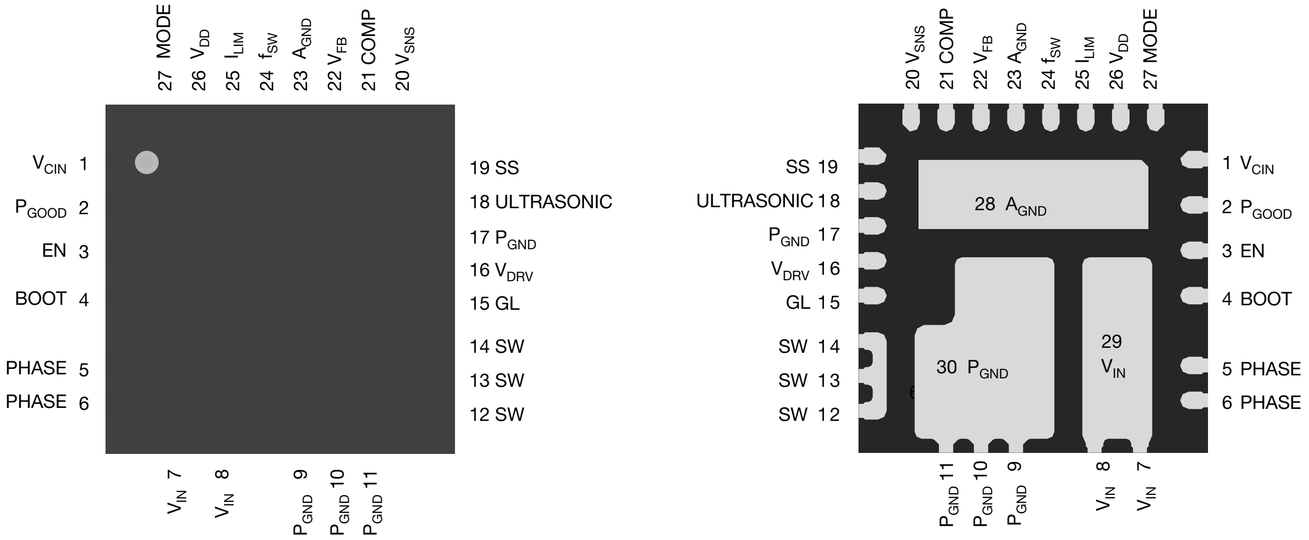


Fig. 2 - SiC462 Pin Configuration

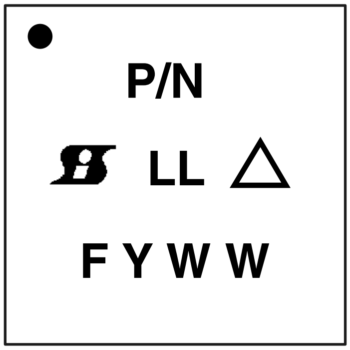
PIN DESCRIPTION

PIN NUMBER	SYMBOL	DESCRIPTION
1	V_{CIN}	Supply voltage for internal regulators V_{DD} and V_{DRV}. This pin should be tied to V_{IN}, but can also be connected to a lower supply voltage (> 5 V) to reduce losses in the internal linear regulators
2	P_{GOOD}	Open-drain power good indicator - high impedance indicates power is good. An external pull-up resistor is required
3	EN	Enable pin
4	BOOT	High-side driver bootstrap voltage
5, 6	PHASE	Return path of high-side gate driver
7, 8, 29	V_{IN}	Power stage input voltage. Drain of high-side MOSFET
9, 10, 11, 17, 30	P_{GND}	Power ground
12, 13, 14	SW	Power stage switch node
15	GL	Low-side MOSFET gate signal
16	V_{DRV}	Supply voltage for internal gate driver. When using the internal LDO as a bias power supply, V_{DRV} is the LDO output. Connect a 4.7 μF decoupling capacitor to P_{GND}
18	ULTRASONIC	Float to disable ultrasonic mode, connect to V_{DD} to enable. Depending on the operation mode set by the MODE pin, power save mode or forced continuous mode will be enabled when the ultrasonic mode is disabled
19	SS	Set the soft start ramp by connecting a capacitor to A_{GND}. An internal current source will charge the capacitor
20	V_{SNS}	Power inductor signal feedback pin for system stability compensation
21	COMP	Output of the internal error amplifier. The feedback loop compensation network is connected from this pin to the V_{FB} pin
22	V_{FB}	Feedback input for switching regulator used to program the output voltage - connect to an external resistor divider from V_{OUT} to A_{GND}
23, 28	A_{GND}	Analog ground
24	f_{SW}	Set the on-time by connecting a resistor to A_{GND}
25	I_{LIMIT}	Set the current limit by connecting a resistor to A_{GND}
26	V_{DD}	Bias supply for the IC. V_{DD} is an LDO output, connect a 1 μF decoupling capacitor to A_{GND}
27	MODE	Set various operation modes by connecting a resistor to A_{GND}. See specification table for details

ORDERING INFORMATION

PART NUMBER	PACKAGE	MARKING CODE
SiC462ED-T1-GE3	PowerPAK® MLP55-27L	SiC462
SiC462EVB	Reference board	

PART MARKING INFORMATION



● = pin 1 indicator
P/N = part number code
= Siliconix logo
△ = ESD symbol
F = assembly factory code
Y = year code
WW = week code
LL = lot code

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

ELECTRICAL PARAMETER	CONDITIONS	LIMITS	UNIT
EN, V_{CIN}, V_{IN}	Reference to P_{GND}	-0.3 to +63	V
SW / PHASE	Reference to P_{GND}	-0.3 to +66	
V_{DRV}	Reference to P_{GND}	-0.3 to +6	
V_{DD}	Reference to A_{GND}	-0.3 to +6	
SW / PHASE (AC)	100 ns	-4 to +72	
BOOT		-0.3 to V_{PHASE} + V_{DRV}	
A_{GND} to P_{GND}		-0.3 to +0.3	
All other pins	Reference to A_{GND}	-0.3 to V_{DD} + 0.3	
Temperature			
Junction temperature	T_J	-40 to +150	°C
Storage temperature	T_{STG}	-65 to +150	
Power Dissipation			
Thermal resistance from junction to ambient		12	°C/W
Thermal resistance from junction to case		2	
ESD Protection			
Electrostatic discharge protection	Human body model, JESD22-A114	2000	V
	Charged device model, JESD22-A101	750	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (all voltages referenced to GND = 0 V)

PARAMETER	MIN.	TYP.	MAX.	UNIT
Input voltage (V_{IN})	4.5	-	60	V
Control input voltage (V_{CIN}) (1)	4.5	-	60	
Enable (EN)	0	-	60	
Bias supply (V_{DD})	4.75	5	5.25	
Drive supply voltage (V_{DRV})	4.75	5.3	5.5	
Output voltage (V_{OUT})	0.8	-	0.8 x V_{IN}	
Temperature				
Recommended ambient temperature	-40 to +105			°C
Operating junction temperature	-40 to +125			

Note

(1) For input voltages below 5 V, provide a separate supply to V_{CIN} of at least 5 V to prevent the internal V_{DD} rail UVLO from triggering.

ELECTRICAL SPECIFICATIONS ($V_{IN} = V_{CIN}$ = 48 V, T_J = -40 °C to +125 °C, unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power Supplies						
V_{DD} supply	V_{DD}	$V_{IN} = V_{CIN}$ = 6 V to 60 V, V_{EN} = 5 V, not switching	-	5	-	V
		$V_{IN} = V_{CIN}$ = 5 V, V_{EN} = 5 V, not switching	-	4.96	-	
V_{DD} dropout	$V_{DD\_DROPOUT}$	$V_{IN} = V_{CIN}$ = 5 V, I_{VDD} = 1 mA	-	60	-	mV
V_{DD} UVLO threshold	V_{DD_UVLO}		-	4.25	-	V
V_{DD} UVLO hysteresis	$V_{DD\_UVLO\_HYST}$		-	250	-	mV
Maximum V_{DD} current	I_{DD}	$V_{IN} = V_{CIN}$ = 6 V to 60 V	3	-	-	mA
V_{DRV} supply	V_{DRV}	$V_{IN} = V_{CIN}$ = 6 V to 60 V, V_{EN} = 5 V, not switching	-	5.3	-	V
		$V_{IN} = V_{CIN}$ = 5 V, V_{EN} = 5 V, not switching	-	5	-	
V_{DRV} dropout	$V_{DRV\_DROPOUT}$	$V_{IN} = V_{CIN}$ = 5 V, I_{VDD} = 10 mA	-	160	-	mV
Maximum V_{DRV} current	I_{DRV}	$V_{IN} = V_{CIN}$ = 6 V to 60 V	50	-	-	mA
V_{DRV} UVLO threshold	V_{DRV_UVLO}		-	4.25	-	V
V_{DRV} UVLO hysteresis	$V_{DRV\_UVLO\_HYST}$		-	275	-	mV
Input current	IV_{CIN}	Non-switching, V_{FB} > 0.8 V	-	245	-	µA
Shutdown current	IV_{CIN_SHDN}	V_{EN} = 0 V	-	5	10	
Controller and Timing						
Feedback voltage	V_{FB}	T_J = 25 °C	796	800	804	m/V
		T_J = -40 °C to +125 °C $^{(1)}$	792	800	808	
V_{FB} input bias current	I_{FB}		-	2	-	nA
Transconductance	g_m		-	0.3	-	mS
COMP source current	I_{COMP_SOURCE}		-	20	-	µA
COMP sink current	I_{COMP_SINK}		-	20	-	
Minimum on-time	$t_{ON\_MIN.}$		-	100	-	ns
t_{ON} accuracy	$t_{ON\_ACCURACY}$		-	10	-	%
On-time range	t_{ON_RANGE}		100	-	8000	ns
Frequency range	f_{kHz}	Ultrasonic mode enabled	20	-	2000	kHz
		Ultrasonic mode disabled	-	-	2000	
Minimum off-time	$t_{OFF\_MIN.}$		-	250	-	ns
Soft start current	I_{SS}		-	5	-	µA
Soft start voltage	V_{SS}	When V_{OUT} reaches regulation	-	1.5	-	V
Power MOSFETs						
High-side on resistance	R_{ON_HS}	V_{GS} = 5.3 V	-	25	-	mΩ
Low-side on resistance	R_{ON_LS}		-	11	-	
Fault Protections						
Current limit accuracy	$I_{LIM\_ACCURACY}$	1 % resistor used for R_{LIM}	-20	-	20	%
Output OVP threshold	OVP	V_{FB} with respect to 0.8 V reference	-	20	-	
Output UVP threshold	UVP		-	-80	-	
Over temperature protection	OTP_R	Rising temperature	-	150	-	°C
	OTP_{HYST}	Hysteresis	-	35	-	

ELECTRICAL SPECIFICATIONS (V_{IN} = V_{CIN} = 48 V, T_J = -40 °C to +125 °C, unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power Good						
Power good output threshold	$V_{FB\_RISING\_VTH\_OV}$	V_{FB} rising above 0.8 V reference	-	20	-	%
	$V_{FB\_FALLING\_VTH\_UV}$	V_{FB} falling below 0.8 V reference	-	-10	-	
Power good hysteresis	P_{GOOD_HYST}		-	55	-	mV
Power good on resistance	R_{ON_PGOOD}		-	8	-	Ω
Power good delay time	t_{DLY_PGOOD}		-	25	-	μs
EN / MODE / Ultrasonic Threshold						
EN logic high level	V_{EN_H}		1.4	-	-	V
EN logic low level	V_{EN_L}		-	-	0.4	
EN pull down resistance	R_{EN}		-	5	-	MΩ
Ultrasonic mode high Level	U_{HIGH}		2	-	-	V
Ultrasonic mode low level	U_{LOW}		-	-	0.8	
Mode pull up current	I_{MODE}		-	5	-	μA
MODE1		Power save mode enabled, V_{DD}, V_{DRV} Pre-reg on	0	-	0.7	V
MODE2		Power save mode disabled, V_{DD}, V_{DRV} Pre-reg on	1.3	-	1.7	
MODE3		Power save mode disabled, V_{DRV} Pre-reg off, V_{DD} Pre-reg on, provide external V_{DRV}	2.3	-	2.7	
MODE4		Power save mode enabled, V_{DRV} Pre-reg off, V_{DD} Pre-reg on, provide external V_{DRV}	3.3	-	V_{DD}	

Note

(1) Guaranteed by design

FUNCTIONAL BLOCK DIAGRAM

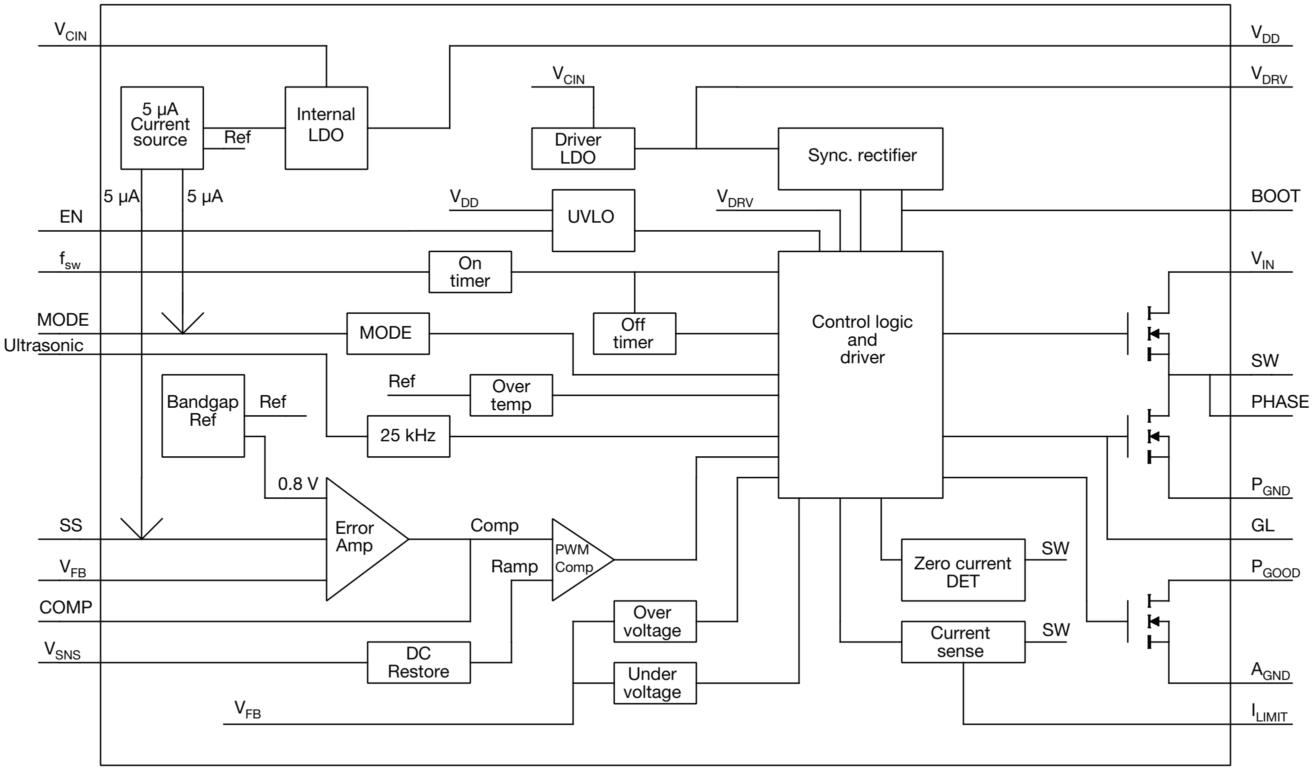


Fig. 3 - SiC462 Functional Block Diagram

OPERATIONAL DESCRIPTION

Device Overview

SiC462 is a high-efficiency synchronous buck regulator capable of delivering up to 6 A continuous current. The device has programmable switching frequency of 100 kHz to 2 MHz. The control scheme is based on voltage mode constant on time. It delivers fast transient response and minimizes external components. It also enables loop stability regardless of the type of output capacitor used, including low-ESR ceramic capacitors. This device also incorporates a power saving feature by enabling diode emulation mode and frequency fold back as the load decreases.

SiC462 has a full set of protection and monitoring features:

- Over current protection in pulse-by-pulse mode
- Output overvoltage protection
- Output undervoltage protection with device latch
- Over temperature protection with hysteresis
- Dedicated enable pin for easy power sequencing
- Power good open drain output
- This device is available in MLP55-27L package to deliver high power density and minimize PCB area.

Power Stage

SiC462 integrates a high-performance power stage with a 25 mΩ n-channel high side MOSFET and a 11 mΩ n-channel low side MOSFET. The MOSFETs are optimized to achieve up to 98 % efficiency.

The power input voltage (V_{IN}) can go up to 60 V and down as low as 4.5 V for power conversion.

Control Scheme

SiC462 employs a voltage - mode COT control mechanism in conjunction with adaptive zero current detection which allows precise power saving feature. The switching frequency, f_{SW}, is set by an external resistor to A_{GND}, R_{fsw}.

$$R_{fsw} = \frac{V_{OUT}}{f_{sw} \times 190 \times 10^{-12}}$$

Note, that there is no V_{IN} dependency on f_{SW} as the on time adjusts as V_{IN} is varied. During steady-state operation, V_{COMP} is generated from the feedback voltage and internal 0.8 V reference inputs to the error amplifier. An internally generated ramp signal and V_{COMP} are fed into a comparator. Once V_{RAMP} crosses V_{COMP}, a single shot ON-time pulse is generated for a fixed time, programmed by the external R_{FSW}. During the On-time pulse, the high side MOSFET will be turned ON. Once the ON-time pulse expires, the high side MOSFET is turned off and the low side MOSFET will be turned ON after a break-before-make period. The low side MOSFET will be on for duration of minimum OFF-time pulse until V_{RAMP} crosses V_{COMP}. The cycle is then repeated.

Fig. 4 illustrates the basic block diagram for voltage mode constant on time architecture with external ripple injection.

- The reference of a basic voltage mode COT regulator is replaced with a high gain error amplifier loop. This loop ensures the DC component of the output voltage follows the internal accurate reference voltage provides excellent regulation
- A second voltage feedback path via the V_{SNS} with a ripple injection scheme ensures rapid correction of the transient perturbation
- This establishes two parallel voltage regulating feedback paths, a ripple injection path, and a steady accurate dc reference path

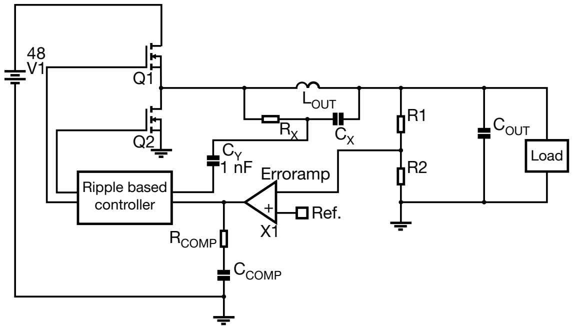


Fig. 4 - SiC462 Control Block Diagram

For stability purposes the SiC462 requires 200 mV of ripple injection. C_X, C_Y, and R_X are selected to achieve the desired ripple injection.

Typically C_y is chosen to be ≥ 2 nF to meet the internal impedance of the V_{SNS} pin.

C_X is chosen to be 10 times greater than C_Y, $C_X = 10 \times C_Y$.

$$R_X = (V_{IN} - V_{OUT}) \times (V_{OUT}/(V_{IN} \times f_{SW} \times C_X \times V_{RIPPLE}))$$

Fig. 5 demonstrates the basic operational waveforms:

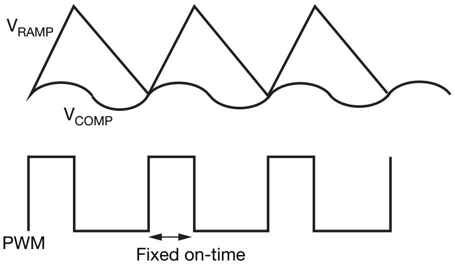


Fig. 5 - SiC462 Operational Principle

Typically, the frequency of R_{COMP} and C_{COMP} is chosen to be around the resonance frequency of L_{OUT} and C_{OUT}.

In this case, set

$$R_{COMP} \times C_{COMP} = \sqrt{L_{OUT} \times C_{OUT}}$$

For good slew rate / transient load response, pick $C_{COMP} \leq 1$ nF, R_{COMP} can be calculated according the formula above.

Power-Save Mode, MODE Pin, and Ultrasonic Pin Operation

To improve efficiency at light-loads, SiC462 provides a set of innovative implementations to eliminate LS re-circulating current and switching losses. The internal zero crossing detector (ZCD) monitors SW node voltage to determine when inductor current starts to flow negatively. In power saving mode, as soon as inductor valley current crosses zero, the device first deploys diode emulation mode by turning off the LS FET. If load further decreases, switching frequency is reduced proportional to the load condition to save switching losses while keeping output ripple within tolerance. If the ultrasonic pin is tied to V_{DD}, the minimum switching frequency in the discontinuous mode is 25 kHz to avoid switching frequencies in the audible range. If this feature is not required this ultrasonic mode can be disabled by floating the ultrasonic pin. When the ultrasonic mode is disabled, the regulator will either operate in forced continuous mode or in a power save mode where there is no limit to the lower frequency limit. In this state, at zero load switching frequency can go as low as hundreds of Hz.

To improve the converter efficiency, the user can choose to disable the internal V_{DRV} regulator by picking either Mode 3 or Mode 4 and connecting a 5 V supply to the V_{DRV} pin. This reduces power dissipation in the SiC462 by eliminating the V_{DRV} linear regulator losses.

The MODE pin supports several modes of operation as shown in table 1. An internal current source is used to set the voltage on this pin using an external resistor:

TABLE 1 - OPERATION MODES

MODE	RANGE (V)	POWER SAVE MODE	INTERNAL V_{DRV} REGULATOR
1	0 to 0.7	Enabled	ON
2	1.3 to 1.7	Disabled	ON
3	2.3 to 2.7	Disabled	OFF (1)
4	3.3 to V_{DD}	Enabled	OFF (1)

Note

(1) Connect a 5 V (± 5 %) supply to the V_{DRV} pin

The mode pin is not latched to any state and can be changed on the fly.

OUTPUT MONITORING AND PROTECTION FEATURES

Output Over-Current Protection (OCP)

SiC462 has cycle by cycle current limiting. The inductor valley current is monitored during LS FET turn-on period through $R_{DS(on)}$ sensing. After a pre-defined blanking time, the valley current is compared with an internal threshold. If monitored current is higher than threshold, HS turn-on pulse is skipped and LS FET is kept on until the valley current returns below OCP limit.

In a short circuit or a severe over-current condition, output undervoltage protection (UVP) will result in both the HS and LS FET turning off. See output undervoltage protection (UVP) section for more details.

OCP is enabled immediately after V_{CC} passes UVLO level.

OCP is set by an external resistor to A_{GND}, R_{LIM}.

$$R_{LIM} = 480k / I_{OUT\ max.}$$

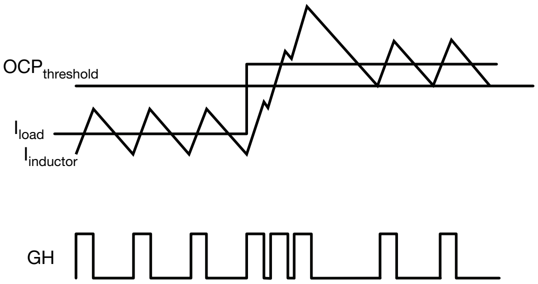


Fig. 6 - Over-Current Protection Illustration

Output Undervoltage Protection (UVP)

UVP is implemented by monitoring output through V_{FB} pin. If the voltage level at V_{FB} goes below 0.16 V (V_{OUT} is 20 % of V_{OUT} set point) for more than 25 μs a UVP event is recognized and both HS and LS MOSFETs are turned off. After a time-out period equal to 20 soft start cycles, the IC attempts to re-start by going through a soft start cycle. If the fault condition still exists, the above cycle will be repeated.

UVP is only active after the completion of soft-start sequence.

Output Over-Voltage Protection (OVP)

For OVP implementation, output is monitored through FB pin. After soft start, if the voltage level at FB is above 0.96 V (typ.) (V_{OUT} is 120 % of V_{OUT} set point), OVP is triggered with both the HS and LS MOSFETs turned off. Normal operation is resumed once FB voltage drops back to 0.96 V.

OVP is active immediately after V_{CC} passes UVLO level.

Over-Temperature Protection (OTP)

SiC462 has internal thermal monitor block that turns off both HS and LS FETs when junction temperature is above 150 °C (typ). A hysteresis of 35 °C is implemented, so when junction temperature drops below 115 °C, the device restarts by initiating soft-start sequence again.

Sequencing of Input / Output Supplies

SiC462 has no sequencing requirements on any of its input / output (V_{IN}, V_{DRV}, V_{DD}, V_{CIN}, EN) supplies or enables.

Enable

The SiC462 has an enable pin to turn the part on and off. Driving this pin high enables the device, while grounding it turns it off.

The SiC462 enable has a weak pull down to prevent unwanted turn on due to a floating GPIO.

There are no sequencing requirements w.r.t other input / output supplies.

Soft-Start

SiC462 soft-start time is adjustable by selecting a capacitor value from the following equation. Once V_{CC} is above UVLO level (2.55 V typ.), V_{OUT} will ramp up slowly, rising monotonically to the programmed output voltage. There is an internal 5 μA current source tied to the soft start pin which charges the external soft start cap.

$$\text{SS time} = \frac{C_{ext} \times 0.8\ \text{V}}{5\ \mu\text{A}}$$

During soft-start period, OCP is activated. Short-circuit protection is not active until soft-start is complete.

Pre-Bias Start-Up

In case of pre-bias startup, output is monitored through FB pin. If the sensed voltage on FB is higher than the internal reference ramp value, control logic prevents HS and LS FET from switching to avoid negative output voltage spike and excessive current sinking through LS FET.

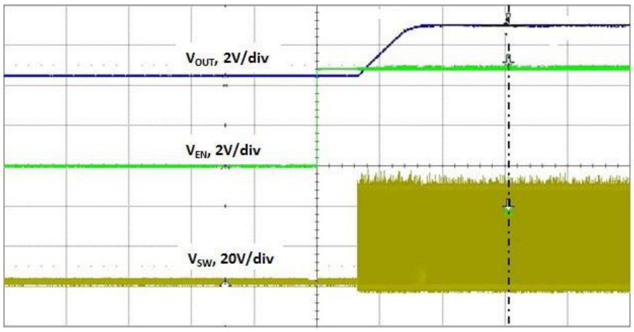


Fig. 7 - Pre-Bias Start-Up

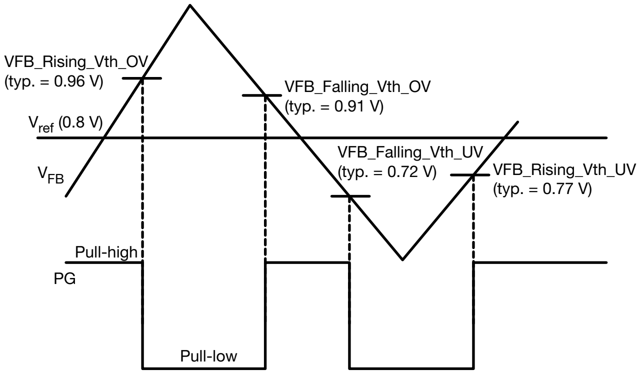
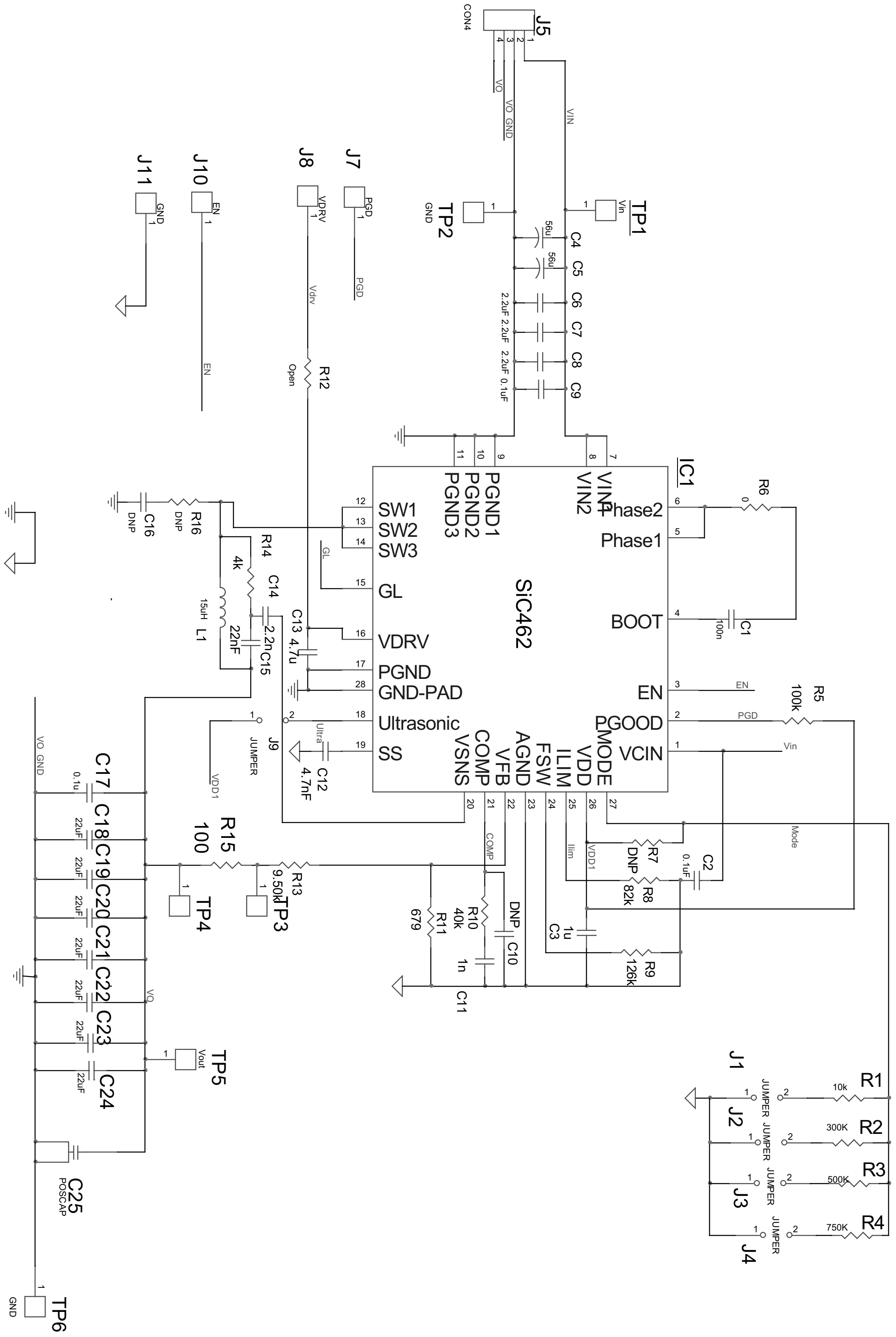


Fig. 8 - P_{GOOD} Window and Timing Diagram

Power Good

SiC462's power good is an open-drain output. Pull P_{GOOD} pin high up to 5 V through a 10K resistor to use this signal. Power good window is shown in the diagram above. If voltage level on FB pin is out of this window, PG signal is de-asserted by pulling down to GND. To prevent false triggering during transient events, P_{GOOD} has a 25 μs blanking time.

REFERENCE BOARD SCHEMATIC



BILL OF MATERIAL				
QTY	**REFERENCE DESIGNATOR**	**DESCRIPTION**	**PART NUMBER**	**MANUFACTURER**
1	C1	Capacitor ceramic 0.1 µF 100 V X5R 0402	GRM155R62A104ME14D	Murata Electronics
1	C3	Capacitor ceramic 1 µF 35 V X5R 0402	C1005X5R1V105M050BC	TDK Corporation
1	C10	DNP	-	-
1	C11	Capacitor ceramic 1000 pF 100 V X7R 0402	GRM155R72A102KA01D	Murata Electronics
1	C12	Capacitor ceramic 10000 pF 100 V X7S 0402	C1005X7S2A103K050BB	TDK Corporation
2	C2, C9	Capacitor ceramic 0.1 µF 100 V X7R 0603	GRM188R72A104KA35D	Murata Electronics
1	C15	Capacitor ceramic 0.022 µF 100 V X7R 0603	C0603C223K1RACTU	Kemet
1	C14	Capacitor ceramic 2200 pF 100 V X7R 0603	C0603C222K1RACTU	Kemet
1	C16	DNP	-	-
1	C17	Capacitor ceramic 0.1 µF 35 V X5R 0603	GMK107BJ104KAHT	Taiyo Yuden
1	C13	Capacitor ceramic 4.7 µF 35 V X5R 0805	GRM219R6YA475KA73D	Murata Electronics
3	C6, C7, C8	Capacitor ceramic 2.2 µF 100 V X7R 1210	HMK325B7225KN-T	Taiyo Yuden
7	C18, C19, C20, C21, C22, C23, C24	Capacitor ceramic 22 µF 25 V X5R 1210	GRM32ER61E226KE15L	Murata Electronics
1	J5	Terminal block 5.08 mm VERT 4POS	ED120/4DS	On Shore Technology Inc.
2	C4, C5 (1)	Capacitor aluminum 56 µF 20 % 100 V radial	UHE2A560MPD	Nichicon
1	L1	Inductor 10 µH	IHLP4040DZER100M11	Vishay
5	J1, J2, J3, J4, J9	B/S II HDR. SR	68000-402	Amphenol FCI
1	C25	DNP	-	-
1	R1	Resistor 10K 1 % 1/16 W 0402	RC0402FR-0710KL	Yageo
1	R2	Resistor 300K 1 % 1/16 W 0402	RC0402FR-07300KL	Yageo
1	R3	Resistor 499K 1 % 1/16 W 0402	RC0402FR-07499KL	Yageo
1	R4	Resistor 750K 1 % 1/16 W 0402	RC0402FR-07750KL	Yageo
2	R5, R7	Resistor 100K 1 % 1/16 W 0402	RC0402FR-07100KL	Yageo
1	R6	Resistor 0.0 Jumper 1/16 W 0402	RC0402JR-070RL	Yageo
1	R8	Resistor 48.7K 1 % 1/16 W 0402	RC0402FR-0748K7L	Yageo
1	R9	Resistor 210K 1 % 1/16 W 0402	RC0402FR-07210KL	Yageo
1	R10	Resistor 56K 5 % 1/16 W 0402	RC0402JR-0756KL	Yageo
1	R11	Resistor 10K 5 % 1/10 W 0603	RC0603FR-0710KL	Yageo
1	R12	-	-	-
1	R14	Resistor 6.8K 5 % 1/10 W 0603	RC0603JR-076K8L	Yageo
1	R13	Resistor 140K 1 % 1/10 W 0603	RC0603FR-07140KL	Yageo
1	R15	Resistor 100 1 % 1/10 W 0603	RC0603FR-07100RL	Yageo
1	R16	DNP	-	-
1	IC1	IC SiC462	SiC462	Vishay
10	J7, J8, J10, J11, TP, TP2, TP3, TP4, TP5, TP6	BERGSTIK II 0.100" SNGL ST	68002-401HLF	Amphenol FCI

Note

(1) These two large Aluminium Electrolytic caps are included in case the customers evaluation set up has long leads. They are not needed for SiC462 operation.

EXTERNAL COMPONENT SELECTION FOR THE SiC462

A reference design has been developed to illustrate how to choose component values for proper operation of the SiC462. The schematic for the demo board is shown in Fig. 9 and Table 2.

Demo Board Connection and Signal / Test Points

Power Sockets

V_{IN}, GND (P1): input voltage source with V_{IN} to be positive. Connect to a voltage source:

V_{OUT}, GND (P3): output voltage with V_{OUT} to be positive. Connect to a load that draws no more than:

5 V, GND (P10): external 5 V MOSFET gate voltage source with 5 V to be the positive input. Apply 5 V when Mode 3 or Mode 4 is selected.

Selection Jumpers

Mode Select

P7: this is an 8 way header which allows the user to select one of four modes of operation.

MODE1 - SHORT PIN 1 to 2 Power save, V_{DRV} and Pre-reg on

MODE2 - SHORT PIN 3 to 4 Forced PWM, V_{DRV} and Pre-reg on

MODE3 - SHORT PIN 5 to 6 Forced PWM, V_{DRV} and Pre-reg off - external 5 V supply

MODE4 - SHORT PIN 7 to 8 Power save, V_{DRV} and Pre-reg off - external 5 V supply

V_{DRV} External Supply

P10: this is a 2 way header that will enable the user to supply an external MOSFET gate driver supply if an external 5 V supply is available. This should only be used in MODES 3 and 4.

ENABLE

P9: this is a 2 way header that will enable the part if left open. When shorted the part is disabled.

OPEN Pin 1-2 - automatic enable on power up
SHORT Pin 1-2 - IC disabled.

Ultrasonic

P8: this is a 2 way header that will enable the user to select the ultrasonic mode of operation. In ultrasonic mode the minimum frequency of operation is 20 kHz, above the audible range. When not in ultrasonic mode the frequency can drop below 20 kHz.

OPEN Pin 1-2 - ultrasonic disabled
SHORT Pin 1-2 - ultrasonic enabled

SIGNALS AND TEST LEADS

Input Voltage Sense

V_{IN_SENSE}, GND_{IN_SENSE} (P2): this allows the user to measure the voltage at the input of the regulator and remove any losses generated due to the, connections from the measurement. This can also be used by a power source with sense capability.

Output Voltage Sense

V_{OUT_SENSE}, GND_{OUT_SENSE} (P4): this allows the user to measure the voltage at the output of the regulator and remove any losses generated due to the connections, from the measurement. This can also be used by an active load with sense capability.

POWER GOOD INDICATOR

P_{GOOD} (P11): is an open drain output and is pulled up with a 10 kΩ resistor to V_{IN}. When FB or V_{OUT} are within -10 % to +20 % of the set voltage this pin will go HI to indicate the output is okay.

POWER UP PROCEDURE

To turn-on the reference board, apply 12 V to V_{IN} with the P7 jumper is in position 1. If the P7 jumper is in place 1 the board will come up in power save mode, if in place 2 then constant PWM will be observed.
When applying higher than 12 V to the input it is reasonable to install a RC snubber from SW to GND if needed however this will affect efficiency. There are place holders on the reference board, R_{11} and C_{12} for the snubber. Values of 4 Ω and 1 nF are a reasonable starting point.

ADJUSTMENTS TO THE REFERENCE BOARD

OUTPUT VOLTAGE ADJUSTMENT

If a different output voltage is needed, simply change the value of V_{OUT} and solve for R_{12} based on the following formula:

$$R_{12} = \frac{R_{13}(V_{OUT} - V_{FB})}{V_{FB}}$$

Where V_{FB} is 0.8 V for the SiC46X. R_{BOTTOM} (R_{13}) should be a maximum of 10 kΩ to prevent V_{OUT} from drifting at no load.

CHANGING SWITCHING FREQUENCY

The following equation illustrates the relationship between on-time, V_{IN}, V_{OUT}, and R_{fsw} value:

$$R_{fsw} = R_7 = \frac{V_{OUT}}{f_{sw} \times 190 \times 10^{-12}}$$

OUTPUT RIPPLE VOLTAGE

There is no requirement for this converter to see output capacitor ripple voltage in the control loop as a voltage injection circuit is employed; the voltage injection ramp is used to alert the converter to the next switch event.

Output ripple voltage is measured with a tip and barrel measurement across C_{OUT}; the barrel of the probe is the GND / 0 V connection and this removes the effect of the long GND / 0 V leads of the probe. Typically output ripple voltage is set to 3 % to 5 % of the output voltage, but an all ceramic output solution can bring output ripple voltage to a much lower level since the ESR of ceramics can be in the range of mΩ's.

VOLTAGE INJECTION NETWORK

This is the network seen placed across the output inductor in the schematic consisting of R_{10}, C_{10} and C_{11}. A quick method to add or remove injection is to reduce or increase R_{10}.

The time constant of the voltage injection network is as follows:

$$\tau_{INJECTION} = R_X \times C_X$$

In order to set a correct magnitude, the SiC46x requires around 200 mV, the following equation is used:

$$R_X = (V_{IN} - V_{OUT}) \times \left(\frac{V_{OUT}}{V_{IN} \times f_{sw} \times C_X \times V_{INJECTION}}\right)$$

Where $V_{INJECTION}$ = 200 mV is the midpoint of the ripple injection RC circuit.

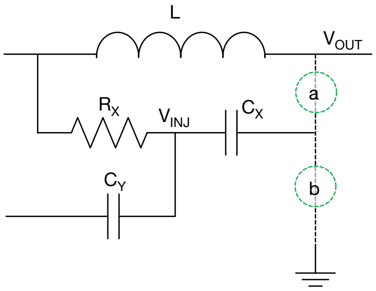


Fig. 9 - Voltage Injection Circuit

In fig. 9 the recommended value of $C_X = C_{10}$ (a or b) ≈ 22 nF and $C_Y = C_{11}$ ≈ 2.2 nF.

The reference design allows placement of C_X in two positions as shown in fig. 9, "a" and "b". The "b" option removes the output ripple and transient response voltage from the injection signal. The effect of connecting the C_X capacitor to GND / 0 V is the same as removing the output information from the fast loop. The output will be very stable in this setup when large transient loads are experienced at the output; in any case you will notice that the effective impedance of the output node is very small and the FB loop will react quickly enough for all loads. Another key aspect of using the GND / 0 V connection for the injection circuit is the ability to use a smaller output capacitance.

Be aware that the b) option is should only be used with forced PWM operation.

$$V_{INJECTION} = (V_{IN\_min.} - V_{OUT}) \times \left(1 - \frac{1}{e^{\frac{t}{\tau_{INJ}}}}\right)$$

Where t is the ON period. The required magnitude is ~ 100 mVpp for stable operation.

Compensation

The COT loop uses a transconductance amplifier to convert a proportional current from the output voltage, V_{FB}. This has the effect of offering a high impedance at the V_{FB} node, however this circuitry is left with a wide bandwidth to accommodate the different switching frequencies. This will require rolling off with an RC circuit, use the following equation:

$$R_{COMP} = \frac{\sqrt{L \times C_{OUT}}}{C_{COMP}}$$

C_{COMP} will be set to 1 nF. This provides a frequency breakpoint around the LC filter peak. It may be necessary to reduce the roll off further, this can be a choice of the designer but an example might be to start at 1/2 the LC filter peak frequency. This will affect the transient response time, something to note is the minimal phase delay in the COT topology and its fast response compared to PWM converters.

INDUCTOR SELECTION

The choice of inductor is specific to each application and quickly determined with the following equations:

$$t_{ON} = \frac{V_{OUT}}{V_{IN\_max.} \times f_{sw}}$$

and

$$L = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{I_{OUT\_MAX.} \times K}$$

Where K is a percentage of maximum output current ripple required. The designer can quickly make a choice of inductor if the ripple percentage is decided, usually no more than 30 % however higher or lower percentages of I_{OUT} can be acceptable depending on application. This device allows choices larger than 30 %.

Other than the inductance the DCR and saturation current parameters are key values. The DCR causes an I^2R loss which will decrease the system efficiency and generate heat. The saturation current has to be higher than the maximum output current plus ½ of the ripple current. In an over current condition the inductor current may be very high. All this needs to be considered when selecting the inductor.

On this board Vishay IHLP series inductors are used to meet cost requirement and high efficiency, a part that utilizes a material that has incredible saturation behaviour compared to competing products.

OUTPUT CAPACITOR SELECTION

Voltage rating, ESR, transient response, overall PCB area and cost are requirements for selecting output capacitors. The types of capacitors and there general advantages and disadvantages are covered next.

Electrolytic have high ESR, dry out over time so ripple current rating must be examined and have slower transient response, but are fairly inexpensive for the amount of overall capacitance.

Tantalums can come in low ESR varieties and high capacitance value for its overall size, but they fail short when damaged and also have slower transient response.

Ceramics have very low ESR, fast transient response and overall small size, but come in low capacitance values compared to the others types. A combination of technology is sensible, however these converters suit an ceramic solution also.

The output capacitance will be determined by the ripple voltage requirement. Voltage mode COT topology can work with very small values of capacitor ESR.

The following equations are used to calculate the size needed to meet a transient load response:

$$I_{LPK} = I_{max.} + 0.5 \text{ x } I_{RIPPLE\_max.}$$

and

$$C_{OUT\_min.} = I_{LPK} \text{ x } \frac{L \text{ x } \frac{I_{LPK}^2}{V_{OUT}} - \frac{I_{max}^2 \text{ x dt}}{dI_{LOAD}}}{2 \text{ x } (V_{PK} - V_{OUT})}$$

Where I_{LPK} is the peak inductor current, $I_{MAX.}$ is the maximum output current, dI_{LOAD} is the current step in µs and V_{PK} is the peak voltage, the output voltage summed with the specified over and under shoot.

The evaluation PCB is fitter with 66 µF.

ENABLE PIN VOLTAGE

The EN pin has an internal pull down resistor and only requires an enable voltage. This needs to be greater than 1.4 V. An input voltage or a resistor connected across V_{IN} and EN can be used. The internal pull down resistance is 5 MΩ.

SOFT START SETTING

Soft start is a useful function helping to limit the current magnitude from the source at switch on. This is simply set with a ceramic capacitor using the following equation:

$$t_{SS} = \frac{C_{SS} \text{ x } 0.8}{5 \text{ x } 10^{-6}}$$

A 100 nF capacitor will provide ~ 16 ms soft start time. V_{DD} pin will need to be decoupled in order to provide a stable voltage internally and externally. The value for this capacitor is recommended as ≥ 1 µF.

CURRENT LIMIT RESISTOR

The current limit is set by placing a resistor between I_{LIM} and A_{GND}. The values can be found using the following equation:

$$R_{LIM} = \frac{480\,000}{I_{OUT\_max.}}$$

INPUT CAPACITANCE

In order to keep the design compact and minimize parasitic elements, ceramic capacitors will be chosen. The initial requirement for the input capacitance is decided by the maximum input voltage, 60 V in this case however a 100 V rated capacitor will be chosen of the X7R variety. The footprint will be a compact 1206.

In order to determine the minimum capacitance the input voltage ripple needs to be specified; $V_{CINPP} \leq 500$ mV is a suitable starting point. This magnitude is determined by the final application specification. The input current needs to be determined for the lowest operating input voltage,

$$I_{CIN(RMS)} = I_O \text{ x } \sqrt{D \text{ x } (1 - D) + \frac{1}{12} \times \left(\frac{V_{OUT}}{L \times f_{sw} \times I_{OUT}}\right)^2 \times (1 - D)^2 \times D}$$

The minimum input capacitance can then be found,

$$C_{IN\_min.} = I_{OUT} \text{ x } \frac{D - (1 - D)}{V_{CINPKPK} \text{ x } f_{sw}}$$

For output voltage greater than 5 V the input capacitance should be increased accordingly. As the output power increases so does the input voltage ripple, the evaluation PCB has 4.4 µF.

Note

- If the input voltage becomes very small then extra capacitance needs adding to the input as the ripple will affect the duty cycle calculation when larger current is required.

ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz unless noted otherwise)

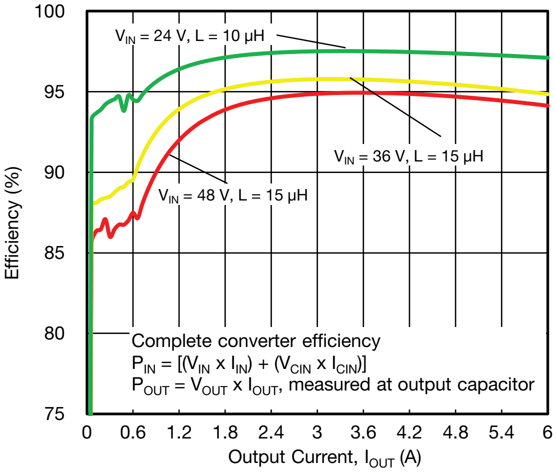


Fig. 10 - Efficiency vs. Output Current (V_{OUT} = 12 V, f_{sw} = 500 kHz)

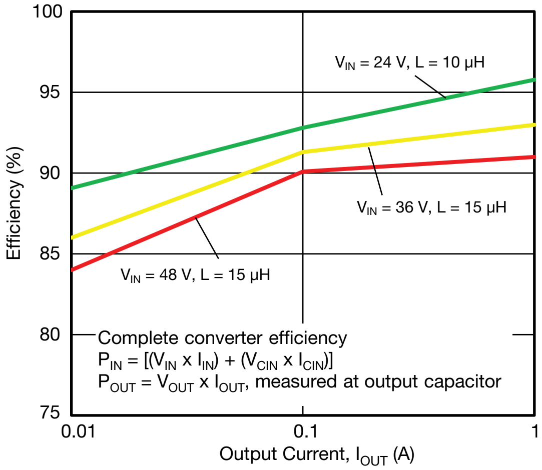


Fig. 13 - Efficiency vs. Output Current (V_{OUT} = 12 V, f_{sw} = 500 kHz)

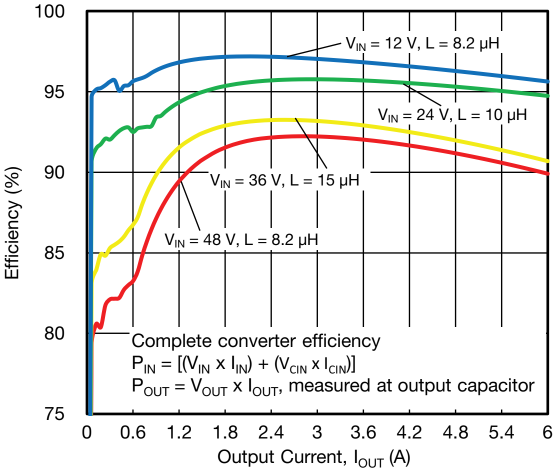


Fig. 11 - Efficiency vs. Output Current (V_{OUT} = 5 V, f_{sw} = 300 kHz)

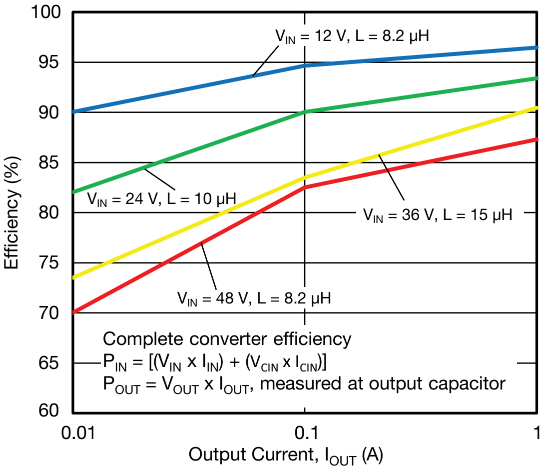


Fig. 14 - Efficiency vs. Output Current (V_{OUT} = 5 V, f_{sw} = 300 kHz)

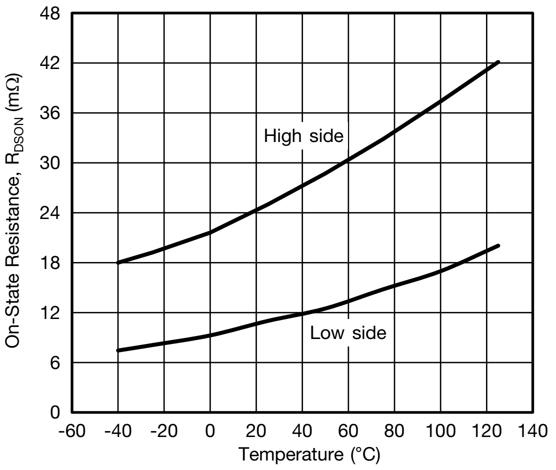


Fig. 12 - On Resistance vs. Junction Temperature

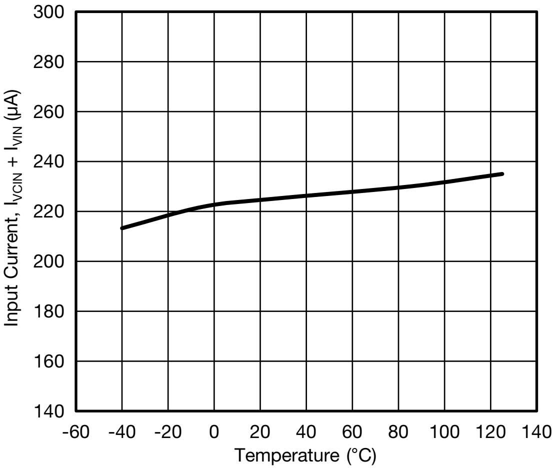


Fig. 15 - Input Current vs. Junction Temperature

ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz unless noted otherwise)

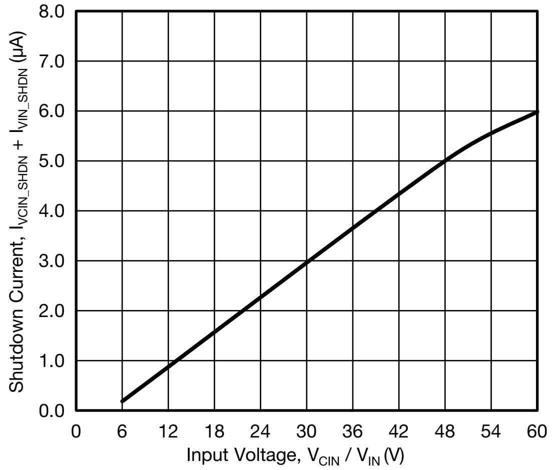


Fig. 16 - Shutdown Current vs. Input Voltage

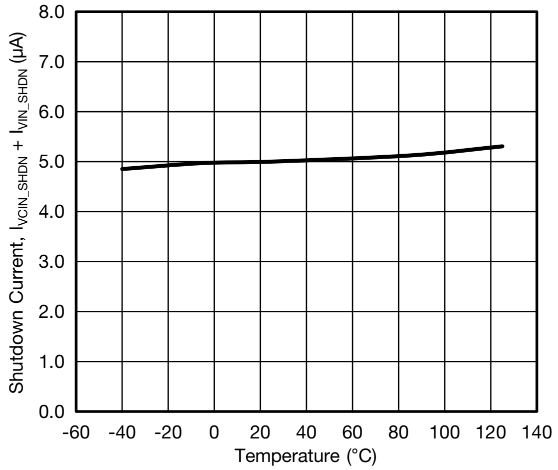


Fig. 19 - Shutdown Current vs. Junction Temperature

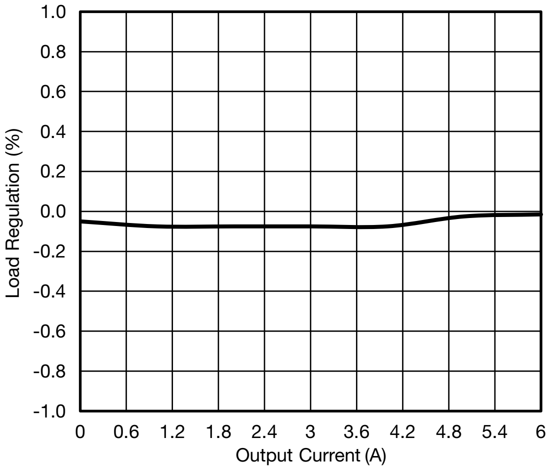


Fig. 17 - Load Regulation, V_{OUT} = 12 V

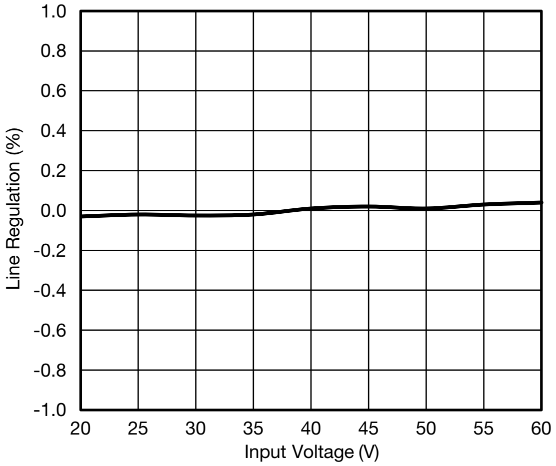


Fig. 20 - Line Regulation, V_{OUT} = 12 V

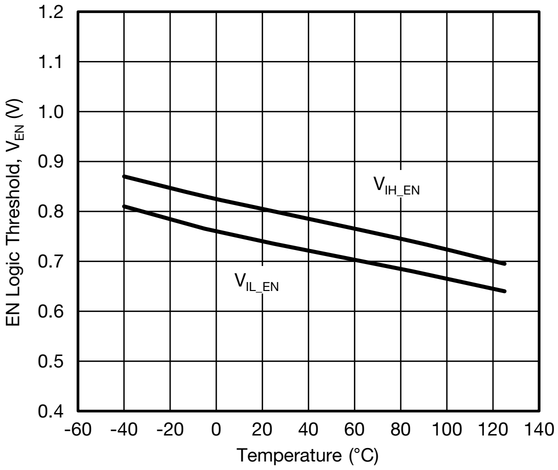


Fig. 18 - EN Logic Threshold vs. Junction Temperature

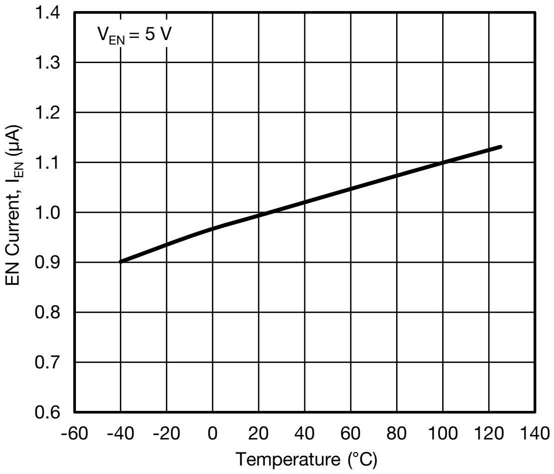


Fig. 21 - EN Current vs. Junction Temperature

ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz unless noted otherwise)

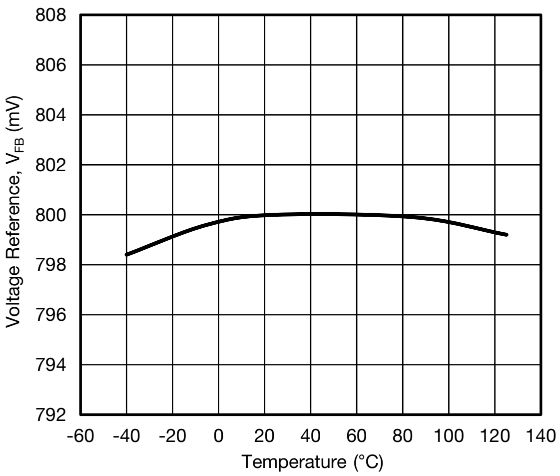


Fig. 22 - Voltage Reference vs. Junction Temperature

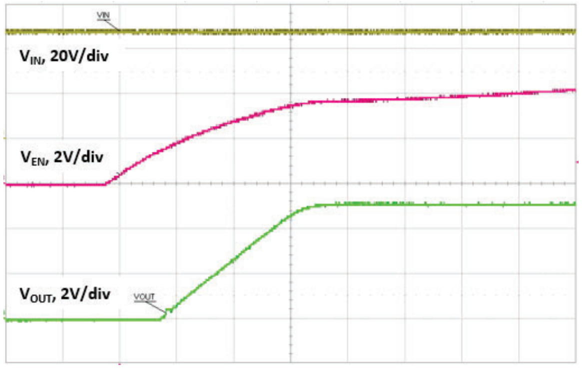


Fig. 23 - Start-Up with EN, Time = 1 ms/div

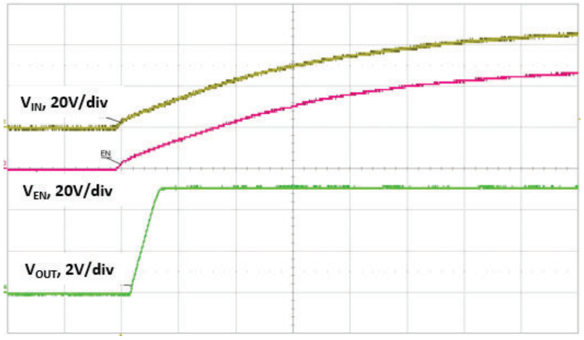


Fig. 24 - Start-Up with V_{IN}, Time = 5 ms/div

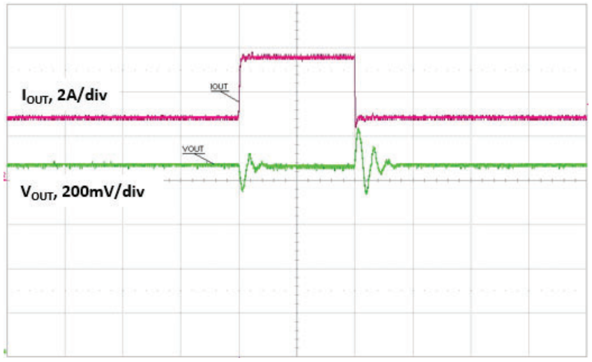


Fig. 25 - Load Transient (3 A to 6 A), (6 A to 3 A), Time = 100 µs/div

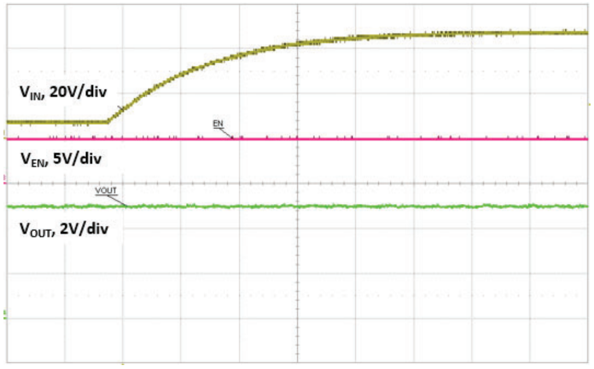


Fig. 26 - Line Transient (8 V to 48 V), Time = 10 ms/div

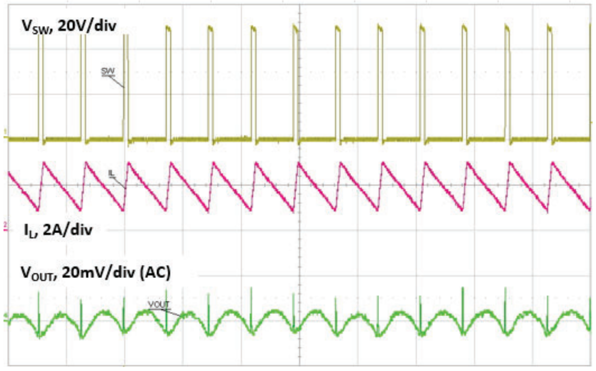


Fig. 27 - Output Ripple 2 A, Time = 5 µs/div

ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz unless noted otherwise)

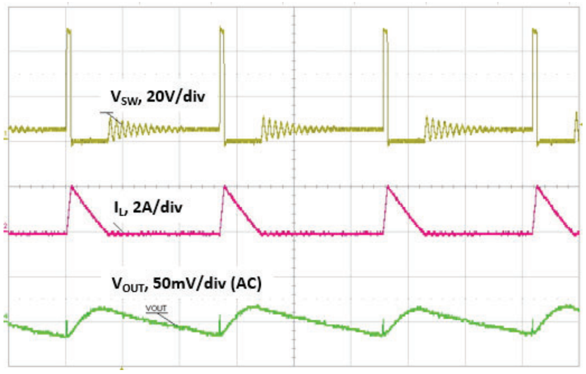


Fig. 28 - Output Ripple 300 mA, Time = 5 µs/div

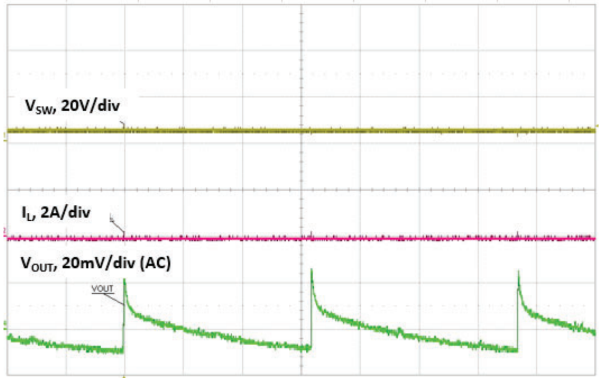


Fig. 29 - Output Ripple PSM, Time = 10 ms/div

PCB LAYOUT RECOMMENDATIONS

Step 1: V_{IN}/GND Planes and Decoupling

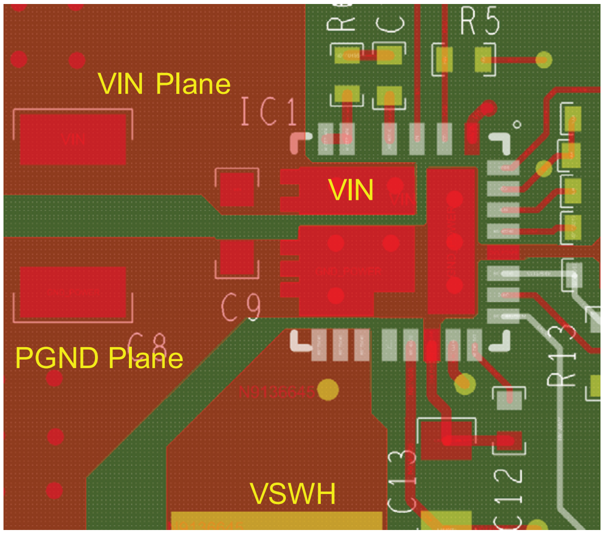


Fig. 30

1. Layout V_{IN} and P_{GND} planes as shown above.
2. Ceramic capacitors should be placed between V_{IN} and P_{GND}, and very close to the device for best decoupling effect.
3. Different values / packages of ceramic capacitors should be used to cover entire decoupling spectrum e.g. 1210 and 0603.
4. Smaller capacitance values, placed closer to device's V_{IN} pin(s), is better for high frequency noise absorbing.

Step 2: V_{CIN} Pin

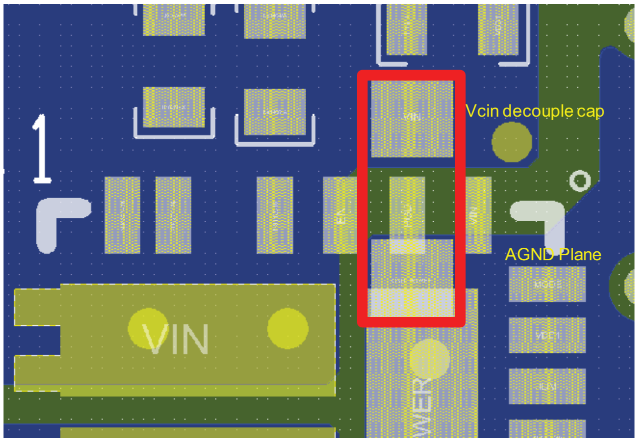


Fig. 31

1. V_{CIN} (pin 1) is the input pin for both internal LDO and t_{ON} block. T_{ON} time varies based on input voltage. It's necessary to put a decoupling capacitor close to this pin.
2. The connection can be made through a via and the cap can be placed at bottom layer.

Step 3: V_{SWH} Plane

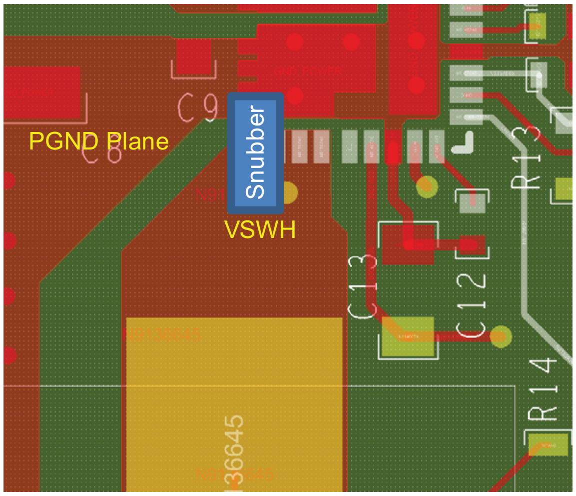


Fig. 32

1. Connect output inductor to SiC462 with large plane to lower the resistance.
2. If any snubber network is required, place the components on the bottom side as shown above.

Step 4: V_{DD}/V_{DRV} Input Filter

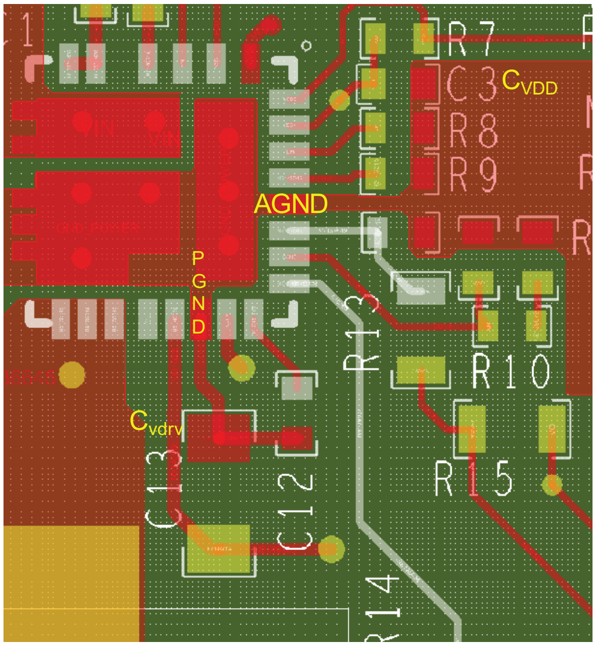


Fig. 33

1. C_{VDD} cap should be placed between pin 26 and pin 23 (the A_{GND} of driver IC) to achieve best noise filtering.
2. C_{VDRV} cap should be placed close to V_{DRV} (pin 16) and P_{GND} (pin 17) to reduce effects of trace impedance and provide maximum instantaneous driver current for low side MOSFET during switching cycle.

Step 5: BOOT Resistor and Capacitor Placement

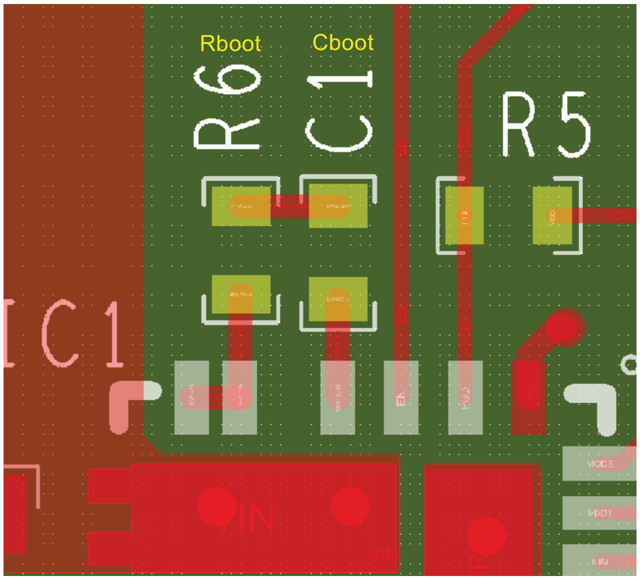


Fig. 34

1. These components need to be placed very close to SiC462, right between PHASE (pin 5, 6) and BOOT (pin 4).
2. In order to reduce parasitic inductance, it is recommended to use 0402 chip size for the resistor and the capacitor.

Step 6: Signal Routing

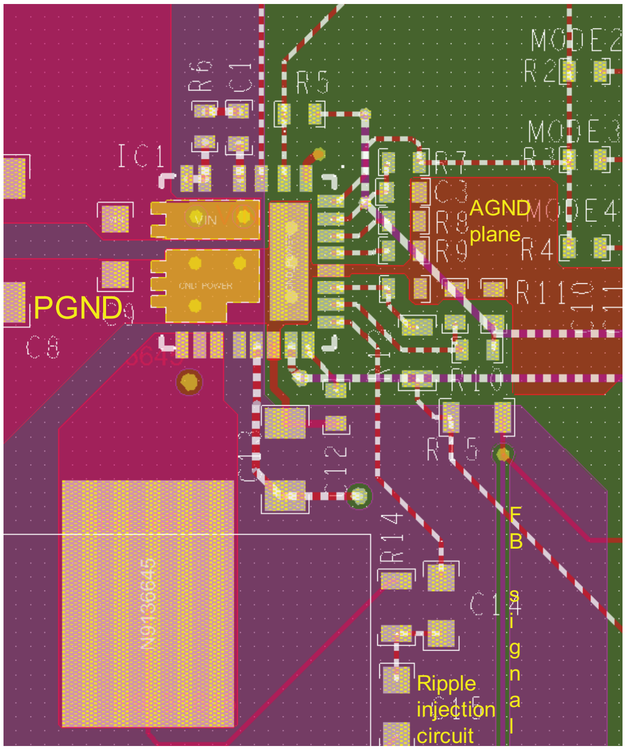


Fig. 35

1. Separate the small analog signal from high current path. As shown above, the high current paths with high dv/dt, di/dt are placed on the left side of the IC, while the small control signals are placed on the right side of the IC. All the components for small analog signal should be placed closer to IC with minimum trace length.
2. Pin 23 is the IC analog ground, which should have a single connection to power ground. The A_{GND} ground plane connected with pin 23 helps keep A_{GND} quiet and improve noise immunity.
3. Feedback signal can be routed through inner layer. Make sure this signal is far away from V_{SWH} node and shielded by inner ground layer.
4. Ripple injection circuit can be placed next to inductor. Kelvin connection as shown above is recommended.

Step 7: Adding Thermal Relief Vias and Duplicate Power Path Plane

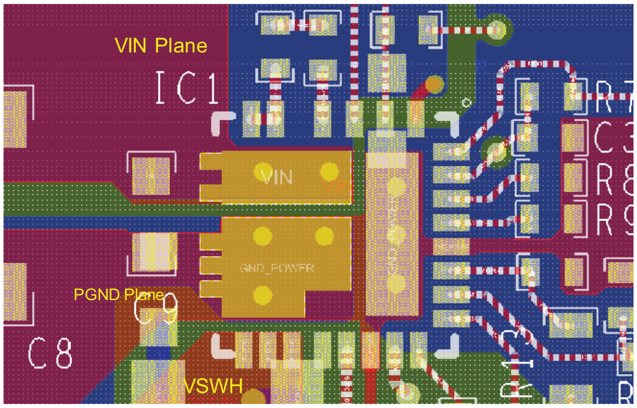


Fig. 36

1. Thermal relief vias can be added on the V_{IN} and P_{GND} pads to utilize inner layers for high-current and thermal dissipation.
2. To achieve better thermal performance, additional vias can be put on V_{IN} and P_{GND} plane. Also, it is necessary to duplicate the V_{IN} and ground planes at bottom layer to maximize the power dissipation capability from PCB.
3. V_{SWH} pad is a noise source and not recommended to put vias on this pad.
4. 8 mil drill for pads and 10 mils drill for plane are optional via sizes. The vias on pads may drain solder during assembly and cause assembly issues. Please consult with the assembly house for guidelines.

Step 8: Ground Layer

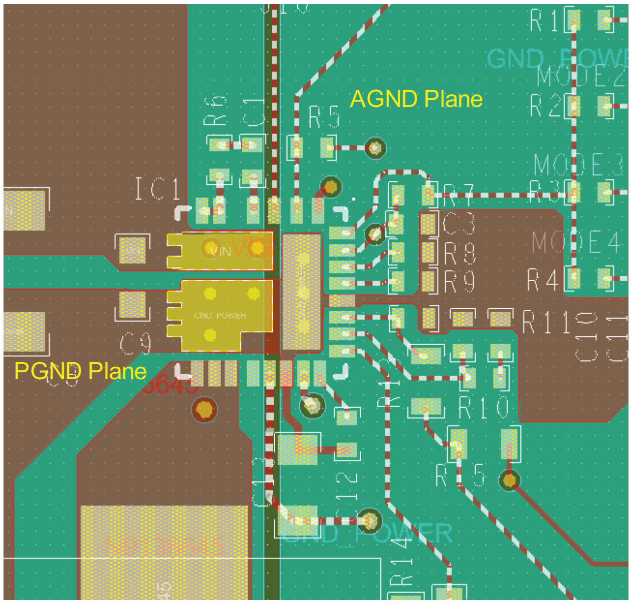
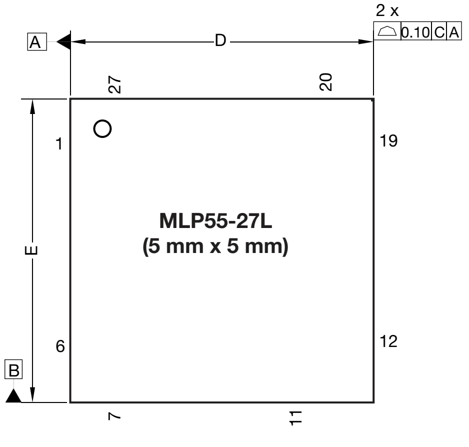


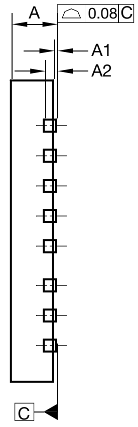
Fig. 37

1. It is recommended to make the entire inner layer (next to top layer) ground plane.
2. This ground plane provides shielding between noise source on top layer and signal trace within inner layer.
3. The ground plane can be broken into two sections as P_{GND} and A_{GND}.

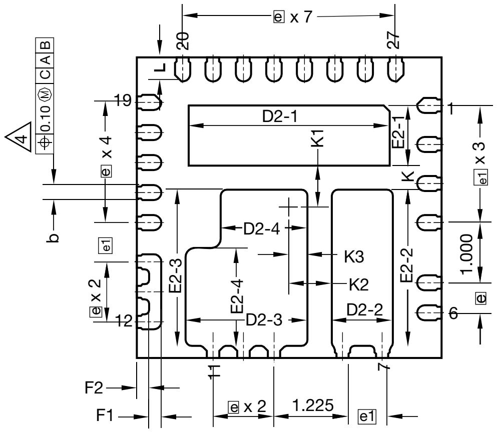
PACKAGE OUTLINE DRAWING PowerPAK® MLP55-27



Top view



Side view



Bottom view

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A (8)	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2	0.20 ref.			0.008 ref.		
b (4)	0.20	0.25	0.30	0.078	0.098	0.011
D	5.00 BSC			0.196 BSC		
e	0.50 BSC			0.019 BSC		
e1	0.65 BSC			0.0256 BSC		
E	5.00 BSC			0.196 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018
N (3)	28			28		
D2-1	3.25	3.30	3.35	0.128	0.130	0.132
D2-2	0.95	1.00	1.05	0.037	0.039	0.041
D2-3	1.95	2.00	2.05	0.077	0.079	0.081
D2-4	1.37	1.42	1.47	0.054	0.056	0.058
E2-1	0.95	1.00	1.05	0.037	0.039	0.041
E2-2	2.55	2.60	2.65	0.100	0.102	0.104
E2-3	2.55	2.60	2.65	0.100	0.102	0.104
E2-4	1.58	1.63	1.68	0.062	0.064	0.066
F1	0.20	-	0.25	0.008	-	0.010
F2	0.20 min.			0.008 min.		
K	0.40 BSC			0.016 BSC		
K1	0.70 BSC			0.028 BSC		
K2	0.70 BSC			0.028 BSC		
K3	0.30 BSC			0.012 BSC		

Notes

1. Use millimeters as primary measurement
2. Dimensioning and tolerances conform to ASME Y14.5M - 1994
3. N is the number of terminals, Nd is the number of terminals in x-direction, and Ne is the number of terminals in y-direction
4. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
5. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
6. Exact shape and size of this feature is optional
7. Package warpage max. 0.08 mm
8. Applied only for terminals

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