Features

- High-performance, Low-power Atmel® AVR® XMEGA® 8/16-bit Microcontroller
- Non-volatile Program and Data Memories
  - 64K - 256KBytes of In-System Self-Programmable Flash
  - 4K - 8KBytes Boot Section
  - 2K - 4KBytes EEPROM
  - 4K - 16KBytes Internal SRAM
- Peripheral Features
  - Four-channel DMA Controller
  - Eight-channel Event System
  - Seven 16-bit Timer/Counters
    - Four Timer/Counters with 4 Output Compare or Input Capture channels
    - Three Timer/Counters with 2 Output Compare or Input Capture channels
    - High Resolution Extensions on all Timer/Counters
    - Advanced Waveform Extension on one Timer/Counter
  - One USB device interface
    - USB 2.0 full speed (12Mbps) and low speed (1.5Mbps) device compliant
    - 32 Endpoints with full configuration flexibility
  - Seven USARTs with IrDA support for one USART
  - AES and DES Crypto Engine
  - CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3) Generator
  - Two Two-wire Interfaces with dual address match (I^2C and SMBus compatible)
  - Three Serial Peripheral Interfaces (SPIs)
  - 16-bit Real Time Counter with Separate Oscillator
  - Two Eight-channel, 12-bit, 2MSPS Analog to Digital Converters
  - One Two-channel, 12-bit, 1MSPS Digital to Analog Converter
  - Four Analog Comparators with Window compare function, and current source feature
  - External Interrupts on all General Purpose I/O pins
  - Programmable Watchdog Timer with Separate On-chip Ultra Low Power Oscillator
  - QTouch® library support
    - Capacitive touch buttons, sliders and wheels
    - Up to 64 sense channels
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal and External Clock Options with PLL
  - Programmable Multi-level Interrupt Controller
  - Five Sleep Modes
  - Programming and Debug Interfaces
    - JTAG (IEEE 1149.1 Compliant) Interface, including Boundary Scan
    - PDI (Program and Debug Interface)
- I/O and Packages
  - 50 Programmable I/O Pins
  - 64-lead TQFP
  - 64-pad QFN
- Operating Voltage
  - 1.6 – 3.6V
- Operating Frequency
  - 0 – 12MHz from 1.6V
  - 0 – 32MHz from 2.7V

Typical Applications

- Industrial control
- Factory automation
- Building control
- Board control
- White goods
- Climate control
- RF and ZigBee
- USB connectivity
- Sensor control
- Optical
- Low power battery applications
- Power tools
- HVAC
- Utility metering
- Medical applications

8/16-bit Atmel XMEGA A3U Microcontroller

ATxmega256A3U
ATxmega192A3U
ATxmega128A3U
ATxmega64A3U

Preliminary

8386A–AVR–07/11

1. Ordering Information

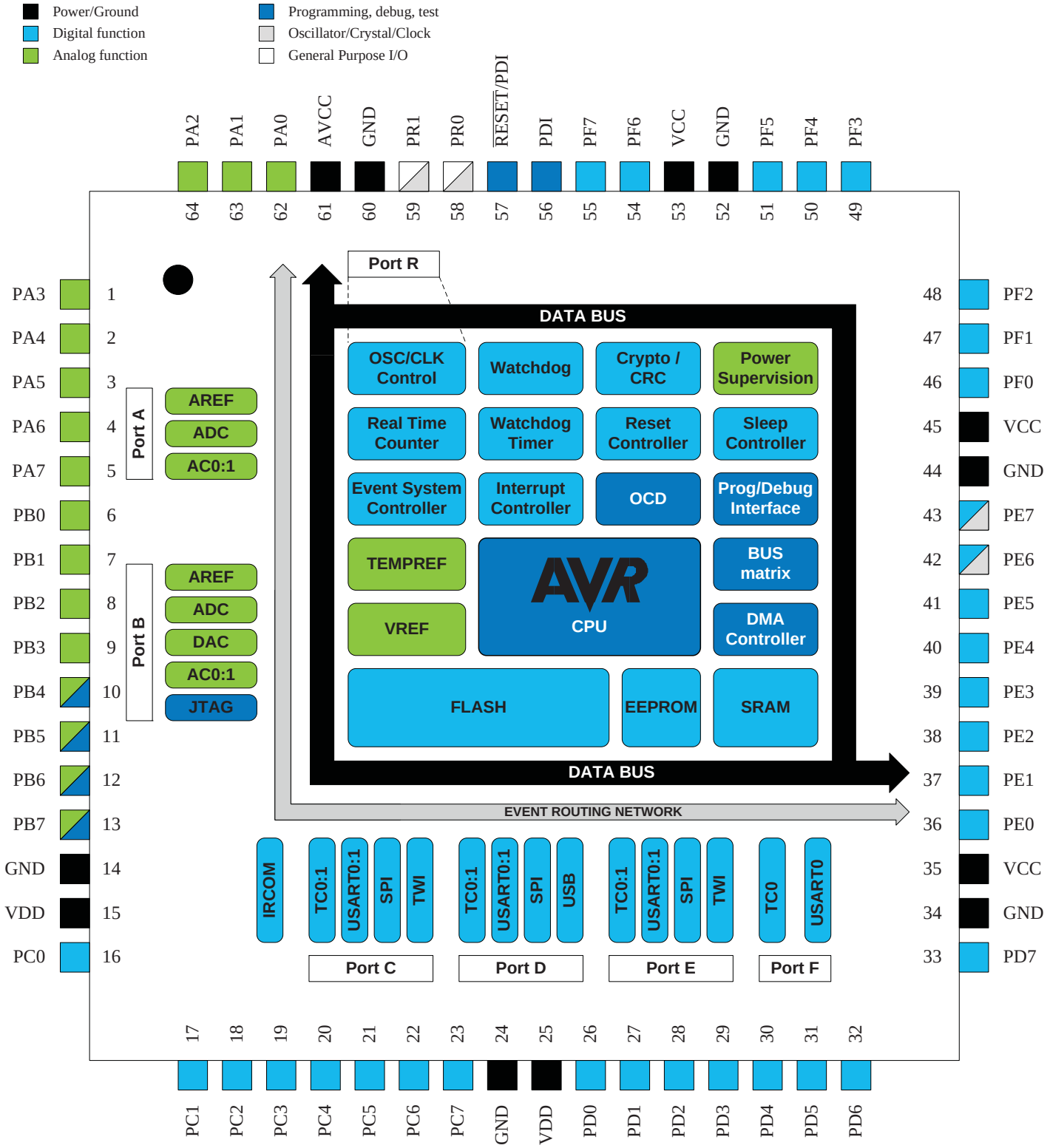
Ordering Code	Flash (Bytes)	EEPROM (Bytes)	SRAM (Bytes)	Speed (MHz)	Power Supply	Package[1][2][3]	Temp
ATxmega256A3U-AU	256K + 8K	4K	16K	32	1.6 - 3.6V	64A	-40°C - 85°C
ATxmega192A3U-AU	192K + 8K	2K	16K				
ATxmega128A3U-AU	128K + 8K	2K	8K				
ATxmega64A3U-AU	64K + 4K	2K	4K				
ATxmega256A3U-MH	256K + 8K	4K	16K			64M2	
ATxmega192A3U-MH	192K + 8K	2K	16K				
ATxmega128A3U-MH	128K + 8K	2K	8K				
ATxmega64A3U-MH	64K + 4K	2K	4K				

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For packaging information, see "Errata" on page 109

Package Type	
64A	64-lead, 14 x 14mm Body Size, 1.0mm Body Thickness, 0.8mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)
64M2	64-Pad, 9 x 9 x 1.0mm Body, Lead Pitch 0.50mm, 7.65mm Exposed Pad, Quad Flat No-Lead Package (QFN)

2. Pinout/Block Diagram

Figure 2-1. Block diagram and pinout



Note: 1. For full details on pinout and alternate pin functions refer to "Pinout and Pin Functions" on page 51.

3. Overview

The Atmel® AVR® XMEGA® is a family of low power, high performance and peripheral rich 8/16-bit microcontrollers based on the AVR® enhanced RISC architecture. By executing instructions in a single clock cycle, the AVR achieves throughputs CPU approaching 1 Million Instructions Per Second (MIPS) per MHz allowing the system designer to optimize power consumption versus processing speed.

Atmel AVR CPU combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs many times faster than conventional single-accumulator or CISC based microcontrollers.

The XMEGA A3U devices provide the following features: In-System Programmable Flash with Read-While-Write capabilities, Internal EEPROM and SRAM, four-channel DMA Controller, eight-channel Event System, Programmable Multi-level Interrupt Controller, 50 general purpose I/O Pins, 16-bit Real Time Counter, seven flexible 16-bit Timer/Counters with compare and PWM channels, one USB 2.0 full speed (12Mbps) Device Interface, seven USARTs, two Two Wire Serial Interfaces (TWIs), three Serial Peripheral Interfaces (SPIs), AES and DES crypto engine, two 8-channel 12-bit ADCs with optional differential input with programmable gain, one 2-channel 12-bit DACs, four analog comparators with window mode, programmable Watchdog Timer with separate Internal Oscillator, accurate internal oscillators with PLL and prescaler and programmable Brown-Out Detection.

The Program and Debug Interface (PDI), a fast 2-pin interface for programming and debugging, is available. The devices also have an IEEE std. 1149.1 compliant JTAG test interface, and this can also be used for On-chip Debug and programming.

All XMEGA devices have five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, DMA Controller, Event System, Interrupt Controller and all peripherals to continue functioning. The Power-down mode saves the SRAM and register contents but stops the oscillators, disabling all other functions until the next TWI or pin-change interrupt, or Reset. In Power-save mode, the asynchronous Real Time Counter continues to run, allowing the application to maintain a timer base while the rest of the device is sleeping. In Standby mode, the Crystal/Resonator Oscillator is kept running while the rest of the device is sleeping. This allows very fast start-up from external crystal combined with low power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run. To further reduce power consumption, the peripheral clock to each individual peripheral can optionally be stopped in Active mode and Idle sleep mode.

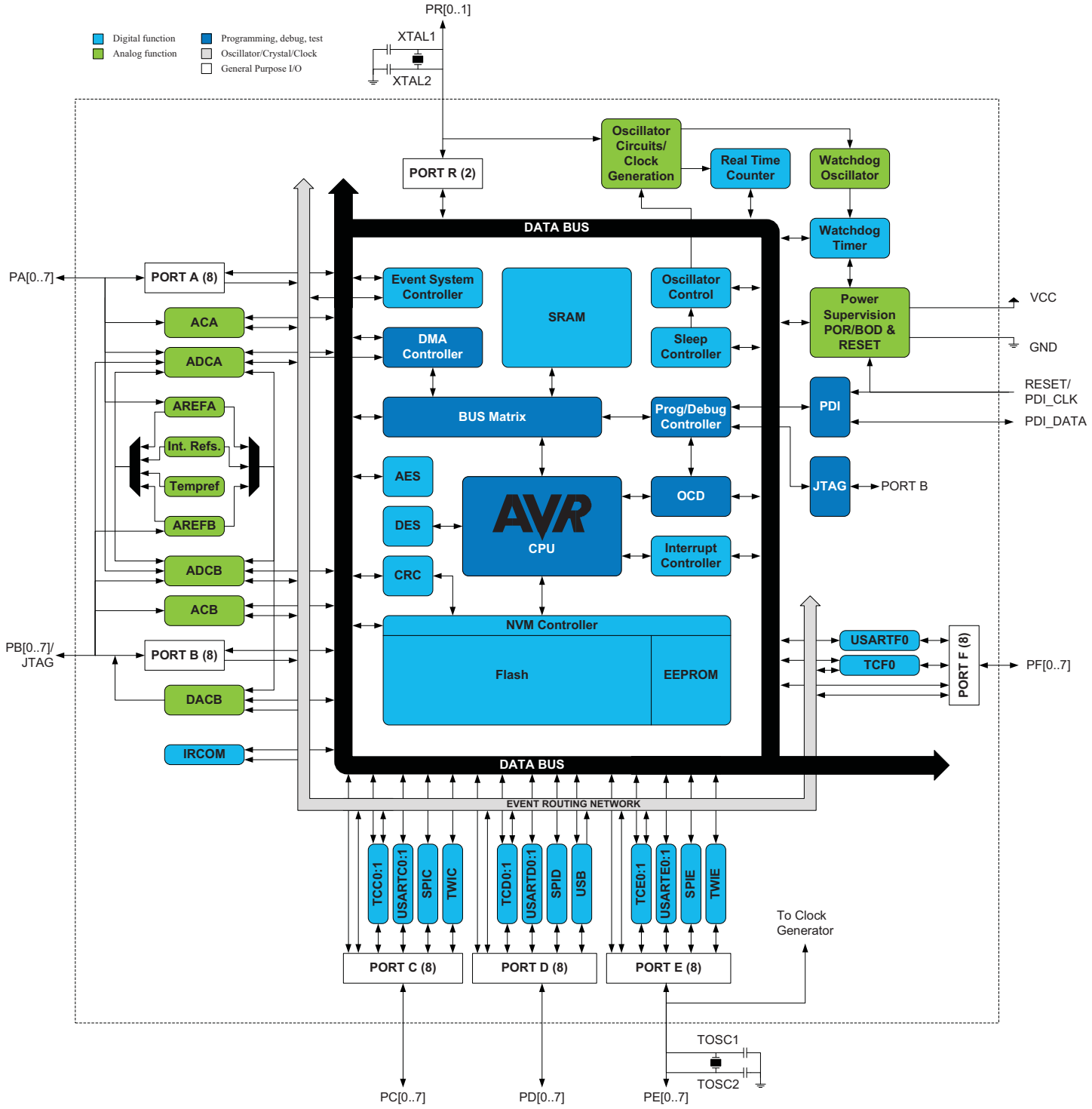
Atmel offers a free QTouch® library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The program Flash memory can be reprogrammed in-system through the PDI or JTAG. A Bootloader running in the device can use any interface to download the application program to the Flash memory. The Bootloader software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8/16-bit RISC CPU with In-System Self-Programmable Flash, the Atmel XMEGA A3U is a powerful microcontroller family that provides a highly flexible and cost effective solution for embedded applications.

The XMEGA devices are supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, programmers, and evaluation kits.

3.1 Block Diagram

Figure 3-1. XMEGA A3U Block Diagram



4. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

4.1 Recommended reading

- XMEGA® AU Manual
- XMEGA Application Notes

This device data sheet only contains part specific information with a short description of each peripheral and module. The XMEGA AU Manual describes the modules and peripherals in depth. The XMEGA application notes contain example code and show applied use of the modules and peripherals.

All documentations are available from www.atmel.com/avr.

5. Capacitive touch sensing

The Atmel® QTouch® Library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR® microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS™) technology for unambiguous detection of key events. The QTouch Library includes support for the QTouch and QMatrix® acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch Library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The QTouch Library is FREE and downloadable from the Atmel website at the following location: www.atmel.com/qtouchlibrary. For implementation details and other information, refer to the Atmel QTouch Library User Guide - also available for download from the Atmel website.

6. AVR CPU

6.1 Features

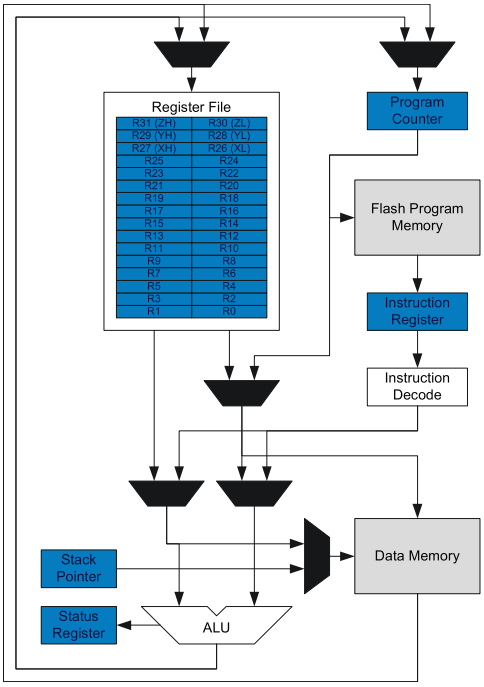
- 8/16-bit high performance AVR RISC Architecture
  - 142 instructions
  - Hardware multiplier
- 32x8-bit registers directly connected to the ALU
- Stack in SRAM
- Stack Pointer accessible in I/O memory space
- Direct addressing of up to 16Mbytes of program and 16Mbytes of data memory
- True 16/24-bit access to 16/24-bit I/O registers
- Support for 8-, 16- and 32-bit Arithmetic
- Configuration Change Protection of system critical features

6.2 Overview

The Atmel® AVR® XMEGA® devices use the 8/16-bit AVR CPU. The main function of the CPU is to execute the code and perform all calculations. The CPU is able to access memories, perform calculations, control peripherals, and execute the program from the FLASH memory. Interrupt handling is described in a separate section, refer to ”Interrupts and Programmable Multi-level Interrupt Controller” on page 26.

Figure 6-1 on page 7 shows the block diagram of the AVR CPU architecture.

Figure 6-1. Block Diagram of the AVR CPU architecture



In order to maximize performance and parallelism, the AVR uses a Harvard architecture with separate memories and buses for program and data. Instructions in the program memory are executed with a single level pipelining. While one instruction is being executed, the next instruc-

tion is pre-fetched from the Program Memory. This enables instructions to be executed in every clock cycle.

The program memory is In-System Self-Programmable Flash memory.

6.3 ALU - Arithmetic Logic Unit

The Arithmetic Logic Unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed. The ALU operates in direct connection with all the 32 general purpose registers. In a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed and the result is stored back in the Register File. After an arithmetic or logic operation, the Status Register is updated to reflect information about the result of the operation.

The ALU operations are divided into three main categories – arithmetic, logical, and bit-functions. Both 8- and 16-bit arithmetic is supported, and the instruction set allows for efficient implementation of 32-bit arithmetic. The hardware multiplier supports signed and unsigned multiplication and fractional format.

6.4 Program Flow

After reset, the CPU starts to execute instructions from the lowest address in the Flash Program Memory ‘0’. The Program Counter (PC) addresses the next instruction to be fetched. After a reset, the PC is set to location ‘0’.

Program flow is provided by conditional and unconditional jump and call instructions, capable of addressing the whole address space directly. Most AVR instructions use a 16-bit word format, while a limited number uses a 32-bit format.

During interrupts and subroutine calls, the return address PC is stored on the Stack. The Stack is allocated in the general data SRAM, and consequently the Stack size is only limited by the total SRAM size and the usage of the SRAM. After reset the Stack Pointer (SP) points to the highest address in the internal SRAM. The SP is read/write accessible in the I/O memory space, enabling easy implementation of multiple stacks or stack areas. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR CPU.

6.5 Register File

The Register File consists of 32 x 8-bit general purpose working registers with single clock cycle access time. The Register File supports the following input/output schemes:

- One 8-bit output operand and one 8-bit result input
- Two 8-bit output operands and one 8-bit result input
- Two 8-bit output operands and one 16-bit result input
- One 16-bit output operand and one 16-bit result input

Six of the 32 registers can be used as three 16-bit address register pointers for data space addressing - enabling efficient address calculations. One of these address pointers can also be used as an address pointer for look up tables in Flash program memory.

7. Memories

7.1 Features

- Flash Program Memory
  - One linear address space
  - In-System Programmable
  - Self-Programming and Bootloader support
  - Application Section for application code
  - Application Table Section for application code or data storage
  - Boot Section for application code or bootloader code
  - Separate read/write protection lock bits for all sections
  - CRC Generator support for CRC check of a selectable flash program memory section
- Data Memory
  - One linear address space
  - Single cycle access from CPU
  - SRAM
  - EEPROM
    - Byte and page accessible
    - Optional memory mapping for direct load and store
  - I/O Memory
    - Configuration and Status registers for all peripherals and modules
    - 16bit-accessible General Purpose Register for global variables or flags
  - Bus arbitration
    - Safe and deterministic handling of priority between CPU, DMA Controller, and other bus masters
  - Separate buses for SRAM, EEPROM, and I/O Memory
    - Simultaneous bus access for CPU and DMA Controller
- Production Signature Row Memory for factory programmed data
  - ID for each microcontroller device type
  - Serial number for each device
  - Calibration bytes for factory calibrated peripherals
- User Signature Row
  - One flash page in size
  - Can be read and written from software
  - Content is kept after chip erase

7.2 Overview

The Atmel® AVR® architecture has two main memory spaces, the Program Memory and the Data Memory. Executable code can only reside in the Program Memory, while data can be stored both in the Program Memory and the Data Memory. The Data Memory includes both SRAM, and EEPROM Memory for nonvolatile data storage. All memory spaces are linear and require no memory bank switching.

The available memory size configurations are shown in ”Ordering Information” on page 2. In addition each device has a Flash memory signature rows for calibration data, device identification, serial number etc.

Non Volatile Memory (NVM) spaces can be locked for further write and read/write operations. This prevents unrestricted access to the application software.

7.3 Flash Program Memory

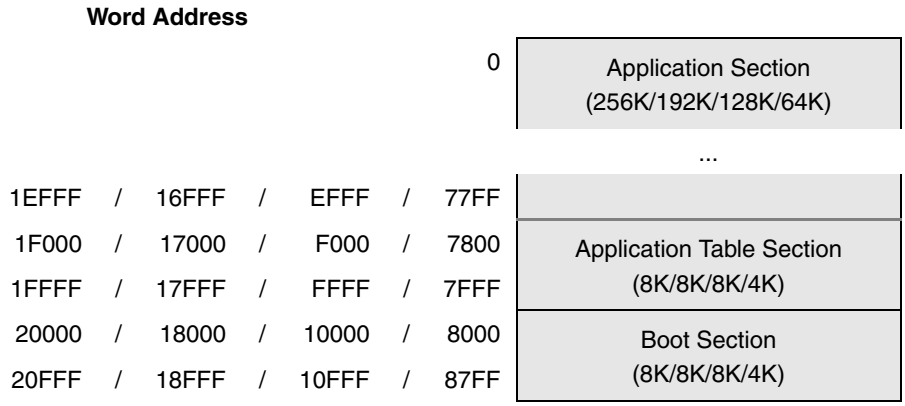
The Atmel® AVR® XMEGA® devices contain On-chip In-System Reprogrammable Flash memory for program storage. The Flash memory can be accessed for read and write both from an external programmer through the PDI, or from application software running in the device.

All AVR instructions are 16- or 32-bit wide, each Flash address location is 16-bit.

The Flash memory is organized in two main sections, the Application Section and the Boot Loader section. The size of the different sections are fixed, but device dependent. These two sections have separate lock bits and can have different levels of protection. The Store Program Memory (SPM) instruction, used to write to the Flash from the application software, will only operate when executed from the Boot Loader Section.

The Application Section contains an Application Table Section with separate lock settings. This enables safe storage of Non-volatile data in the Program Memory.

Figure 7-1. Flash Program Memory (Hexadecimal address)

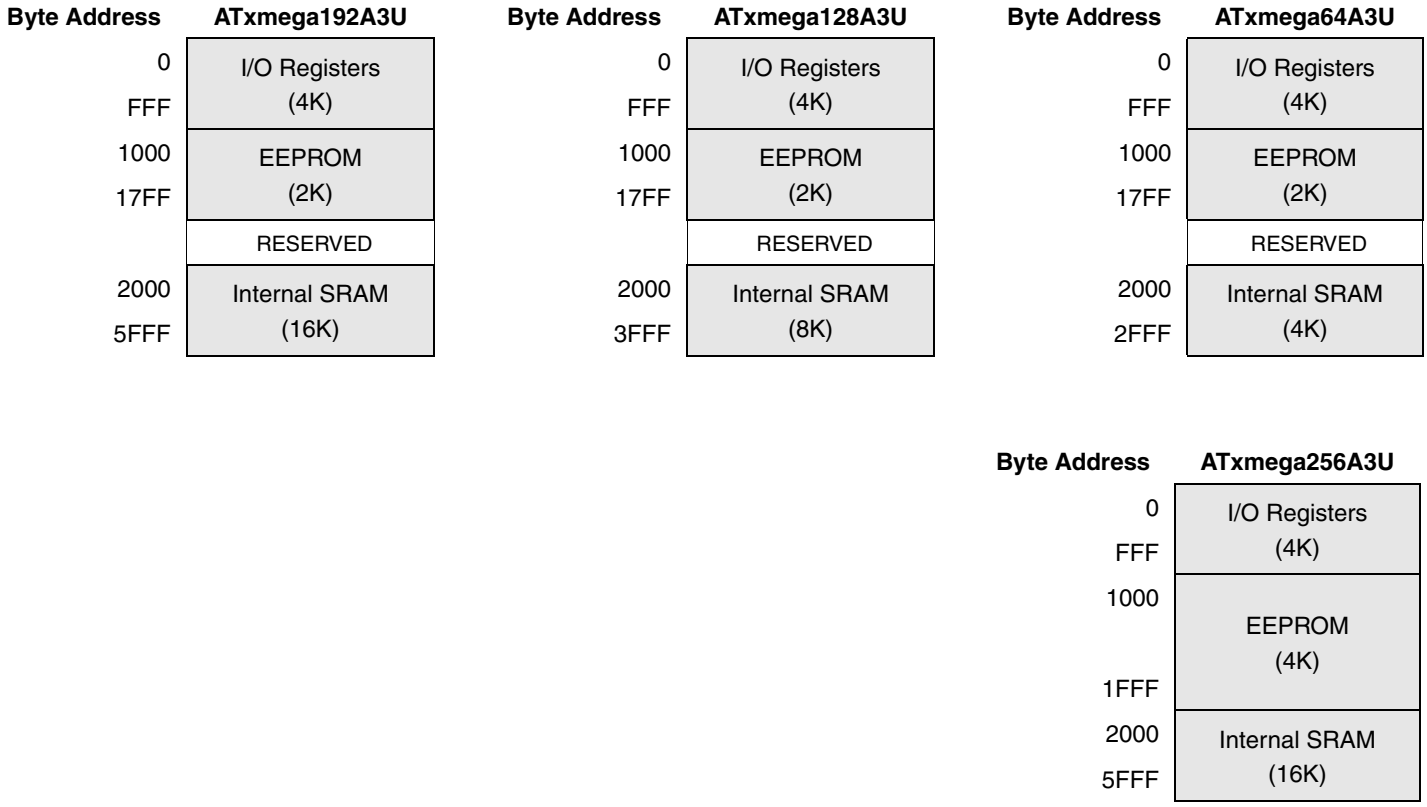


The Application Table Section and Boot Section can also be used for general application software.

7.4 Data Memory

The Data memory contains the I/O Memory, internal SRAM, optionally memory mapped EEPROM, and external memory if available. The data memory is organized as one continuous memory section, see Figure 7-2 on page 11. To simplify development, I/O Memory, EEPROM and SRAM will always have the same start addresses for all XMEGA devices.

Figure 7-2. Data Memory Map (Hexadecimal address)



7.4.1 I/O Memory

The Status and configuration registers for peripherals and modules, including the CPU, are addressable through I/O memory locations. All I/O locations can be accessed by the load (LD/LDS/LDD) and store (ST/STS/STD) instructions, which is used to transfer data between the 32 registers in the Register File and the I/O memory. The IN and OUT instructions can address I/O memory locations in the range 0x00 - 0x3F directly. In the address range 0x00 - 0x1F, single- cycle instructions for manipulation and checking of individual bits are available.

The I/O memory address for all peripherals and modules in XMEGA A3U is shown in the ”Peripheral Module Address Map” on page 56.

7.4.2 SRAM Data Memory

The devices have internal SRAM memory for data storage.

7.4.3 EEPROM Data Memory

The devices have internal EEPROM memory for non-volatile data storage. It is addressable either in a separate data space or it can be memory mapped into the normal data memory space. The EEPROM memory supports both byte and page access.

7.5 Production Signature Row

The Production Signature Row is a separate memory section for factory programmed data. It contains calibration data for functions such as oscillators and analog modules.

The production signature row also contains an ID that identifies each microcontroller device type, and a serial number that is unique for each manufactured device. The device ID for the available devices is shown in Table 7-1 on page 13. The serial number consist of the production LOT number, wafer number, and wafer coordinates for the device.

The production signature row can not be written or erased, but it can be read from both application software and external programming.

Table 7-1. Device ID bytes for XMEGA A3U devices.

Device	Device ID bytes		
	Byte 2	Byte 1	Byte 0
ATxmega64A3U	42	96	1E
ATxmega128A3U	42	97	1E
ATxmega192A3U	44	97	1E
ATxmega256A3U	42	98	1E

7.6 User Signature Row

The User Signature Row is a separate memory section that is fully accessible (read and write) from application software and external programming. It is one flash page in size, and is meant for static user parameter storage, such as calibration data, custom serial numbers or identification numbers, random number seeds etc. This section is not erased by Chip Erase commands that erase the Flash, and requires a dedicated erase command. This ensures parameter storage during multiple program/erase session and on-chip debug sessions.

7.7 Flash and EEPROM Page Size

The Flash Program Memory and EEPROM data memory are organized in pages. The pages are word accessible for the Flash and byte accessible for the EEPROM.

Table 7-2 on page 14 shows the Flash Program Memory organization. Flash write and erase operations are performed on one page at a time, while reading the Flash is done one byte at a time. For Flash access the Z-pointer (Z[m:n]) is used for addressing. The most significant bits in the address (FPAGE) gives the page number and the least significant address bits (FWORD) gives the word in the page.

Table 7-2. Number of words and Pages in the Flash.

Devices	Flash Size	Page Size (words)	FWORD	FPAGE	Application		Boot	
					Size	No of Pages	Size	No of Pages
ATxmega64A3U	64K + 4K	128	Z[7:1]	Z[16:8]	64K	256	4K	16
ATxmega128A3U	128K + 8K	256	Z[8:1]	Z[17:9]	128K	256	8K	16
ATxmega192A3U	192K + 8K	256	Z[8:1]	Z[18:9]	192K	384	8K	16
ATxmega256A3U	256K + 8K	256	Z[8:1]	Z[18:9]	256K	512	8K	16

Table 7-3 on page 14 shows EEPROM memory organization for the XMEGA A3U devices. EEEPROM write and erase operations can be performed one page or one byte at a time, while reading the EEPROM is done one byte at a time. For EEPROM access the NVM Address Register (ADDR[m:n]) is used for addressing. The most significant bits in the address (E2PAGE) gives the page number and the least significant address bits (E2BYTE) gives the byte in the page.

Table 7-3. Number of bytes and Pages in the EEPROM.

Devices	EEPROM Size	Page Size (Bytes)	E2BYTE	E2PAGE	No of Pages
ATxmega64A3U	2K	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega128A3U	2K	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega192A3U	2K	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega256A3U	4K	32	ADDR[4:0]	ADDR[11:5]	128

8. DMAC - Direct Memory Access Controller

8.1 Features

- The DMA Controller allows data transfers with minimal CPU intervention
  - from data memory to data memory
  - from data memory to peripheral
  - from peripheral to data memory
  - from peripheral to peripheral
- Four DMA Channels with separate
  - transfer triggers
  - interrupt vectors
  - addressing modes
- Programmable channel priority
- From 1byte to 16Mbytes of data in a single transaction
- Multiple addressing modes
  - Static
  - Increment
  - Decrement
- Optional reload of source and destination address at the end of each
  - Burst
  - Block
  - Transaction
- Optional Interrupt on end of transaction
- Optional connection to CRC Generator module for CRC on DMA data

8.2 Overview

The 4-channel Direct Memory Access (DMA) Controller can transfer data between memories and peripherals, and thus offload these tasks from the CPU. It enables high data transfer rates with minimum CPU intervention, and frees up CPU time. The 4 DMA channels enable up to four independent and parallel transfers.

The DMA Controller can move data between SRAM and peripherals, between SRAM locations and between peripheral registers directly. With access to all peripherals the DMA Controller can handle automatic transfer of data to/from communication modules, as well as data retrieval from ADC conversions, or data transfer to or from port pins. The DMA Controller can also read from memory mapped EEPROM.

Data transfers are done in continues bursts of 1, 2, 4 or 8bytes. They build block transfers of configurable size from 1 to 64Kbytes. A repeat counter can be used to repeat each block transfer for single transactions up to 16Mbytes. Source and destination addressing can be static, incremental or decremental. Automatic reload of source and/or destination address can be done after each burst, block transfer, or when transaction is complete. Application software, peripherals and events can trigger DMA transfers.

The four DMA channels have individual configuration and control settings. This include source, destination, transfer triggers and transaction sizes. They have individual interrupt settings. Interrupt requests can be generated both when a transaction is complete or if the DMA Controller detects an error on a DMA channel.

To allow for continuous transfers, two channels can be interlinked so that the second takes over the transfer when the first is finished and vice versa.

9. Event System

9.1 Features

- System for direct peripheral to peripheral communication and signaling
- Peripherals can directly send, receive and react to peripheral events
  - CPU and DMA controller independent operation
  - 100% predictable signal timing
  - Short and guaranteed response time
- 8 Event Channels for up to 8 different and parallel signal routines and configurations
- Events can be sent and/or used by most peripherals, clock system and software
- Additional functions include
  - Quadrature Decoders
  - Digital Filtering of I/O pin change
- Works in Active mode and Idle sleep mode

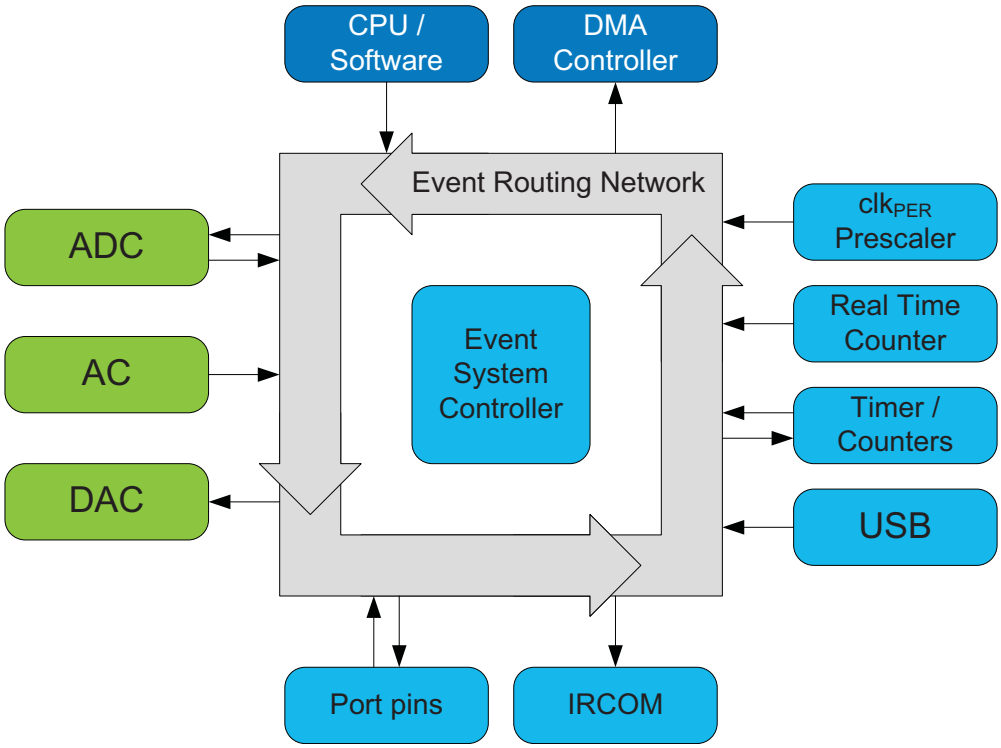
9.2 Overview

The Event System is system for direct peripheral to peripheral communication and signaling. It enables the possibility for a change in one peripheral to automatically trigger actions in others peripherals. It is designed for having a predictable system for short and guaranteed response time between peripherals. It is simple and powerful since it allows for autonomous peripheral control and interaction without use of interrupts, CPU or DMA Controller resources. It also enables synchronized timing of actions in several peripheral modules.

The change in a peripheral is referred to as an event, and is it usually the same as the interrupt conditions for the peripheral. These events can be directly passed to other peripherals using a dedicated routing network called the Event Routing Network. How events are routed and used by other peripherals is configured in software.

Figure 9-1 on page 17 shows a basic block diagram of all connected peripherals. The Event System can directly connect together Analog and Digital converters, Analog Comparators, I/O ports pins, the Real-time Counter, Timer/Counters, IR Communication Module (IRCOM), and USB. It can also be used to trigger DMA transactions (DMA Controller). Events can also be generated from software and the Peripheral Clock.

Figure 9-1. Event system block diagram.



The Event Routing Network consists of eight software configurable multiplexers that control how events are routed and used. This is called Event Channels and it enables up to eight parallel event configurations and routings. The maximum routing latency between two peripherals is two Peripheral clock cycles. The Event System works in both Active mode and Idle sleep mode.

10. System Clock and Clock options

10.1 Features

- **Fast start-up time**
- **Safe run-time clock switching**
- **Internal Oscillators:**
  - **32MHz run-time calibrated and tuneable oscillator**
  - **2MHz run-time calibrated oscillator**
  - **32.768kHz calibrated oscillator**
  - **32kHz Ultra Low Power (ULP) oscillator with 1kHz output**
- **External clock options**
  - **0.4 - 16MHz Crystal Oscillator**
  - **32kHz Crystal Oscillator**
  - **External clock**
- **PLL with 20 - 128MHz output frequency**
  - **Internal and external clock options and 1 to 31x multiplication**
  - **Lock detector**
- **Clock Prescalers with 1 to 2048x division**
- **Fast peripheral clocks running at 2 and 4 times the CPU clock frequency**
- **Automatic Run-Time Calibration of internal oscillators**
- **External oscillator and PLL lock failure detection with optional non maskable interrupt**

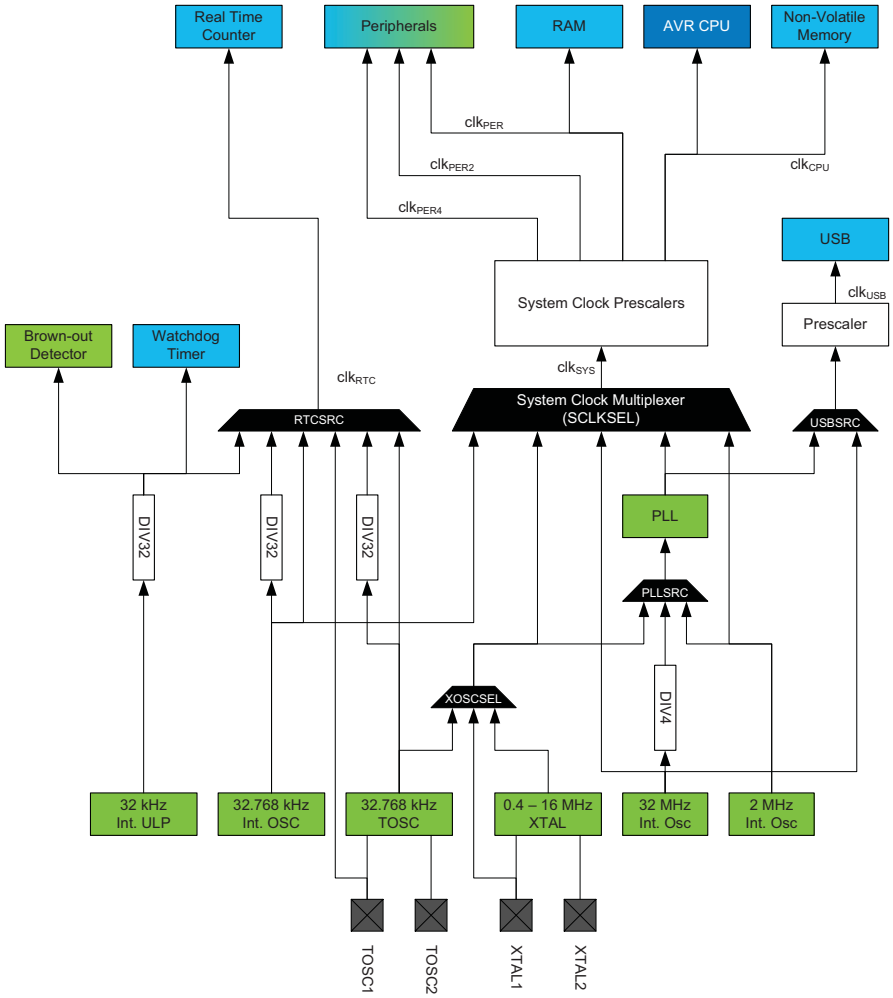
10.2 Overview

The flexible clock system supports a large number of clock sources. It incorporates both accurate internal oscillators, and external crystal oscillators and resonator support. A high frequency Phase Locked Loop (PLL) and clock prescalers can be used to generate a wide range of clock frequencies. A calibration feature (DFLL) is available, and can be used for automatic runtime calibration of the internal oscillators to remove frequency drift over voltage and temperate. An Oscillator Failure Monitor can be enabled to issue a Non-Maskable Interrupt and switch to internal oscillator if the external oscillator or PLL fails.

When a reset occur, all clock sources except 32kHz Ultra Low Power oscillator are disabled. After reset, the device will always start up running from the 2MHz internal oscillator. During normal operation, the System Clock source and prescalers can be changed from software at any time.

Figure 10-1 on page 19 presents the principal clock system in the XMEGA. All of the clocks do not need to be active at a given time. The clocks to the CPU and peripherals can be stopped using sleep modes and power reduction registers.

Figure 10-1. The Clock system, clock sources and clock distribution



10.3 Clock Options

10.3.1 32kHz Ultra Low Power Internal Oscillator

This oscillator provides an approximate 32kHz clock. The 32kHz Ultra Low Power (ULP) Internal Oscillator is a very low power clock source, and it is not designed for high accuracy. The oscillator employs a built in prescaler providing a 1kHz output. The oscillator is automatically enabled/disabled when used as clock source for any part of the device. This oscillator can be selected as clock source for the RTC.

10.3.2 32.768kHz Calibrated Internal Oscillator

This oscillator provides an approximate 32.768kHz clock. A factory-calibrated value is written to the 32.768kHz oscillator calibration register during reset to ensure that the oscillator is running within its specification. The calibration register can also be written from software for run-time calibration of the oscillator frequency. The oscillator employs a built in prescaler providing both a 32.768kHz output and a 1.024kHz output.

10.3.3 32.768kHz Crystal Oscillator

A 32.768kHz crystal oscillator can be connected between TOSC1 and TOSC2 pins and enable a dedicated low frequency oscillator input circuit. A low power mode with reduced voltage swing on TOSC2 is available. This oscillator can be used as clock source for the System Clock, RTC and as the DFLL reference clock.

10.3.4 0.4 - 16MHz Crystal Oscillator

The 0.4 - 16MHz Crystal Oscillator is a driver intended for driving both external resonators and crystals ranging from 400kHz to 16MHz.

10.3.5 2MHz Run-time Calibrated Internal Oscillator

The 2MHz Run-time Calibrated Internal Oscillator is the default system clock source after reset. It is calibrated during production to provide a default frequency which is close to its nominal frequency. A Digital Frequency Looked Loop (DFLL) that can be enabled for automatic run-time calibration of the oscillator to compensate for temperature and voltage drift to optimize the oscillator accuracy.

10.3.6 32MHz Run-time Calibrated Internal Oscillator

The 32MHz Run-time Calibrated Internal Oscillator is a high frequency oscillator. It is calibrated during production to provide a default frequency which is close to its nominal frequency. A DFLL that can be enabled for automatic run-time calibration of the oscillator to compensate for temperature and voltage drift to optimize the oscillator accuracy This oscillator can also be adjusted and calibrated to any frequency between 30 and 55MHz.

10.3.7 External Clock input

The external clock input gives the possibility to connect a clock from an external source to XTAL1.

10.3.8 PLL with Multiplication factor 1 - 31x

The PLL provides the possibility of multiplying a frequency by any number from 1 to 31. In combination with the prescalers, this gives a wide range of output frequencies from all clock sources.

11. Power Management and Sleep Modes

11.1 Features

- **Power management for adjusting power consumption and enabled functions**
- **5 sleep modes:**
  - **Idle**
  - **Power-down**
  - **Power-save**
  - **Standby**
  - **Extended standby**
- **Power Reduction register to disable clock and turn off unused peripherals in Active and Idle mode**

11.2 Overview

Various sleep modes and clock gating are implemented in order to tailor power consumption to the application's requirement. This enables the microcontroller to stop unused modules to save power.

All sleep modes are available and can be entered from Active mode. In Active mode the CPU is executing application code. When the device enters sleep mode, program execution is stopped and interrupts or reset is used to wake the device again. The application code decides when and what sleep mode to enter. Interrupts from enabled peripherals and all enabled reset sources can restore the microcontroller from sleep to Active mode.

In addition, Power Reduction registers provide a method to stop the clock to individual peripherals from software. When this is done, the current state of the peripheral is frozen and there is no power consumption from that peripheral. This reduces the power consumption in Active mode and Idle sleep mode and enable much more fine-tuned power management than sleep modes alone.

11.3 Sleep Modes

11.3.1 Idle Mode

In Idle mode the CPU and Non-Volatile Memory are stopped, but all peripherals including the Interrupt Controller, Event System and DMA Controller are kept running. Any enabled interrupt will wake the device.

11.3.2 Power-down Mode

In Power-down mode all clocks, including the Real Time Counter clock source are stopped. This only allows operation of asynchronous modules that does not require a running clock. The only interrupts that can wake up the MCU are the Two Wire Interface address match interrupt, asynchronous port interrupts and USB resume interrupt.

11.3.3 Power-save Mode

Power-save mode is identical to Power-down, with one exception, if the Real Time Counter (RTC) is enabled, it will keep running during sleep and the device can also wake up from either RTC Overflow or Compare Match interrupt.

11.3.4 Standby Mode

Standby mode is identical to Power-down with the exception that the enabled system clock sources are kept running, while the CPU, Peripheral and RTC clocks are stopped. This reduces the wake-up time.

11.3.5 Extended Standby Mode

Extended Standby mode is identical to Power-save mode with the exception that the enabled system clock sources are kept running while the CPU and Peripheral clocks are stopped. This reduces the wake-up time.

12. System Control and Reset

12.1 Features

- **Reset the microcontroller and set it to its initial state when a reset source goes active**
- **Multiple reset sources that cover different situations**
  - **Power-On Reset**
  - **External Reset**
  - **Watchdog Reset**
  - **Brown-Out Reset**
  - **PDI reset**
  - **Software reset**
- **Asynchronous operation**
  - **No running system clock in the device is required for the reset**
- **Reset Status Register for reading the reset source from the application code**

12.2 Overview

The Reset System issues a microcontroller reset and set the device to its initial state. This is for situation where operation should not start or continue, for example when the microcontroller operates below its power supply rating. If a reset source goes active, the device enters and be kept in reset until all reset sources have released their reset. The I/O pins are immediately tristated.

The program counter is set to the Reset Vector location and all I/O registers are set to the initial value. The SRAM content is kept, but not guaranteed.

After reset is released from all reset sources, the default oscillator is started and calibrated before the device starts running from the Reset Vector address. By default this is the lowest program memory address, '0', but it is possible to move the Reset Vector to the lowest address in the Boot Section.

The reset functionality is asynchronous, so no running system clock is required to reset the device. The software reset feature makes it possible to issue a controlled system reset from the user software.

The reset status register has individual status flags for each reset source. It is cleared at Power-on Reset, it shows which sources that have issued a reset since the last power-on.

12.3 Reset Sources

12.3.1 Power-On Reset

The device is reset when the supply voltage VCC is below the Power-on Reset threshold voltage.

12.3.2 External Reset

The device is reset when a low level is present on the RESET pin.

12.3.3 Watchdog Reset

The device is reset when the Watchdog Timer period expires and the Watchdog Reset is enabled. The Watchdog Timer runs from a dedicated oscillator independent of the System Clock. For more details see ”WDT - Watchdog Timer” on page 25.

12.3.4 Brown-Out Reset

The device is reset when the supply voltage VCC is below the Brown-Out Reset threshold voltage and the Brown-out Detector is enabled. The Brown-out threshold voltage is programmable.

12.3.5 JTAG reset

The device is reset as long as there is a logic one in the Reset Register in one of the scan chains of the JTAG system. Refer to IEEE 1149.1 (JTAG) Boundary-scan for details.

12.3.6 PDI reset

The MCU can be reset through the Program and Debug Interface (PDI).

12.3.7 Software reset

The MCU can be reset by the CPU writing to a special I/O register through a timed sequence.

13. WDT - Watchdog Timer

13.1 Features

- **Issues a device reset if the timer is not reset before its timeout period**
- **Asynchronously operation from dedicated oscillator**
  - **1kHz output of the 32kHz Ultra Low Power oscillator**
- **11 selectable timeout periods, from 8ms to 8s.**
- **Two operation modes**
  - **Normal mode**
  - **Window mode**
- **Configuration lock to prevent unwanted changes**

13.2 Overview

The Watchdog Timer (WDT) is a system function for monitoring correct program operation. It makes it possible to recover from error situations such as run-away or dead-lock code. The WDT is a timer, configured to a predefined timeout period and is constantly running when enabled. If the WDT is not reset within the timeout period, it will issue a microcontroller reset. The WDT is reset by executing the WDR (Watchdog Timer Reset) instruction from the application code.

The window mode makes it possible to define a time slot window inside the total timeout period where WDT must be reset within. If the WDT is reset too early or too late and outside this window, a system reset will be issued. Compared to the normal mode, this can also catch situations where a code error also causes constant WDR execution.

The WDT will run in Active mode and all sleep modes if enabled. It is asynchronous and runs from a CPU independent clock source, and will continue to operate to issue a system reset even if the main clocks fail. The Configuration Change Protection mechanism ensures that the WDT settings cannot be changed by accident. For increased safety, a fuse for locking the WDT settings is available.

14. Interrupts and Programmable Multi-level Interrupt Controller

14.1 Features

- **Short and predictable interrupt response time**
- **Separate interrupt configuration and vector address for each interrupt**
- **Programmable Multi-level Interrupt Controller**
  - **Interrupt prioritizing according to level and vector address**
  - **3 selectable interrupt levels for all interrupts: Low, Medium and High**
  - **Selectable round-robin priority scheme within low level interrupts**
  - **Non-Maskable Interrupts for critical functions**
- **Interrupt vectors can be moved from the Application Section to the Boot Loader Section**

14.2 Overview

Atmel® AVR® XMEGA® have a Programmable Multi-level Interrupt Controller (PMIC). Interrupts signal a change of state in peripherals, and this can be used to alter program execution. Peripherals can have one or more interrupts, and all are individually enabled and configured. When an interrupt is enabled and configured, it will generate an interrupt request when the interrupt condition is present. The Programmable Multi-level Interrupt Controller (PMIC) controls the handling and prioritizing of interrupt requests. When an interrupt request is acknowledged by the PMIC, the program counter is set to point to the interrupt vector, and the interrupt handler can be executed.

All peripherals can select between three different priority levels for their interrupts; low, medium and high. Interrupts are prioritized according to their level and their interrupt vector address. Medium level interrupts will interrupt low level interrupt handlers. High level interrupts will interrupt both medium and low level interrupt handlers. Within each level, the interrupt priority is decided from the interrupt vector address, where the lowest interrupt vector address has the highest interrupt priority. Low level interrupts have an optional round-robin scheduling scheme to ensure that all interrupts are serviced within a certain amount of time.

Non-Maskable Interrupts (NMI) is also supported and can be used for critical functions. If a bootloader is used, it is possible to move the interrupt vectors from the Application Section to the Boot Loader Sections so interrupts can be used and executed also during self-programming.

14.3 Interrupt vectors

The interrupt vector is the sum of the peripheral's base interrupt address and the offset address for specific interrupts in each peripheral. The base addresses for the XMEGA A3U devices are shown in Table 14-1. Offset addresses for each interrupt available in the peripheral are described for each peripheral in the XMEGA AU manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in Table 14-1. The program address is the word address.

Table 14-1. Reset and Interrupt Vectors

Program Address (Base Address)	Source	Interrupt Description
0x000	RESET	
0x002	OSCF_INT_vect	Crystal Oscillator Failure Interrupt vector (NMI)
0x004	PORTC_INT_base	Port C Interrupt base

Table 14-1. Reset and Interrupt Vectors (Continued)

Program Address (Base Address)	Source	Interrupt Description
0x008	PORTR_INT_base	Port R Interrupt base
0x00C	DMA_INT_base	DMA Controller Interrupt base
0x014	RTC_INT_base	Real Time Counter Interrupt base
0x018	TWIC_INT_base	Two-Wire Interface on Port C Interrupt base
0x01C	TCC0_INT_base	Timer/Counter 0 on port C Interrupt base
0x028	TCC1_INT_base	Timer/Counter 1 on port C Interrupt base
0x030	SPIC_INT_vect	SPI on port C Interrupt vector
0x032	USARTC0_INT_base	USART 0 on port C Interrupt base
0x03D	USARTC1_INT_base	USART 1 on port C Interrupt base
0x03E	AES_INT_vect	AES Interrupt vector
0x040	NVM_INT_base	Non-Volatile Memory Interrupt base
0x044	PORTB_INT_base	Port B Interrupt base
0x048	ACB_INT_base	Analog Comparator on Port B Interrupt base
0x04E	ADCB_INT_base	Analog to Digital Converter on Port B Interrupt base
0x056	PORTE_INT_base	Port E INT base
0x05A	TWIE_INT_base	Two-Wire Interface on Port E Interrupt base
0x05E	TCE0_INT_base	Timer/Counter 0 on port E Interrupt base
0x06A	TCE1_INT_base	Timer/Counter 1 on port E Interrupt base
0x072	SPIE_INT_vect	SPI on port E Interrupt vector
0x074	USARTE0_INT_base	USART 0 on port E Interrupt base
0x07A	USARTE1_INT_base	USART 1 on port E Interrupt base
0x080	PORTD_INT_base	Port D Interrupt base
0x084	PORTA_INT_base	Port A Interrupt base
0x088	ACA_INT_base	Analog Comparator on Port A Interrupt base
0x08E	ADCA_INT_base	Analog to Digital Converter on Port A Interrupt base
0x09A	TCD0_INT_base	Timer/Counter 0 on port D Interrupt base
0x0A6	TCD1_INT_base	Timer/Counter 1 on port D Interrupt base
0x0AE	SPID_INT_vector	SPI D Interrupt vector
0x0B0	USARTD0_INT_base	USART 0 on port D Interrupt base
0x0B6	USARTD1_INT_base	USART 1 on port D Interrupt base
0x0D0	PORTF_INT_base	Port F Interrupt base
0x0D8	TCF0_INT_base	Timer/Counter 0 on port F Interrupt base
0x0EE	USARTF0_INT_base	USART 0 on port F Interrupt base
0x0FA	USB_INT_base	USB on port D Interrupt base

15. I/O Ports

15.1 Features

- General purpose input and output pins with several and individual configuration options
- Output driver with configurable driver and pull settings:
  - Totem-pole
  - Wired-AND
  - Wired-OR
  - Bus-keeper
  - Inverted I/O
- Input with synchronous and/or asynchronous sensing with port interrupts and events
  - Sense both edges
  - Sense rising edges
  - Sense falling edges
  - Sense low level
- Optimal pull-up and pull-down resistor on input and Wired-OR/AND configurations
- Optional slew rate control
- Asynchronous pin change sensing that can wake-up the device from all sleep modes
- Two port interrupts with pin masking per I/O port
- Efficient and safe access to port pins
  - Hardware read-modify-write through dedicated Toggle/Clear/Set registers
  - Configuration of multiple pins in a single operation
  - Mapping of port registers into bit-accessible I/O memory space
- Peripheral Clocks output on port pin
- Real Time Counter Clock output to port pin
- Event Channel output on port pin
- Remap of digital peripheral pin functions
  - Selectable USART, SPI and Timer/Counter input/output pin locations

15.2 Overview

One port consists of up to 8 pins ranging from pin 0 to 7. Each port pin can be configured as input or output with configurable driver and pull settings. They also implement synchronous and asynchronous input sensing with interrupts and events for selectable pin change conditions. Asynchronous pin-change sensing means that a pin change can wake the device from all sleep modes, included the modes where no clocks are running.

All functions are individual and configurable per pin, but several pins can be configured in one single operation. The pins have hardware Read-Modify-Write (RMW) functionality for safe and correct change of drive value and/or pull resistor configuration. The direction of one port pin can be changed without unintentionally changing the direction of any other pin.

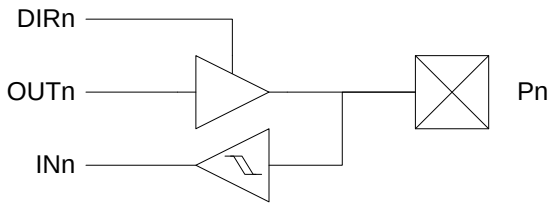
The port pin configuration also controls input and output selection of other device function. It is possible to have both the peripheral clock and the real time clock output to a port pin, and available for external use. The same applies to events from the Event System that can be used to synchronize and control external functions. Other digital peripherals such as USART, SPI and Timer/Counters can be remapped to selectable pin location in order to optimize pinout versus application needs.

15.3 Output Driver

All port pins (Pn) have programmable output configuration. The port pins also have configurable slew rate limitation to reduce electromagnetic emission.

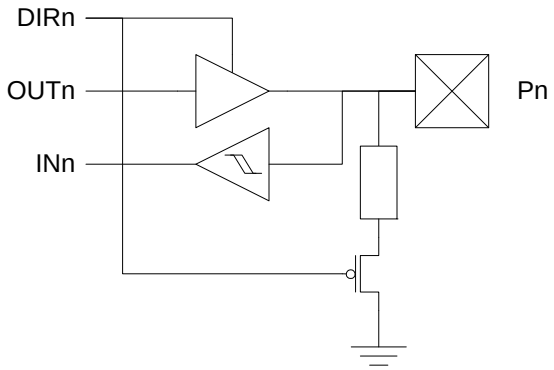
15.3.1 Push-pull

Figure 15-1. I/O configuration - Totem-pole



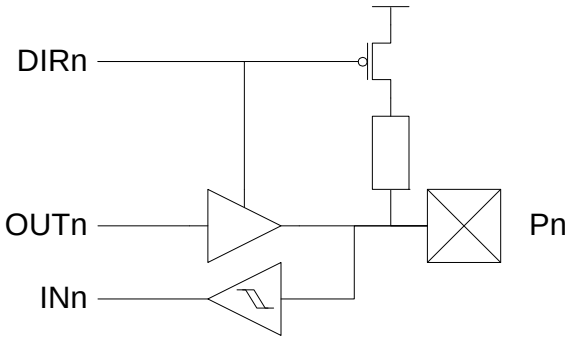
15.3.2 Pull-down

Figure 15-2. I/O configuration - Totem-pole with pull-down (on input)



15.3.3 Pull-up

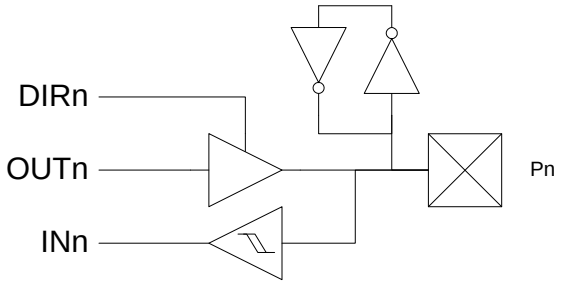
Figure 15-3. I/O configuration - Totem-pole with pull-up (on input)



15.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

Figure 15-4. I/O configuration - Totem-pole with bus-keeper



15.3.5 Others

Figure 15-5. Output configuration - Wired-OR with optional pull-down

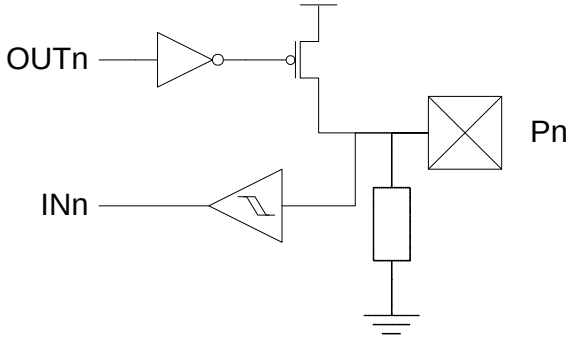
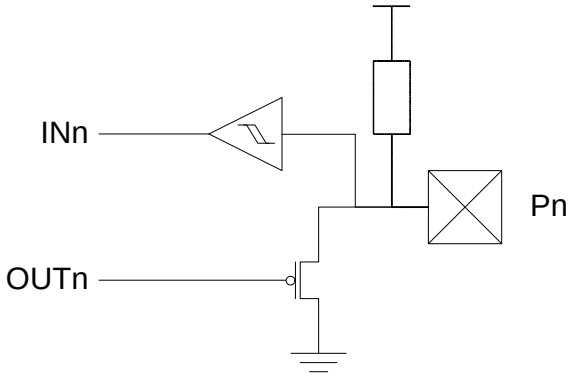


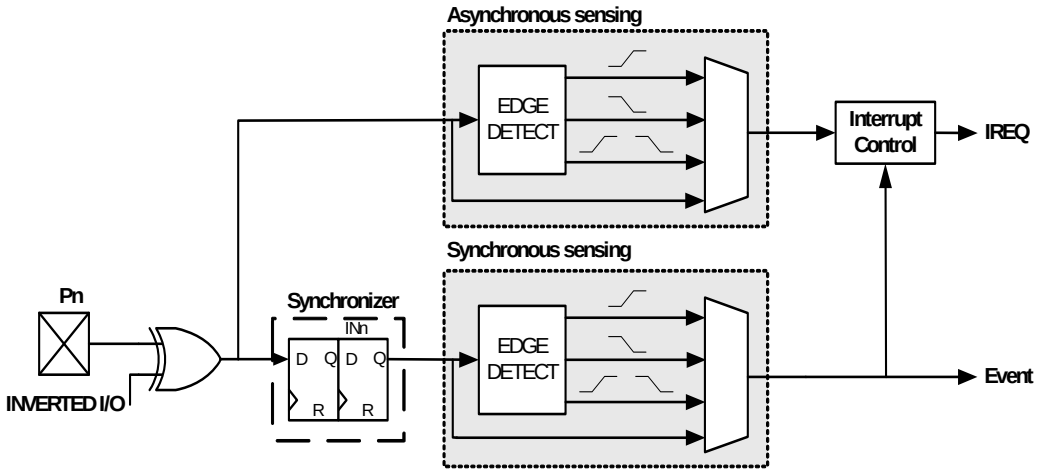
Figure 15-6. I/O configuration - Wired-AND with optional pull-up



15.4 Input sensing

Input sensing is synchronous or asynchronous depending on the enabled clock for the ports, and the configuration is shown in Figure 15-7 on page 31.

Figure 15-7. Input sensing system overview



When a pin is configured with inverted I/O, the pin value is inverted before the input sensing.

15.5 Alternate Port Functions

In addition to the input/output functions on all port pins, most pins have alternate functions. This means that other modules or peripherals connected to the port can use the port pins for their functions, such as communication or pulse-width modulation. ”Pinout and Pin Functions” on page 51 shows which modules on peripherals that enable alternate functions on a pin, and which alternate functions that are available on a pin.

16. T/C - 16-bit Timer/Counter

16.1 Features

- Seven 16-bit Timer/Counters
  - Four Timer/Counters of type 0
  - Three Timer/Counters of type 1
- 32-bit Timer/Counter support by cascading two Timer/Counters
- Up to 4 Compare or Capture (CC) Channels
  - 4 CC Channels for Timer/Counters of type 0
  - 2 CC Channels for Timer/Counters of type 1
- Double Buffered timer period setting
- Double Buffered Capture or Compare Channels
- Waveform Generation:
  - Frequency Generation
  - Single Slope Pulse Width Modulation
  - Dual Slope Pulse Width Modulation
- Input Capture:
  - Input Capture with noise cancelling
  - Frequency capture
  - Pulse width capture
  - 32-bit input capture
- Timer Overflow and Error interrupts / events
- One Compare Match or Input Capture interrupt / event per CC Channel
- Can be used with Event System for
  - Quadrature Decoding
  - Count and direction control
  - Capture
- Can be used with DMA and trigger DMA transactions
- High-Resolution Extension
  - Increases frequency and waveform resolution by 4x (2-bit), or 8x (3-bit)
- Advanced Waveform Extension
  - Low and High-side output with programmable Dead-Time Insertion (DTI)
- Event controlled fault protection for safe disabling of external drivers

16.2 Overview

There are seven flexible 16-bit Timer/Counters (TC). Their capabilities include accurate program execution timing, frequency and waveform generation, and input capture with time and frequency measurement of digital signals. Two Timer/Counters can be cascaded to create 32-bit Timer/Counter with optional 32-bit capture.

A Timer/Counter consists of a Base Counter and a set of Compare or Capture (CC) channels. The Base Counter can be used to count clock cycles or events. It has direction control and period setting that can be used for timing. The CC channels can be used together with the Base Counter to do compare match control, frequency generation and pulse width waveform modulation, or various input capture operations. A Timer/Counter can be configured for either capture or compare functions, and not perform both at the same time.

A Timer/Counter can be clocked and timed from the Peripheral Clock with optional prescaling or the Event System. The Event System can also be used for direction control, capture trigger or to synchronize operations.

Figure 16-1. Overview of a Timer/Counter and closely related peripherals

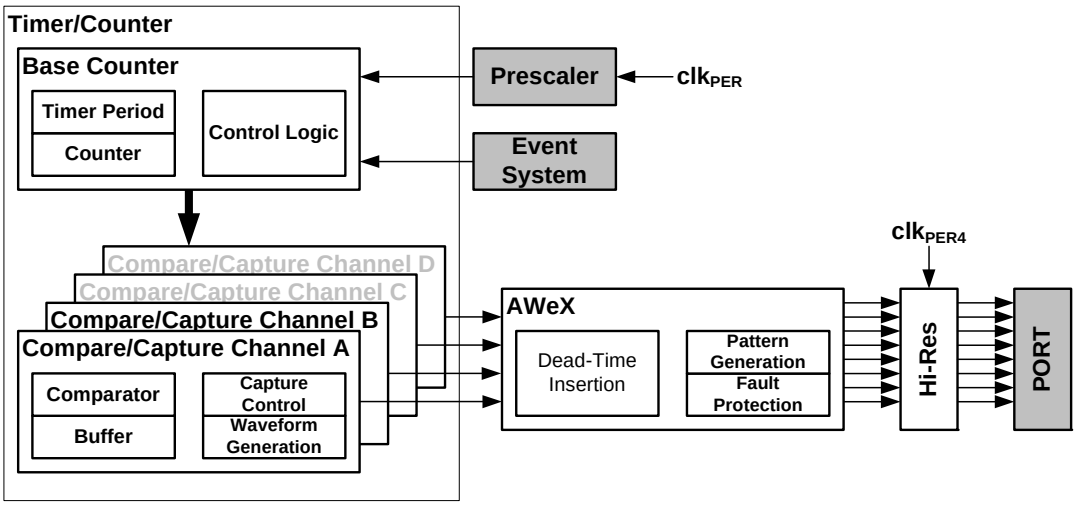


Figure 16-2. Overview of a Timer/Counter and closely related peripherals

The only difference between Timer/Counter type 0 and 1 is the number of CC Channels. Timer/Counter 0 has four CC channels, and Timer/Counter 1 has two CC channels. All information related to CC channel 3 and 4 is only valid for Timer/Counter 0.

The High Resolution (Hi-Res) extension can be used to increase the waveform output resolution by up to eight times, by using internal clock source running up to four times faster than the Peripheral Clock. See ”Hi-Res - High Resolution Extension” on page 35 for more details.

The Advanced Waveform Extension can be enabled to provide extra and more advanced features for the Timer/Counter. This are only available for Timer/Counter 0. See ”AWeX - Advanced Waveform Extension” on page 34 for more details.

PORTC, PORTD and PORTE each has one Timer/Counter 0 and one Timer/Counter1. PORTF has one Timer/Counter 0. Notation of these are TCC0 (Time/Counter C0), TCC1, TCD0, TCD1, TCE0, TCE1 and TCF0, respectively.

17. AWeX - Advanced Waveform Extension

17.1 Features

- **Wafeform output with complementary output from each Compare channel**
- **4 Dead-Time Insertion (DTI) Units**
  - **8-bit Resolution**
  - **Separate High and Low Side Dead-Time Setting**
  - **Double Buffered Dead-Time**
  - **Optionally halts Timer during Dead-Time Insertion**
- **Pattern Generation unit creating synchronised bit pattern across the port pins**
  - **Double buffered pattern generation**
  - **Optionally distribution of one Compare channel output across the port pins**
- **Event controlled Fault Protection for instant and predictably fault triggering**

17.2 Overview

The Advanced Waveform Extension (AWeX) provides extra functions to the Timer/Counter in Waveform Generation (WG) modes. It is primarily intended for different types of motor control and other power control applications. It enables Low- and High Side output with Dead Time Insertion, and fault protection for disabling and shutdown of drivers. It can also generate a synchronized bit pattern across the port pins.

Each of the waveform generator outputs from the Timer/Counter 0 are split into a complimentary pair of outputs when any AWeX features are enabled. These output pairs go through a Dead-Time Insertion (DTI) unit that generates the non-inverted Low Side (LS) and inverted High Side (HS) of the WG output with dead time insertion between LS and HS switching. The DTI output will override the normal port value according to the port override setting.

The Pattern Generation unit can be used to generate a synchronized bit pattern across the port it is connected to. In addition, the WG output from the Compare Channel A can be distributed to and override all the port pins. When the Pattern Generator unit is enabled the DTI unit is bypassed.

The Fault Protection unit is connected to the Event System, enabling any event to trigger a fault condition that will disable the AWeX output. The Event System ensure predictable and instant fault reaction, and gives great flexibility in the selection of fault triggers.

The AWEX is available for TCC0. The notation of this is AWEXC.

18. Hi-Res - High Resolution Extension

18.1 Features

- **Increases Waveform Generator resolution by up to 8 times (3-bit)**
- **Supports Frequency, Single Slope PWM and Dual Slope PWM generation**
- **Supports the AWEX when this is used for the same Timer/Counter**

18.2 Overview

The Hi-Resolution (Hi-Res) Extension is able to increase the resolution of the waveform generation output by a factor of four or eight. It can be used for a Timer/Counter doing Frequency, Single Slope PWM or Dual Slope PWM generation. It can also be used with the AWeX if this is used for the same Timer/Counter.

Atmel® AVR® XMEGA® A3U devices have four Hi-Res Extensions that each can be enabled for each Timer/Counters pair on PORTC, PORTD, PORTE and PORTF. The notation of these are HIRESC, HIRESD, HIRESE and HIRESF, respectively.

19. RTC - 16-bit Real-Time Counter

19.1 Features

- 16-bit resolution
- Selectable clock source
  - 32.768kHz external crystal
  - External clock
  - 32.768kHz internal oscillator
  - 32kHz internal ULP oscillator
- Programmable 10-bit clock prescaling
- One Compare register
- One Period register
- Clear Counter on period overflow
- Optional Interrupt/ Event on overflow and compare match

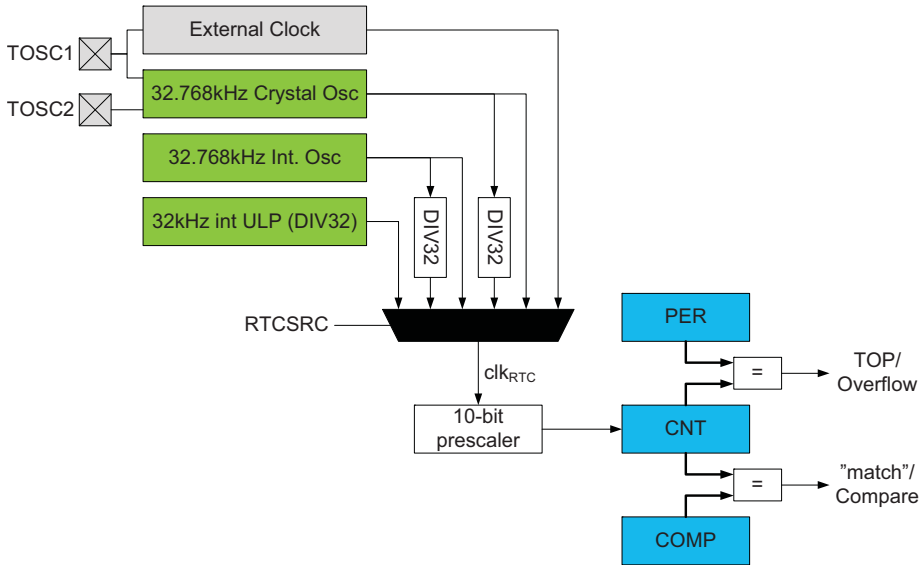
19.2 Overview

The 16-bit Real Time Counter (RTC) is a counter that typically runs continuously, including in low power sleep modes, to keep track of time. It can wake up the device from sleep modes and/or interrupt the device at regular intervals.

The reference clock is typically the 1.024kHz output from a high accuracy crystal of 32.768kHz, and this is the configuration most optimized for low power consumption. The faster 32.768kHz output can be selected if the RTC needs a higher resolution than 1mS. The RTC can also be clocked from an external clock signal, the internal 32.768kHz oscillator or the internal 32kHz ULP oscillator.

The RTC includes a 10-bit programmable prescaler that can scale down the reference clock before it reaches the Counter. A wide range of resolution and time-out periods can be configured. With a 32.768kHz clock source the maximum resolution of 30.5µs, time-out periods range up to 2000seconds. With a resolution of 1 second, the maximum time-out period is over 18hours (65536seconds). The RTC can give a compare interrupt and/or event when the counter equals the Compare register value, and an overflow interrupt and/event when it equals the Period register value.

Figure 19-1. Real-time Counter overview



20. USB - Universal Serial Bus Interface

20.1 Features

- One USB 2.0 full speed (12Mbps) and low speed (1.5Mbps) device compliant interface
- Integrated on-chip USB transceiver, no external components needed
- 16 endpoint addresses with full endpoint flexibility for up to 32 endpoints
  - One input endpoint per endpoint address
  - One output endpoint per endpoint address
- Endpoint address transfer type selectable to
  - Control transfers
  - Interrupt transfers
  - Bulk transfers
  - Isochronous transfers
- Configurable data payload size per endpoint, up to 1023bytes
- Endpoint configuration and data buffers located in internal SRAM
  - Configurable location for endpoint configuration data
  - Configurable location for each endpoint's data buffer
- Built in Direct Memory Access (DMA) to internal SRAM for
  - Endpoint configurations
  - Read and write of endpoint data
- Ping-Pong operation for higher throughput and double buffered operation
  - Input and output endpoint data buffers used in a single direction
  - CPU/DMA controller can update data buffer during transfer
- Multi-Packet transfer for reduced interrupt load and software intervention
  - Data payload exceeding max packet size is transferred in one continuous transfer
  - No interrupts or software interaction on packet transaction level
- Transaction Complete FIFO for easy flow management when using multiple endpoints
  - Tracks all completed transactions in a first come, first serve work-queue
- Clock selection independent of System Clock source selection
- Connection to Event System
- On chip debug possibilities during USB transactions

20.2 Overview

The USB interface is an USB 2.0 full speed (12Mbps) and low speed (1.5Mbps) device compliant interface.

It supports 16 endpoint addresses. All endpoint addresses have one input and one output endpoint, for a total of 32 endpoints. Each endpoint address is fully configurable and can be configured for any of the four transfer types: control, interrupt, bulk or isochronous. The data payload size is also selectable and it supports data payloads up to 1023bytes.

No dedicated memory is allocated for or included in the USB module. Internal SRAM is used to keep the configuration for each endpoint address, and the data buffer for each endpoint. The memory locations used for endpoint configurations and data buffers are fully configurable. The amount of memory allocated is fully dynamic according to the number of endpoints in use, and the configuration of these. The USB module has built-in Direct Memory Access (DMA) and will read/write data from/to the SRAM when a USB transaction takes place.

To maximise throughput, an endpoint address can be configured for Ping-Pong operation. When this is done, the input and output endpoints are both used in the same direction. The CPU or

DMA Controller can then read/write one data buffer while the USB module writes/reads the other, and vice versa. This gives double buffered communication.

Multi-packet transfer enables a data payload exceeding the maximum packet size of an end-pointto be transferred as multiple packets without software intervention. This reduce the CPU intervention and the interrupts needed for USB transfers.

For low power operation, the USB module can put the microcontroller in any sleep mode when the USB bus is idle and a suspend condition is given. Upon bus resume, the USB module can wake the microcontroller from any sleep mode.

PORTD has one USB. Notation of this is USBD.

21. TWI - Two Wire Interface

21.1 Features

- **Two Identical Two Wire Interface peripherals**
- **Bi-directional two-wire communication interface**
  - **Phillips I^2C compatible**
  - **System Management Bus (SMBus) compatible**
- **Bus master and slave operation supported**
  - **Slave operation**
  - **Single bus master operation**
  - **Bus master in multi-master bus environment**
  - **Multi-master arbitration**
- **Flexible slave address match functions**
  - **7-bit and General Call Address Recognition in Hardware**
  - **10-bit addressing supported**
  - **Address mask register for dual address match or address range masking**
  - **Optional software address recognition for unlimited number of addresses**
- **Slave can operate in all sleep modes**
- **Slave address match can wake device from all sleep modes**
- **100kHz and 400kHz bus frequency support**
- **Slew-rate limited output drivers**
- **Input filter for bus noise and spike suppression**
- **Support arbitration between START/Repeated START and Data Bit (SMBus)**
- **Slave arbitration allows support for Address Resolve Protocol (ARP) (SMBus)**

21.2 Overview

The Two Wire Interface is a bi-directional two-wire communication interface. It is I^2C and System Management Bus (SMBus) compatible. The only external hardware needed to implement the bus is one pull-up resistor on each bus line.

The TWI module supports master and slave functionality. The master and slave functionality are separated from each other and can be enabled and configured separately. The master module supports multi-master bus operation and arbitration. It contains the baud rate generator. Both 100kHz and 400kHz bus frequency is supported.

The slave module implements 7-bit address match and general address call recognition in hardware. 10-bit addressing is also supported. A dedicated address mask register can act as a second address match register or as a register for address range masking. The slave continues to operate in all sleep modes, including Power down mode. This enables the slave to wake up the device from all sleep modes on TWI address match. It is possible to disable the address matching to let this be handled in software instead. Smart Mode can be enabled to auto trigger operations and reduce software complexity.

The TWI module will detect START and STOP conditions, bus collision and bus errors. Arbitration lost, errors, collision and clock hold on the bus is also detected and indicated in separate status flags available in both master and slave mode.

It is possible to disable the TWI drivers in the device, and enable a 4-wire digital interface for connecting to an external TWI bus driver. This can be used for applications where the device operates from a different VCC voltage than used by the TWI bus.

PORTC and PORTE each has one TWI. Notation of these peripherals are TWIC and TWIE.

22. SPI - Serial Peripheral Interface

22.1 Features

- **Three Identical SPI peripherals**
- **Full-duplex, Three-wire Synchronous Data Transfer**
- **Master or Slave Operation**
- **LSB First or MSB First Data Transfer**
- **Seven Programmable Bit Rates**
- **Interrupt Flag at the End of Transmission**
- **Write collision flag to indicate data collision**
- **Wake-up from Idle Mode**
- **Double Speed Master Mode**

22.2 Overview

The Serial Peripheral Interface (SPI) is a high-speed synchronous data transfer interface using three or four pins. It allows fast communication between an XMEGA device and peripheral devices or other microcontrollers. The SPI supports full duplex communication.

A device connected to the bus must act as a master or slave. The master initiates and controls all data transactions, and data is transferred both to and from the device simultaneously.

PORTC, PORTD, and PORTE each has one SPI. Notation of these peripherals are SPIC, SPID, and SPIE respectively.

23. USART

23.1 Features

- Seven Identical USART peripherals
- Full Duplex Operation
- Asynchronous or Synchronous Operation
  - Synchronous clock rates up to 1/2 o the device clock frequency
  - Asynchronous clock rates up to 1/8 of the device clock frequency
- Supports Serial Frames with 5, 6, 7, 8, or 9 Data Bits and 1 or 2 Stop Bits
- Fractional Baud Rate Generator
  - Can generate desired baud rate from any system clock frequency
  - No need for external oscillator with certain frequencies
- Built in error detection and correction schemes
  - Odd or Even Parity Generation and Parity Check
  - Data Over Run and Framing Error Detection
  - Noise Filtering Includes False Start Bit Detection and Digital Low Pass Filter
- Separate Interrupts for
  - Transmit Complete
  - Transmit Data Register Empty
  - Receive Complete
- Multi-Processor Communication Mode
  - Addressing scheme to address a specific devices on a multi-device bus
  - Enable unaddressed devices to automatically ignore all frames
- Master SPI Mode
  - Double Buffered Operation
  - Configurable Data Order
  - High Speed Operation up to 1/2 of the peripheral clock frequency
- IRCOM Module for IrDA compliant pulse modulation/demodulation

23.2 Overview

The Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a fast and flexible serial communication module. The USART supports full duplex communication, and both asynchronous and clocked synchronous operation. The USART can also be set in Master SPI mode and be used for SPI communication.

Communication is frame based, and the frame format can be customized to support a wide range of standards. The USART is buffered in both direction, enabling continued data transmission without any delay between frames. There are separate interrupts for receive and transmit complete, enabling fully interrupt driven communication. Frame error and buffer overflow are detected in hardware and indicated with separate status flags. Even or odd parity generation and parity check can also be enabled.

The Clock Generation logic has a fractional baud rate generator that is able to generate a wide range of USART baud rates from any system clock frequencies. This remove the need to use an external crystal oscillator with a certain frequency in order to achieve a required baud rate. It also includes support external clock input in synchronous slave operation.

One USART can use the IRCOM module to support IrDA 1.4 physical compliant pulse modulation and demodulation for baud rates up to 115.2kbps.

PORTC, PORTD, and PORTE each has two USARTs, while PORTF has one USART only. Notation of these peripherals are USARTC0, USARTC1, USARTD0, USARTD1, USARTE0, USARTE1 and USARTF0, respectively.

24. IRCOM - IR Communication Module

24.1 Features

- **Pulse modulation/demodulation for infrared communication**
- **IrDA Compatible for baud rates up to 115.2kbps**
- **Selectable pulse modulation scheme**
  - **3/16 of baud rate period**
  - **Fixed pulse period, 8-bit programmable**
  - **Pulse modulation disabled**
- **Built in filtering**
- **Can be connected to and used by one USART at a time**

24.2 Overview

The Infrared Communication Module (IRCOM) is used for IrDA communication with baud rates up to 115.2kbps. There is one IRCOM available which can be connected to any USART to enable infrared pulse coding/decoding for that USART.

25. AES and DES Crypto Engine

25.1 Features

- **Data Encryption Standard (DES) CPU instruction**
- **Advanced Encryption Standard (AES) Crypto module**
- **DES Instruction**
  - **Encryption and Decryption**
  - **Single-cycle DES instruction**
  - **Encryption/Decryption in 16 clock cycles per 8-byte block**
- **AES Crypto Module**
  - **Encryption and Decryption**
  - **Support 128-bit keys**
  - **Support XOR data load mode to the State memory for Cipher Block Chaining**
  - **Encryption/Decryption in 375 clock cycles per 16-byte block**

25.2 Overview

The Advanced Encryption Standard (AES) and Data Encryption Standard (DES) are two commonly used standards for cryptography. These are supported through an AES peripheral module and a DES CPU instruction, and the communication interfaces and the CPU can use these for fast encrypted communication and secure data storage.

DES is supported by an instruction in the AVR CPU. The 8-byte key and 8-byte data blocks must be loaded into the Register file, and then the DES instruction must be executed 16 times to encrypt/decrypt the data block.

The AES Crypto Module encrypts and decrypts 128-bit data blocks with the use of a 128-bit key. The key and data must be loaded into the key and state memory in the module before encryption/ decryption is started. It takes 375 Peripheral clock cycles before the encryption/decryption is done. The encrypted/encrypted data can then be read out, and an optional interrupt can be generated. The AES Crypto Module also has DMA support with transfer triggers when encryption/decryption is done and optional auto-start of encryption/decryption when the state memory is fully loaded.

26. CRC - Cyclic Redundancy Check Generator

26.1 Features

- **Cyclic Redundancy Check (CRC) Generation and Checking for**
  - **Communication Data**
  - **Program or Data in Flash memory**
  - **Data in SRAM memory and I/O memory space**
- **Integrated with Flash memory, DMA Controller and CPU**
  - **Continuous CRC on data going through a DMA Channel**
  - **Automatic CRC of the complete, or selectable range of the Flash memory**
  - **CPU can load data to CRC Generator through I/O interface**
- **CRC polynomial software selectable to**
  - **CRC-16 (CRC-CCITT)**
  - **CRC-32 (IEEE 802.3)**
- **Zero remainder detection**

26.2 Overview

A Cyclic Redundancy Check (CRC) is a test algorithm used to detect accidental errors on data, and is commonly used to determine the correctness of a data transmission, data memory and program memory. A CRC takes a data stream or block of data as input and generates a 16- or 32-bit output that can be kept with the data and used as checksum. When the same data is later received or read, the device or application repeats the calculation. If the new CRC calculation does not match the one calculated earlier, the block contains a data error. The application will then detect this and may take corrective action such as requesting the data to be sent again.

Typically, an n-bit CRC, applied to a data block of arbitrary length, will detect any single error burst not longer than n bits (in other words, any single alteration that spans no more than n bits of the data), and will detect a fraction $1-2^{-n}$ of all longer error bursts.The CRC module in XMEGA supports two commonly used CRC polynomials; CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3).

- **CRC-16:**

Polynomial:	$x^{16}+x^{12}+x^5+1$
Hex value:	0x1021

- **CRC-32:**

Polynomial:	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$
Hex value:	0x04C11DB7

27. ADC - 12-bit Analog to Digital Converter

27.1 Features

- Two Analog to Digital Converters
- 12-bit resolution
- Up to 2 Million Samples Per Second
  - 4 inputs can be sampled within 1.5µs
  - Down to 2.5µs conversion time with 8-bit resolution
  - Down to 3.5µs conversion time with 12-bit resolution
- Differential and Single-ended input
  - Up to 16 single-ended inputs
  - 16x4 differential inputs without gain
  - 16x4 differential input with gain
- Built in differential gain stage
  - 1/2x, 1x, 2x, 4x, 8x, 16x, 32x and 64x gain options
- Single, continues and scan conversion options
- 4 internal inputs
  - Internal Temperature sensor
  - DAC Output
  - VCC voltage divided by 10
  - 1.1V Bandgap voltage
- 4 conversion channels with individual input control and result registers
  - Enable 4 parallel configurations and results
- Internal and external reference options
- Compare function for accurate monitoring of user defined thresholds
- Optional event triggered conversion for accurate timing
- Optional DMA transfer of conversion results
- Optional interrupt/event on compare result

27.2 Overview

There are two Analog to Digital Converters (ADCs) modules that can be operated simultaneously, individually or synchronized.

The ADC converts analog signals to digital values. The ADC has 12-bit resolution and is capable of converting up to 2Million Samples Per Second (MSPS). The input selection is flexible, and both single-ended and differential measurements can be done. For differential measurements an optional gain stage is available to increase the dynamic range. In addition several internal signal inputs are available. The ADC can provide both signed and unsigned results.

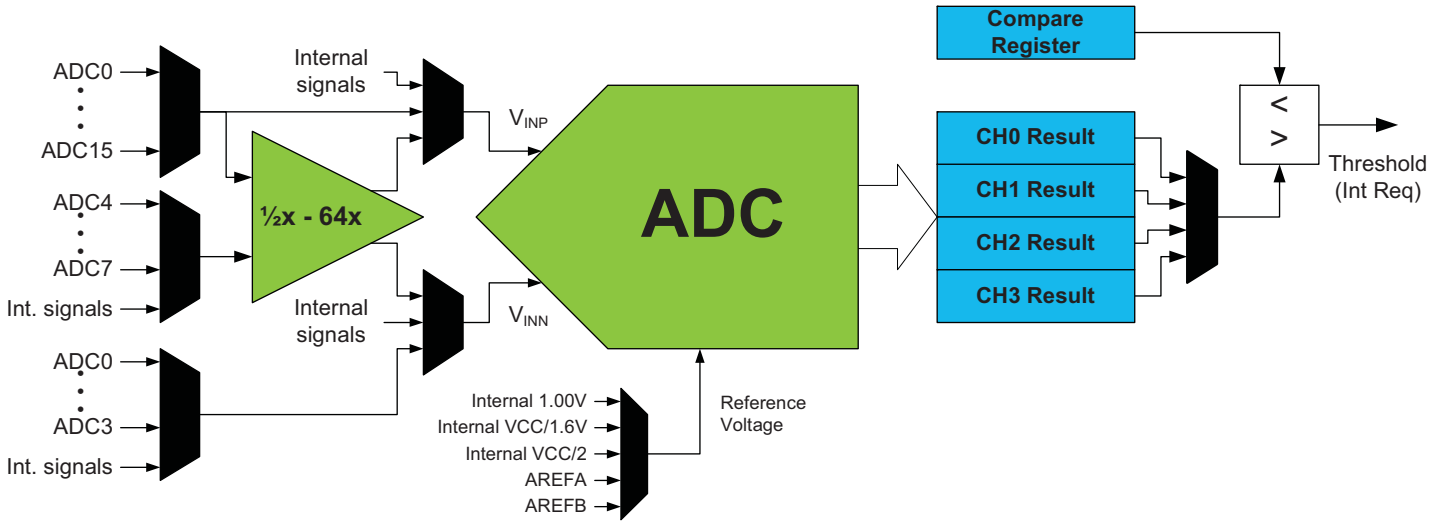
This is a pipelined ADC that consists of several consecutive stages. The pipelined design allows high sample rate at a low System Clock frequency. It also means that a new input can be sampled and a new ADC conversion started while other ADC conversions are still ongoing. This remove dependencies between sample rate and propagation delay.

The ADC has four conversion channels (Channel 0-3) with individual input selection, result registers and conversion start control. The ADC can then keep and use four parallel configurations and results, and this will ease use for applications with high data throughput or multiple modules using the ADC independently. It is possible to use DMA to move ADC results directly to memory or peripherals when conversions are done.

Both internal and external reference voltages can be used. An integrated temperature sensor is available for use with the ADC. The output from the DAC, VCC/10 and the Bandgap voltage can also be measured by the ADC.

The ADC has a compare function for accurate monitoring of user defined thresholds with minimum software intervention required.

Figure 27-1. ADC overview



Four inputs can be sampled within 1.5µs without any intervention by the application.

The ADC may be configured for 8- or 12-bit result, reducing the minimum conversion time (propagation delay) from 3.5µs for 12-bit to 2.5µs for 8-bit result.

ADC conversion results are provided left- or right adjusted with optional ‘1’ or ‘0’ padding. This eases calculation when the result is represented as a signed integer (signed 16-bit number).

PORTA and PORTB each has one ADC. Notation of these peripherals are ADCA and ADCB, respectively.

28. DAC - 12-bit Digital to Analog Converter

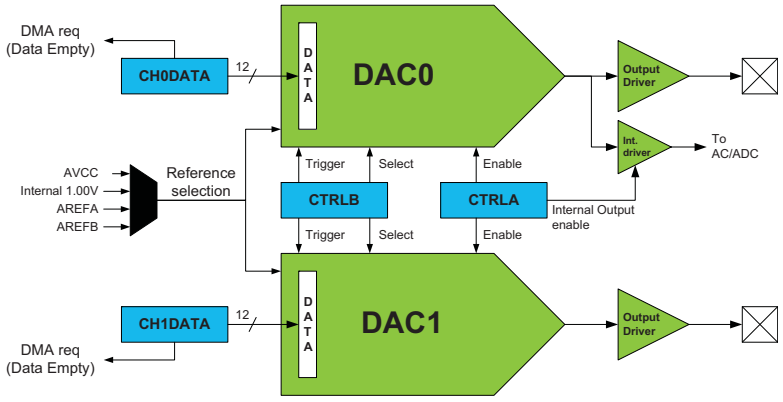
28.1 Features

- One Digital to Analog Converter (DAC)
- 12-bit resolution
- Up to 1Million Samples Per Second conversion rate per DAC channel
- Built in calibration that removes
  - Offset error
  - Gain error
- Multiple conversion trigger sources
  - On new available data
  - Events from the Event System
- High drive capabilities and support for
  - Resistive load
  - Capacitive load
  - Combined resistive and capacitive load
- Internal and external reference options
- DAC output available as input to Analog Comparator and ADC
- Low Power mode with reduced drive strength
- Optional DMA transfer of data

28.2 Overview

The Digital to Analog Converter (DAC) converts digital values to voltages. Each DAC has two channels, 12-bit resolution, and is capable of converting 1Million Samples Per Second (MSPS) on each channels. The built-in calibration system can remove offset and gain error when loaded with calibration values from software.

Figure 28-1. DAC overview



A DAC conversion is automatically started when new data to be converted is available. Event from the Event System can also be used, and this enable synchronized and timed conversions between the DAC and other peripherals such as a Timer/Counter. The DMA Controller can be used to transfer data to the DAC.

The DAC has high drive strengths and is capable of driving both resistive and capacitive loads, and a load which is a combination of this. A low power mode is available, and this will reduce the drive strengths of the output. Both internal and external voltage reference can be used. The DAC output is also internally available for use as input to the Analog Comparator or ADC.

PORTB each has one DAC. Notation of this peripheral is DACB.

29. AC - Analog Comparator

29.1 Features

- **Four Analog Comparators**
- **Selectable propagation delay vs current consumption**
- **Selectable hysteresis**
  - **No**
  - **Small**
  - **Large**
- **Analog Comparator output available on pin**
- **Flexible Input Selection**
  - **All pins on the port**
  - **Output from the DAC**
  - **Bandgap reference voltage.**
  - **A 64-level programmable voltage scaler of the internal VCC voltage**
- **Interrupt and event generation on**
  - **Rising edge**
  - **Falling edge**
  - **Toggle**
- **Window function interrupt and event generation on**
  - **Signal above window**
  - **Signal inside window**
  - **Signal below window**
- **Constant current source with configurable output pin selection**

29.2 Overview

The Analog Comparator (AC) compares the voltage level on two inputs and gives a digital output based on this comparison. The Analog Comparator may be configured to give interrupt requests and/or events upon several different combinations of input change.

Two important properties of the Analog Comparator when it comes to the dynamic behavior, are hysteresis and propagation delay. Both these parameters may be adjusted in order to find the optimal operation for each application.

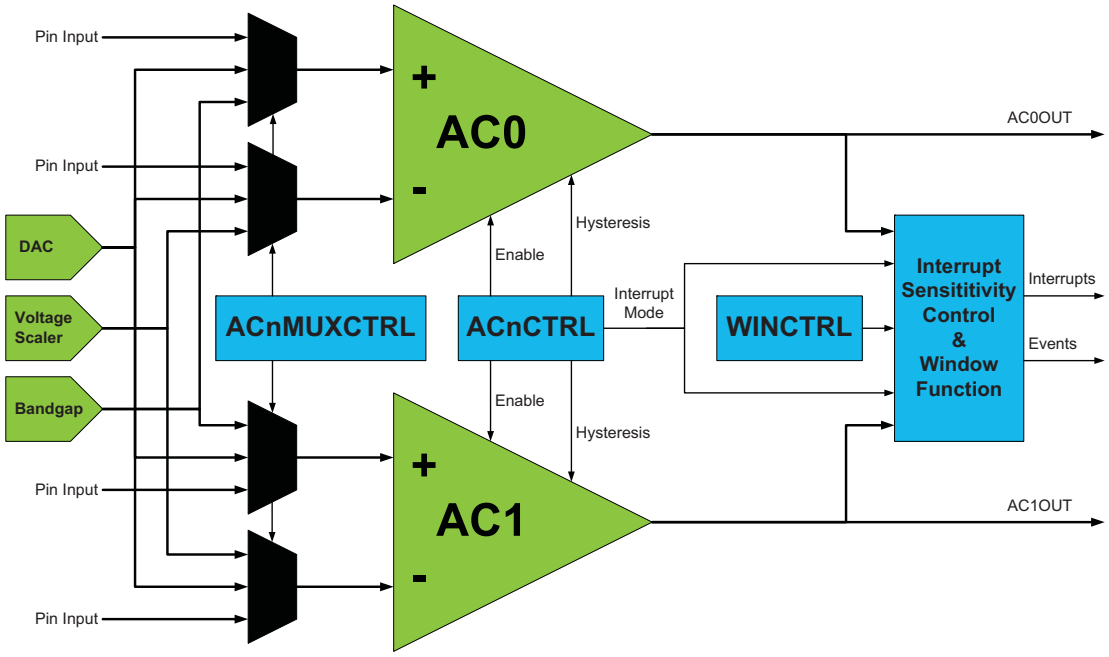
The input section includes analog port pins, several internal signals and a 64-level programmable voltage scaler. The analog comparator output state can also be directly available on a pin for use by external devices. Using as pair they can also be set in Window mode to monitor a signal compared to a voltage window instead of a voltage level.

A constant current source can be enabled, and output on a selectable pin. This can be used to replace for example external resistors used to charge capacitors in capacitive touch sensing applications.

The Analog Comparators are always grouped in pairs on each port. They have identical behavior but separate control registers.

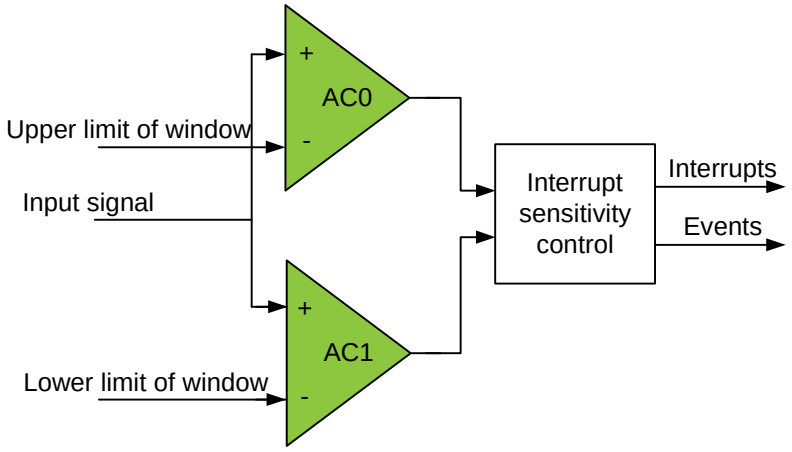
PORTA and PORTB each has one AC pair. Notations are ACA and ACB, respectively.

Figure 29-1. Analog comparator overview



The window function is realized by connecting the external inputs of the two analog comparators in a pair as shown in Figure 29-2..

Figure 29-2. Analog comparator window function



30. Programming and Debugging

30.1 Features

- **Programming**
  - **External programming through the PDI or JTAG interface**
    - **Minimal protocol overhead for fast operation**
    - **Built in error detection and handling for reliable operation**
  - **Bootloader support for programming through any communication interface**
- **Debugging**
  - **Non-Intrusive Real-Time On-Chip Debug System**
  - **No software or hardware resources required from device expect pin connection**
  - **Program Flow Control**
    - **Go, Stop, Reset, Step into, Step over, Step out, Run-to-Cursor**
  - **Unlimited Number of User Program Breakpoints**
  - **Unlimited Number of User Data Breakpoints, break on:**
    - **Data location read, write or both read and write**
    - **Data location content equal or not equal to a value**
    - **Data location content is greater or smaller than a value**
    - **Data location content is within or outside a range**
  - **No limitation on device clock frequency**
- **Program and Debug Interface (PDI)**
  - **2-pin interface for external programming and debugging**
  - **Uses the Reset pin and a dedicated pin**
  - **No I/O pins required during programming or debugging**
- **JTAG Interface**
  - **4-pin IEEE std. 1149.1 compliant interface for programming and debugging**
  - **Boundary-scan capabilities According to the IEEE std. 1149.1 (JTAG) Standard**

30.2 Overview

Atmel® AVR® XMEGA® devices together with Atmel's development tool chain include the necessary functions for efficient development. All external programming and debugging are done through the Program and Debug Interface (PDI), or the JTAG interface.

The Program and Debug Interface is 2-pin interface that uses the Reset pin and a dedicated pin. No I/O pins are required during programming or debugging.

The JTAG Interface is a 4-pin IEEE std. 1149.1 compliant interface. This also has Boundary-scan capabilities according to the IEEE std. 1149.1 (JTAG) Standard

In addition to the PDI and JTAG interface, programming can also be done through a bootloader. A bootloader in the device can use any other communication interface such as UART, TWI or SPI to download and program new application code to the Flash memory.

Debug is supported through a on-chip debug system that offers Non-Intrusive Real-Time debug. It does not require any software or hardware resources expect for the device expect pin connection. Using Atmel's tool chain, it offers complete program flow control and has supported for unlimited number of program and complex data breakpoints. Application debug can be done from C and high level language source code level, as well as assembler and disassembler level.

31. Pinout and Pin Functions

The device pinout is shown in ”Pinout/Block Diagram” on page 3. In addition to general purpose I/O functionality, each pin can have several alternate functions. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the pin functions can be used at time.

31.1 Alternate Pin Function Description

The tables below show the notation for all pin functions available and describe its function.

31.1.1 Operation/Power Supply

VCC	Digital supply voltage
AVCC	Analog supply voltage
GND	Ground

31.1.2 Port Interrupt functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNC	Port pin with full synchronous and full asynchronous interrupt function

31.1.3 Analog functions

ACn	Analog Comparator input pin n
ACnOUT	Analog Comparator n Output
ADCn	Analog to Digital Converter input pin n
DACn	Digital to Analog Converter output pin n
AREF	Analog Reference input pin

31.1.4 Timer/Counter and AWEX functions

OCnxLS	Output Compare Channel x Low Side for Timer/Counter n
OCnxHS	Output Compare Channel x High Side for Timer/Counter n

31.1.5 Communication functions

SCL	Serial Clock for TWI
SDA	Serial Data for TWI
SCLIN	Serial Clock In for TWI when external driver interface is enabled
SCLOUT	Serial Clock Out for TWI when external driver interface is enabled
SDAIN	Serial Data In for TWI when external driver interface is enabled
SDAOUT	Serial Data Out for TWI when external driver interface is enabled
XCKn	Transfer Clock for USART n
RXDn	Receiver Data for USART n
TXDn	Transmitter Data for USART n
$\overline{SS}$	Slave Select for SPI
MOSI	Master Out Slave In for SPI
MISO	Master In Slave Out for SPI
SCK	Serial Clock for SPI
D-	Data- for USB
D+	Data+ for USB

31.1.6 Oscillators, Clock and Event

TOSCn	Timer Oscillator pin n
XTALn	Input/Output for Oscillator pin n
CLKOUT	Peripheral Clock Output
EVOUT	Event Channel 0 Output
RTCOUT	RTC Clock Source Output

31.1.7 Debug/System functions

$\overline{RESET}$	Reset pin
PDI_CLK	Program and Debug Interface Clock pin
PDI_DATA	Program and Debug Interface Data pin
TCK	JTAG Test Clock
TDI	JTAG Test Data In
TDO	JTAG Test Data Out
TMS	JTAG Test Mode Select

31.2 Alternate Pin Functions

The tables below show the primary/default function for each pin on a port in the first column, the pin number in the second column, and then all alternate pin functions in the remaining columns. The head row shows what peripheral that enable and use the alternate pin functions.

For better flexibility, some alternate functions also have selectable pin locations for their functions, this is noted under the the first table where this apply.

Table 31-1. Port A - Alternate functions

PORT A	PIN #	INTERRUPT	ADCA POS/GAINPOS	ADCB POS/GAINPOS	ADCA NEG	ADCA GAINNEG	ACA POS	ACA NEG	ACA OUT	REFA
GND	60									
AVCC	61									
PA0	62	SYNC	ADC0	ADC8	ADC0		AC0	AC0		AREF
PA1	63	SYNC	ADC1	ADC9	ADC1		AC1	AC1		
PA2	64	SYNC/ASYNC	ADC2	ADC10	ADC2		AC2			
PA3	1	SYNC	ADC3	ADC11	ADC3		AC3	AC3		
PA4	1	SYNC	ADC4	ADC12		ADC4	AC4			
PA5	1	SYNC	ADC5	ADC13		ADC5	AC5	AC5		
PA6	4	SYNC	ADC6	ADC14		ADC6	AC6		AC1OUT	
PA7	5	SYNC	ADC7	ADC15		ADC7		AC7	AC0OUT	

Table 31-2. Port B - Alternate functions

PORT B	PIN #	INTERRUPT	ADCA POS/GAINPOS	ADCB POS/GAINPOS	ADCB NEG	ADCB GAINNEG	ACB POS	ACB NEG	ACB OUT	DACB	REFB	JTAG
PB0	6	SYNC	ADC8	ADC0	ADC0		AC0	AC0			AREF	
PB1	7	SYNC	ADC9	ADC1	ADC1		AC1	AC1				
PB2	8	SYNC/ASYNC	ADC10	ADC2	ADC2		AC2			DAC0		
PB3	9	SYNC	ADC11	ADC3	ADC3		AC3	AC3		DAC1		
PB4	10	SYNC	ADC12	ADC4		ADC4	AC4					TMS
PB5	11	SYNC	ADC13	ADC5		ADC5	AC5	AC5				TDI
PB6	12	SYNC	ADC14	ADC6		ADC6	AC6		AC1OUT			TCK
PB7	13	SYNC	ADC15	ADC7		ADC7		AC7	AC0OUT			TDO
GND	14											
VCC	15											

Table 31-3. Port C - Alternate functions

PORT C	PIN #	INTERRUPT	TCC0[1]	AWEXC	TCC1	USARTC0[2]	USARTC1	SPIC[3]	TWIC	CLOCKOUT[4]	EVENTOUT[5]
PC0	16	SYNC	OC0A	OC0ALS					SDA		
PC1	17	SYNC	OC0B	OC0AHS		XCK0			SCL		
PC2	18	SYNC/ASYNC	OC0C	OC0BLS		RXD0					
PC3	19	SYNC	OC0D	OC0BHS		TXD0					
PC4	20	SYNC		OC0CLS	OC1A			$\overline{SS}$			
PC5	21	SYNC		OC0CHS	OC1B		XCK1	MOSI			
PC6	22	SYNC		OC0DLS			RXD1	MISO		RTCOUT	
PC7	23	SYNC		OC0DHS			TXD1	SCK		clk_{PER}	EVOUT
GND	24										
VCC	25										

Notes:
1. Pin mapping of all TC0 can optionally be moved to high nibble of port.
2. Pin mapping of all USART0 can optionally be moved to high nibble of port.
3. Pins MOSI and SCK for all SPI can optionally be swapped.
4. CLKOUT can optionally be moved between port C, D and E and between pin 4 and 7.
5. EVOUT can optionally be moved between port C, D and E and between pin 4 and 7.

Table 31-4. Port D - Alternate functions

PORT D	PIN #	INTERRUPT	TCD0	TCD1	USBD	USARTD0	USARTD1	SPID	TWID	CLOCKOUT	EVENTOUT
PD0	26	SYNC	OC0A						SDA		
PD1	27	SYNC	OC0B			XCK0			SCL		
PD2	28	SYNC/ASYNC	OC0C			RXD0					
PD3	29	SYNC	OC0D			TXD0					
PD4	30	SYNC		OC1A				$\overline{SS}$			
PD5	31	SYNC		OC1B			XCK1	MOSI			
PD6	32	SYNC			D-		RXD1	MISO			
PD7	33	SYNC			D+		TXD1	SCK		clk_{PER}	EVOUT
GND	33										
VCC	34										

Table 31-5. Port E - Alternate functions

PORT E	PIN #	INTERRUPT	TCE0	AWEXE	TCE1	USARTE0	USARTE1	SPIE	TWIE	CLOCKOUT	EVENTOUT
PE0	36	SYNC	OC0A	OC0ALS					SDA		
PE1	37	SYNC	OC0B	OC0AHS		XCK0			SCL		
PE2	38	SYNC/ASYNC	OC0C	OC0BLS		RXD0					
PE3	39	SYNC	OC0D	OC0BHS		TXD0					
PE4	40	SYNC		OC0CLS	OC1A			$\overline{SS}$			
PE5	41	SYNC		OC0CHS	OC1B		XCK1	MOSI			
PE6	42	SYNC		OC0DLS			RXD1	MISO			
PE7	43	SYNC		OC0DHS			TXD1	SCK		clk_{PER}	EVOUT
GND	44										
VCC	45										

Table 31-6. Port F - Alternate functions

PORT F	PIN #	INTERRUPT	TCF0	USARTF0
PF0	46	SYNC	OC0A	
PF1	47	SYNC	OC0B	XCK0
PF2	48	SYNC/ASYNC	OC0C	RXD0
PF3	49	SYNC	OC0D	TXD0
PF4	50	SYNC		
PF5	51	SYNC		
GND	52			
VCC	53			
PF6	54	SYNC		
PF7	53	SYNC		

Table 31-7. Port R- Alternate functions

PORT R	PIN #	INTERRUPT	PDI	XTAL
PDI	56		PDI_DATA	
$\overline{\text{RESET}}$	57		PDI_CLOCK	
PRO	58	SYNC		XTAL2
PR1	59	SYNC		XTAL1

32. Peripheral Module Address Map

The address maps show the base address for each peripheral and module in XMEGA A3U. For complete register description and summary for each peripheral module, refer to the XMEGA AU Manual.

Base Address	Name	Description
0x0000	GPIO	General Purpose IO Registers
0x0010	VPORT0	Virtual Port 0
0x0014	VPORT1	Virtual Port 1
0x0018	VPORT2	Virtual Port 2
0x001C	VPORT3	Virtual Port 3
0x0030	CPU	CPU
0x0040	CLK	Clock Control
0x0048	SLEEP	Sleep Controller
0x0050	OSC	Oscillator Control
0x0060	DFLLRC32M	DFLL for the 32MHz Internal Oscillator
0x0068	DFLLRC2M	DFLL for the 2MHz Internal Oscillator
0x0070	PR	Power Reduction
0x0078	RST	Reset Controller
0x0080	WDT	Watch-Dog Timer
0x0090	MCU	MCU Control
0x00A0	PMIC	Programmable Multilevel Interrupt Controller
0x00B0	PORTCFG	Port Configuration
0x00C0	AES	AES Module
0x00D0	CRC	CRC Module
0x0100	DMA	DMA Controller
0x0180	EVSYS	Event System
0x01C0	NVM	Non Volatile Memory (NVM) Controller
0x0200	ADCA	Analog to Digital Converter on port A
0x0240	ADCB	Analog to Digital Converter on port B
0x0320	DACB	Digital to Analog Converter on port B
0x0380	ACA	Analog Comparator pair on port A
0x0390	ACB	Analog Comparator pair on port B
0x0400	RTC	Real Time Counter
0x0480	TWIC	Two Wire Interface on port C
0x04A0	TWIE	Two Wire Interface on port E
0x04C0	USB	USB Device
0x0600	PORTA	Port A
0x0620	PORTB	Port B
0x0640	PORTC	Port C
0x0660	PORTD	Port D
0x0680	PORTE	Port E
0x06A0	PORTF	Port F
0x07E0	PORTR	Port R
0x0800	TCC0	Timer/Counter 0 on port C
0x0840	TCC1	Timer/Counter 1 on port C
0x0880	AWEXC	Advanced Waveform Extension on port C
0x0890	HIRESC	High Resolution Extension on port C
0x08A0	USARTC0	USART 0 on port C
0x08B0	USARTC1	USART 1 on port C
0x08C0	SPIC	Serial Peripheral Interface on port C
0x08F8	IRCOM	Infrared Communication Module
0x0900	TCD0	Timer/Counter 0 on port D
0x0940	TCD1	Timer/Counter 1 on port D
0x0990	HIRESD	High Resolution Extension on port D
0x09A0	USARTD0	USART 0 on port D
0x09B0	USARTD1	USART 1 on port D
0x09C0	SPID	Serial Peripheral Interface on port D
0x0A00	TCE0	Timer/Counter 0 on port E
0x0A40	TCE1	Timer/Counter 1 on port E
0x0A80	AWEXE	Advanced Waveform Extension on port E
0x0A90	HIRESE	High Resolution Extension on port E
0x0AA0	USARTE0	USART 0 on port E
0x0AB0	USARTE1	USART 1 on port E
0x0AC0	SPIE	Serial Peripheral Interface on port E
0x0B00	TCF0	Timer/Counter 0 on port F

Base Address	Name	Description
0x0B90	HIRESF	High Resolution Extension on port F
0x0BA0	USARTF0	USART 0 on port F
0x0BC0	SPIF	Serial Peripheral Interface on port F

33. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
Arithmetic and Logic Instructions					
ADD	Rd, Rr	Add without Carry	Rd ← Rd + Rr	Z,C,N,V,S,H	1
ADC	Rd, Rr	Add with Carry	Rd ← Rd + Rr + C	Z,C,N,V,S,H	1
ADIW	Rd, K	Add Immediate to Word	Rd ← Rd + 1:Rd + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract without Carry	Rd ← Rd - Rr	Z,C,N,V,S,H	1
SUBI	Rd, K	Subtract Immediate	Rd ← Rd - K	Z,C,N,V,S,H	1
SBC	Rd, Rr	Subtract with Carry	Rd ← Rd - Rr - C	Z,C,N,V,S,H	1
SBCI	Rd, K	Subtract Immediate with Carry	Rd ← Rd - K - C	Z,C,N,V,S,H	1
SBIW	Rd, K	Subtract Immediate from Word	Rd + 1:Rd ← Rd + 1:Rd - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND	Rd ← Rd • Rr	Z,N,V,S	1
ANDI	Rd, K	Logical AND with Immediate	Rd ← Rd • K	Z,N,V,S	1
OR	Rd, Rr	Logical OR	Rd ← Rd v Rr	Z,N,V,S	1
ORI	Rd, K	Logical OR with Immediate	Rd ← Rd v K	Z,N,V,S	1
EOR	Rd, Rr	Exclusive OR	Rd ← Rd ⊕ Rr	Z,N,V,S	1
COM	Rd	One's Complement	Rd ← $FF - Rd	Z,C,N,V,S	1
NEG	Rd	Two's Complement	Rd ← $00 - Rd	Z,C,N,V,S,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V,S	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • ($FFh - K)	Z,N,V,S	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V,S	1
DEC	Rd	Decrement	Rd ← Rd - 1	Z,N,V,S	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V,S	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V,S	1
SER	Rd	Set Register	Rd ← $FF	None	1
MUL	Rd,Rr	Multiply Unsigned	R1:R0 ← Rd x Rr (UU)	Z,C	2
MULS	Rd,Rr	Multiply Signed	R1:R0 ← Rd x Rr (SS)	Z,C	2
MULSU	Rd,Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr (SU)	Z,C	2
FMUL	Rd,Rr	Fractional Multiply Unsigned	R1:R0 ← Rd x Rr<<1 (UU)	Z,C	2
FMULS	Rd,Rr	Fractional Multiply Signed	R1:R0 ← Rd x Rr<<1 (SS)	Z,C	2
FMULSU	Rd,Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← Rd x Rr<<1 (SU)	Z,C	2
DES	K	Data Encryption	if (H = 0) then R15:R0 ← Encrypt(R15:R0, K) else if (H = 1) then R15:R0 ← Decrypt(R15:R0, K)		1/2
Branch Instructions					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2
EIJMP		Extended Indirect Jump to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	2
JMP	k	Jump	PC ← k	None	3
RCALL	k	Relative Call Subroutine	PC ← PC + k + 1	None	2 / 3(1)
ICALL		Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2 / 3(1)
EICALL		Extended Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	3(1)

Mnemonics	Operands	Description	Operation	Flags	#Clocks
CALL	k	call Subroutine	PC ← k	None	3 / 4[1]
RET		Subroutine Return	PC ← STACK	None	4 / 5[1]
RETI		Interrupt Return	PC ← STACK	I	4 / 5[1]
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2 / 3
CP	Rd,Rr	Compare	Rd - Rr	Z,C,N,V,S,H	1
CPC	Rd,Rr	Compare with Carry	Rd - Rr - C	Z,C,N,V,S,H	1
CPI	Rd,K	Compare with Immediate	Rd - K	Z,C,N,V,S,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b) = 0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBRS	Rr, b	Skip if Bit in Register Set	if (Rr(b) = 1) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIC	A, b	Skip if Bit in I/O Register Cleared	if (I/O(A,b) = 0) PC ← PC + 2 or 3	None	2 / 3 / 4
SBIS	A, b	Skip if Bit in I/O Register Set	If (I/O(A,b) =1) PC ← PC + 2 or 3	None	2 / 3 / 4
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC ← PC + k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC ← PC + k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
Data Transfer Instructions					
MOV	Rd, Rr	Copy Register	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Pair	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LDS	Rd, k	Load Direct from data space	Rd ← (k)	None	2[1][2]
LD	Rd, X	Load Indirect	Rd ← (X)	None	1[1][2]
LD	Rd, X+	Load Indirect and Post-Increment	Rd ← (X) X ← X + 1	None	1[1][2]
LD	Rd, -X	Load Indirect and Pre-Decrement	X ← X - 1, ← X - 1 Rd ← (X) ← (X)	None	2[1][2]
LD	Rd, Y	Load Indirect	Rd ← (Y) ← (Y)	None	1[1][2]
LD	Rd, Y+	Load Indirect and Post-Increment	Rd ← (Y) Y ← Y + 1	None	1[1][2]

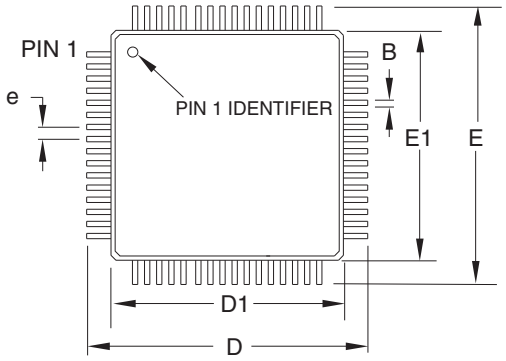
Mnemonics	Operands	Description	Operation	Flags	#Clocks
LD	Rd, -Y	Load Indirect and Pre-Decrement	Y ← Y - 1 Rd ← (Y)	None	2[1][2]
LDD	Rd, Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2[1][2]
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	1[1][2]
LD	Rd, Z+	Load Indirect and Post-Increment	Rd ← (Z), Z ← Z+1	None	1[1][2]
LD	Rd, -Z	Load Indirect and Pre-Decrement	Z ← Z - 1, Rd ← (Z)	None	2[1][2]
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2[1][2]
STS	k, Rr	Store Direct to Data Space	(k) ← Rd	None	2[1]
ST	X, Rr	Store Indirect	(X) ← Rr	None	1[1]
ST	X+, Rr	Store Indirect and Post-Increment	(X) ← Rr, X ← X + 1	None	1[1]
ST	-X, Rr	Store Indirect and Pre-Decrement	X ← X - 1, (X) ← Rr	None	2[1]
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	1[1]
ST	Y+, Rr	Store Indirect and Post-Increment	(Y) ← Rr, Y ← Y + 1	None	1[1]
ST	-Y, Rr	Store Indirect and Pre-Decrement	Y ← Y - 1, (Y) ← Rr	None	2[1]
STD	Y+q, Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2[1]
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	1[1]
ST	Z+, Rr	Store Indirect and Post-Increment	(Z) ← Rr Z ← Z + 1	None	1[1]
ST	-Z, Rr	Store Indirect and Pre-Decrement	Z ← Z - 1	None	2[1]
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2[1]
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Increment	Rd ← (Z), Z ← Z + 1	None	3
ELPM		Extended Load Program Memory	R0 ← (RAMPZ:Z)	None	3
ELPM	Rd, Z	Extended Load Program Memory	Rd ← (RAMPZ:Z)	None	3
ELPM	Rd, Z+	Extended Load Program Memory and Post-Increment	Rd ← (RAMPZ:Z), Z ← Z + 1	None	3
SPM		Store Program Memory	(RAMPZ:Z) ← R1:R0	None	-
SPM	Z+	Store Program Memory and Post-Increment by 2	(RAMPZ:Z) ← R1:R0, Z ← Z + 2	None	-
IN	Rd, A	In From I/O Location	Rd ← I/O(A)	None	1
OUT	A, Rr	Out To I/O Location	I/O(A) ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	1[1]
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2[1]
XCH	Z, Rd	Exchange RAM location	Temp ← Rd, Rd ← (Z), (Z) ← Temp	None	2
LAS	Z, Rd	Load and Set RAM location	Temp ← Rd, Rd ← (Z), (Z) ← Temp v (Z)	None	2
LAC	Z, Rd	Load and Clear RAM location	(Z) ← ($FF – Rd) • (Z) Rd ← (Z)	None	2

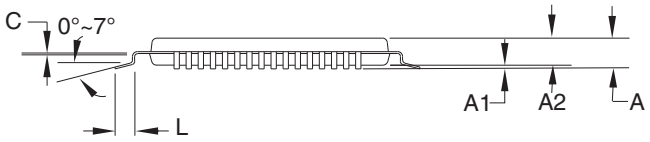
Mnemonics	Operands	Description	Operation	Flags	#Clocks
LAT	Z, Rd	Load and Toggle RAM location	(Z) ← Rd ⊕ (Z) Rd ← (Z)	None	2
Bit and Bit-test Instructions					
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0, C ← Rd(7)	Z,C,N,V,H	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0, C ← Rd(0)	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0) ← C, Rd(n+1) ← Rd(n), C ← Rd(7)	Z,C,N,V,H	1
ROR	Rd	Rotate Right Through Carry	Rd(7) ← C, Rd(n) ← Rd(n+1), C ← Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0) ↔ Rd(7..4)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
SBI	A, b	Set Bit in I/O Register	I/O(A, b) ← 1	None	1
CBI	A, b	Clear Bit in I/O Register	I/O(A, b) ← 0	None	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Two's Complement Overflow	V ← 1	V	1
CLV		Clear Two's Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
MCU Control Instructions					
BREAK		Break	(See specific descr. for BREAK)	None	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR)	None	1

Notes: 1. Cycle times for Data memory accesses assume internal memory accesses, and are not valid for accesses via the external RAM interface.
2. One extra cycle must be added when accessing Internal SRAM.

34. Packaging information

34.1 64A





COMMON DIMENSIONS
(Unit of Measure = mm)

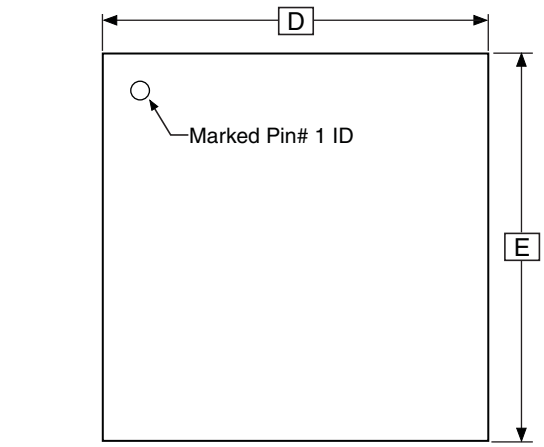
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation AEB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

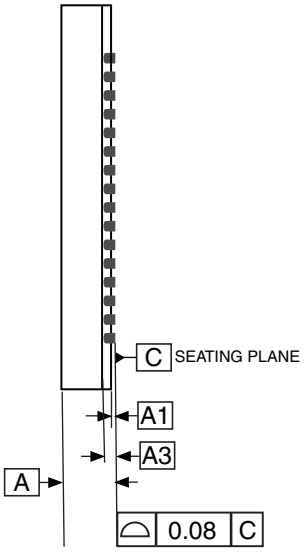
2010-10-20

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**64A,** 64-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	64A	C

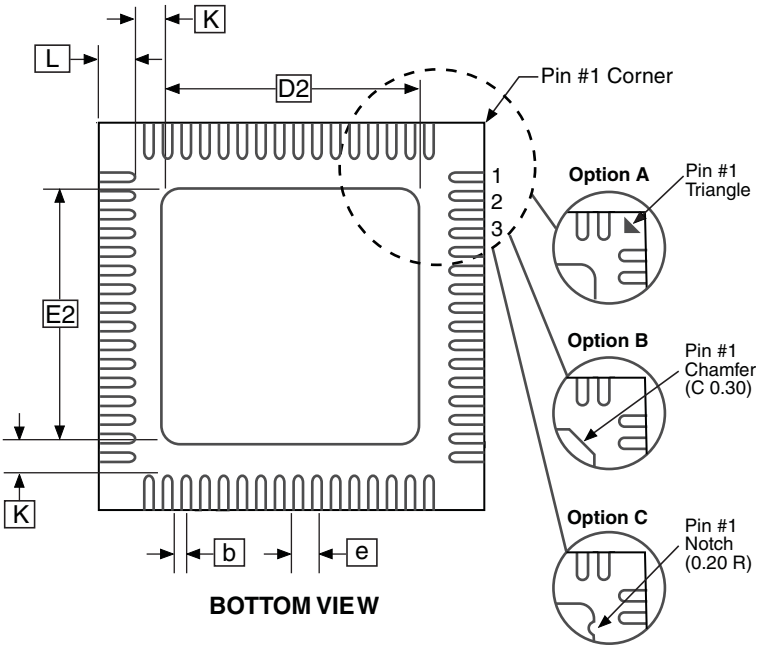
34.2 64M2



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A3		0.20 REF		
b	0.18	0.25	0.30	
D	8.90	9.00	9.10	
D2	7.50	7.65	7.80	
E	8.90	9.00	9.10	
E2	7.50	7.65	7.80	
e		0.50 BSC		
L	0.35	0.40	0.45	
K	0.20	0.27	0.40	

Notes: 1. JEDEC Standard MO-220, (SAW Singulation) Fig. 1, VMMD.
2. Dimension and tolerance conform to ASMEY14.5M-1994.

2010-10-20

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**64M2**, 64-pad, 9 x 9 x 1.0 mm Body, Lead Pitch 0.50 mm, 7.65 mm Exposed Pad, Micro Lead Frame Package (MLF)	64M2	E

35. Electrical Characteristics

All typical values are measured at T = 25°C unless other temperature condition is given. All minimum and maximum values are valid across operating temperature and voltage unless other conditions are given.

35.1 Absolute Maximum Ratings*

Operating Temperature	-55°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin with respect to Ground	-0.5V to V_{CC}+0.5V
Maximum Operating Voltage	4.0V
DC Current per I/O Pin	20.0mA
DC Current V_{CC} and GND Pins	200.0mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

35.2 DC Characteristics

Table 35-1. Current Consumption for Active and sleep modes

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{CC}	Active Power consumption(1)	32kHz, Ext. Clk	V_{CC} = 1.8V		148		µA
			V_{CC} = 3.0V		287		
		1MHz, Ext. Clk	V_{CC} = 1.8V		345		
			V_{CC} = 3.0V		697		
		2MHz, Ext. Clk	V_{CC} = 1.8V		575	700	
			V_{CC} = 3.0V		1.15	1.6	mA
		32MHz, Ext. Clk			10.6	15	
	Idle Power consumption(1)	32kHz, Ext. Clk	V_{CC} = 1.8V		4.3		µA
			V_{CC} = 3.0V		4.8		
		1MHz, Ext. Clk	V_{CC} = 1.8V		78		
			V_{CC} = 3.0V		147		
		2MHz, Ext. Clk	V_{CC} = 1.8V		156	250	
			V_{CC} = 3.0V		293	600	
		32MHz, Ext. Clk			4.7	7.0	mA
I_{CC}	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			1.75	5.0	
		WDT and Sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.3	3.0	
		WDT and Sampled BOD enabled, T=85°C			3.1	7.0	

Table 35-1. Current Consumption for Active and sleep modes (Continued)

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{CC}	Power-save power consumption[2]	RTC on ULP clock, WDT and sampled BOD enabled, T = 25°C					µA
			V_{CC} = 3.0V		1.3		
		RTC on 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.5	2	
			V_{CC} = 3.0V		0.7	2	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.9	3	
			V_{CC} = 3.0V		1.15	3	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		1150		
Module and peripheral power consumption[3]							
I_{CC}	ULP oscillator						µA
	32.768kHz int. oscillator				27		
	2MHz int. oscillator				85		
		DFLL enabled with 32.768kHz int. osc. as reference			115		
	32MHz int. oscillator				270		
		DFLL enabled with 32.768kHz int. osc. as reference			460		
	PLL	Multiplication factor = 20x			220		
	Real Time Counter				0.015		
	Watchdog Timer				1		
	BOD	Continuous mode			138		
		Sampled mode, include ULP oscillator			1.2		
	Internal 1.0V reference				100		
	Temperature sensor				95		
	ADC	250 kSPS VREF = Ext ref			3.0		mA
			CURRLIMIT = LOW		2.61		
			CURRLIMIT = MEDIUM		2.16		
			CURRLIMIT = HIGH		1.06		
	DAC	250kSPS VREF = Ext ref No load	Normal mode		1.63		
			Low Power mode		1.06		
	AC	High Speed Mode			330		µA
		Low Power Mode			130		
	DMA	615KBps between I/O registers and SRAM			115		
	Timer/Counter				16		
	USART	Rx and Tx enabled, 9600 BAUD			2.5		
	Flash memory and EEPROM programming				4		mA

Notes: 1. All Power Reduction Registers set.
2. Maximum limits are based on characterization and not tested in production.

3. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz External clock without prescaling, T = 25°C unless other conditiond are given .

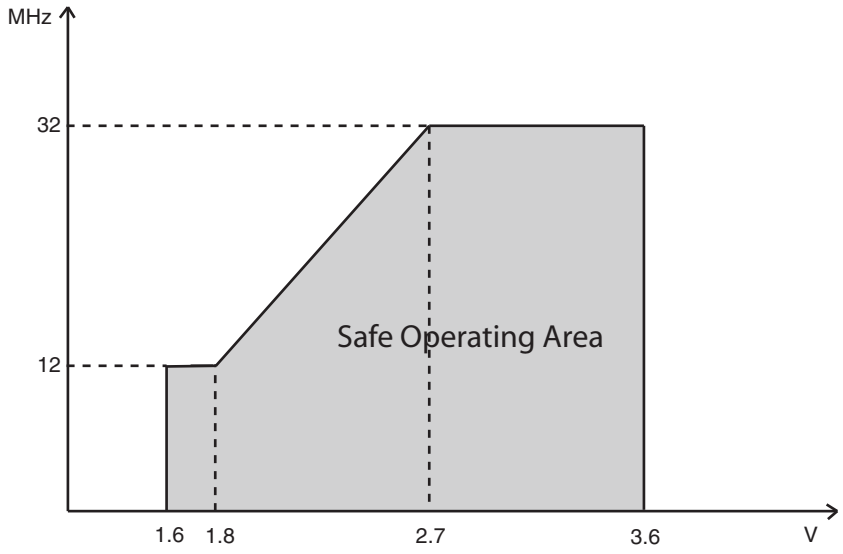
35.3 Operating Voltage and Frequency

Table 35-2. Operating voltage and frequency

Symbol	Parameter	Condition	Min	Typ	Max	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum System clock frequency of the Atmel® AVR® XMEGA A3U devices is depending on V_{CC}. As shown in Figure 35-1 on page 66 the Frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Figure 35-1. Maximum Frequency vs. Vcc



35.4 Wakeup time from sleep

Table 35-3. Device wakeup time from sleep modes with various system clock sources

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{wakeup}	Wake-up time from Idle	External 2MHz clock		2		µs
		32.768kHz internal oscillator		120		
		2MHz internal oscillator		2		
		32MHz internal oscillator		0.2		
	Wake-up time from Standby	External 2MHz clock		2		
		32.768kHz internal oscillator		120		
		2MHz internal oscillator		2		
		32MHz internal oscillator		0.2		
	Wake-up time from Extend Standby	External 2MHz clock		2		
		32.768kHz internal oscillator		120		
		2MHz internal oscillator		2		
		32MHz internal oscillator		0.2		
	Wake-up time from Power-save	External 2MHz clock		4.5		
		32.768kHz internal oscillator		320		
		2MHz internal oscillator		9		
		32MHz internal oscillator		5		
	Wake-up time from Power-down	External 2MHz clock		4.5		
		32.768kHz internal oscillator		320		
		2MHz internal oscillator		9		
		32MHz internal oscillator		5		

35.5 I/O Pin Characteristics

The I/O pins complies with the JEDEC LVTTL and LVCSMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

Table 35-4. I/O Pin Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	V_{CC} = 3.0 - 3.6V		2		V_{CC}+0.3	V
		V_{CC} = 2.3 - 2.7V		1.7		V_{CC}+0.3	
		V_{CC} = 1.6 - 2.7V		0.7*V_{CC}		V_{CC}+0.3	
V_{IL}	Low Level Input Voltage	V_{CC} = 3.0 - 3.6V		-0.3		0.8	
		V_{CC} = 2.3 - 2.7V		-0.3		0.7	
		V_{CC} = 1.6 - 2.7V		-0.3		0.2*V_{CC}	
V_{OH}	High Level Output Voltage	V_{CC} = 3.0 - 3.6V	I_{OH} = -2mA	2.4	3.19		
		V_{CC} = 2.3 - 2.7V	I_{OH} = -1mA	2.0	2.43		
			I_{OH} = -2mA	1.7	2.37		
V_{OL}	Low Level Output Voltage	V_{CC} = 3.0 - 3.6V	I_{OL} = 2mA		0.05	0.4	
		V_{CC} = 2.3 - 2.7V	I_{OL} = 1mA		0.03	0.4	
			I_{OL} = 2mA		0.05	0.7	
V_{OL}	Output Low Voltage GPIO	V_{CC} = 3.3V	I_{OL} = 15mA		0.41	0.76	
		V_{CC} = 3.0V	I_{OL} = 10mA		0.28	0.64	
		V_{CC} = 1.8V	I_{OL} = 5mA		0.18	0.46	
V_{OH}	Output High Voltage GPIO	V_{CC} = 3.3V	I_{OH} = -8mA	2.6	2.86		
		V_{CC} = 3.0V	I_{OH} = -6mA	2.1	2.63		
		V_{CC} = 1.8V	I_{OH} = -2mA	1.4	1.63		
I_{IN}	Input Leakage Current I/O pin				<0.001	0.1	µA
I_{IL}	Input Leakage Current I/O pin				<0.001	0.1	
R_P	I/O pin Pull/Buss keeper Resistor				27		kΩ
R_{RST}	Reset pin Pull-up Resistor				25		
	Input hysteresis				0.2		V
t_r	Pad rise time	No load			4		nS
			slew rate limitation		7		

35.6 ADC Characteristics

Table 35-5. ADC Characteristics

Symbol	Parameter	Condition[2]		Min	Typ	Max	Units
RES	Resolution			8	12	12	Bits
	Conversion time (latency)	(RES+2)/2+(GAIN !=0), RES = 8 or 2		5		8	Clk_{ADC} cycles
	Sampling Time	1/2 Clk_{ADC} cycle		0.25		5	µS
Clk_{ADC}	ADC Clock frequency	Max is 1/4 of Peripheral clock frequency		100		2000	kHz
		Measuring internal signals		100		125	
f_{ADC}	Sample rate			100		2000	kSPS
		CURRLIMIT = LOW		100		1500	
		CURRLIMIT = MEDIUM		100		1000	
		CURRLIMIT = HIGH		100		500	
AVCC	Analog supply voltage			V_{CC}- 0.3		V_{CC}+ 0.3	V
VREF	Reference voltage			1		AV_{CC}- 0.6	
Rin	Input resistance	Switched			4.0		kΩ
Cin	Input capacitance	Switched			4.4		pF
R_{AREF}	Reference input resistance	(leackage only)			>10		MΩ
C_{AREF}	Reference input capacitance	Static load			7		pF
	Start-up time	ADC clock cycles			12	24	Clk_{ADC} cycles
	ADC settling time	After changing reference or input mode			7	7	
		After ADC flush			1	1	
Vin	Input range			-0.1		AV_{CC}+ 0.1	V
	Conversion range	Differential mode, Vinp - Vinn		-VREF		VREF	
Vin	Conversion range	Single ended unsigned mode, Vinp		-ΔV		VREF-ΔV	
INL[1]	Integral non-linearity	500kSPS	V_{CC}-1.0V < VREF< V_{CC}-0.6V		±1.2	2	LSB
					±1.5	3	
		2000kSPS	V_{CC}-1.0V < VREF< V_{CC}-0.6V		±1.0	2	
					±1.5	3	
DNL[1]	Differential non-linearity	500kSPS, guaranteed monotonic	V_{CC}-1.0V < VREF< V_{CC}-0.6V		±0.8	1.2	
					±0.5	1.5	
		2000kSPS, guaranteed monotonic	V_{CC}-1.0V < VREF< V_{CC}-0.6V		±0.8	1.2	
					±0.5	1.5	
	Offset Error				-2		mV
		Temperature drift			<0.01		mV/K
		Operating voltage drift			<0.6		mV/V

Table 35-5. ADC Characteristics (Continued)

Symbol	Parameter	Condition[2]		Min	Typ	Max	Units
	Gain Error	Differential mode	External reference		-1		mV
			AVCC/1.6		10		
			AVCC/2.0		8		
			Bandgap		±5		
		Temperature drift			<0.02		mV/K
		Operating voltage drift			<0.5		mV/V

Notes: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external VREF is used.

Table 35-6. ADC Gain Stage Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Units
Rin	Input resistance	Switched in normal mode			4.0		kΩ
Cin	Input capacitance	Switched in normal mode			4.4		pF
	Signal range	Gain stage output		0		V_{CC}- 0.6	V
	Propagation delay	ADC conversion rate			1		Clk_{ADC} cycles
	Clock rate	Same as ADC		100		1000	kHz
INL[1]	Integral Non-Linearity	500kSPS	All gain settings		±2.0	4	LSB
DNL[1]	Differential Non-Linearity		All gain setting, guaranteed monotonic		±0.9	1.5	
	Gain Error	1x gain, normal mode			-0.8		%
		8x gain, normal mode			-2.5		
		64x gain, normal mode			-3.5		
	Offset Error, input refered	1x gain, normal mode			-2		mV
		8x gain normal mode			-5		
		64x gain normal mode			-4		

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.

35.7 DAC Characteristics

Table 35-7. DAC Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Units
RES	Input Resolution					12	Bits
AVREF	External reference voltage			1.0		V_{CC}-0.6	V
$R_{channel}$	DC output impedance					50	Ω
	Linear output voltage range			0.15		AV_{CC}-0.15	
R_{AREF}	Reference input resistance				>10		MΩ
C_{AREF}	Reference input capacitance	Static load			7		pF
	Minimum Resistance load			1			kΩ
	Maximum capacitance laod					100	pF
		1000Ω serial resistance				1	nF
	Output sink/source	Operating within specification				AV_{CC}/1000	mA
		Safe operation				10	
	Enable, reset to code				0		Ox
INL[1]	Integral non-linearity	VREF= Ext 1.0V	V_{CC} = 1.6V		±2.0	3	LSB
			V_{CC} = 3.6V		±1.5	2.5	
		VREF=AVCC	V_{CC} = 1.6V		±2.0	4	
			V_{CC} = 3.6V		±1.5	4	
		VREF=INT1V	V_{CC} = 1.6V		±3.0		
			V_{CC} = 3.6V		±3.0		
DNL[1]	Differential Non-Linearity	VREF=Ext 1.0V, guaranteed monotonic	V_{CC} = 1.6V		±1.5	3	
			V_{CC} = 3.6V		±0.6	1.5	
		VREF=AVCC, guaranteed monotonic	V_{CC} = 1.6V		±1.0	3.5	
			V_{CC} = 3.6V		±0.6	1.5	
		VREF=INT1V	V_{CC} = 1.6V		±3.0		
			V_{CC} = 3.6V		±3.0		
	Gain error	After calibration			<4		
	Gain calibration step size				4		
	Gain calibration drift	VREF= Ext 1.0V			<0.2		mV/K
	Offset error	After calibration			<1		LSB
	Offset calibration step size				1		
Fclk	Conversion rate	Fout=Fclk/4, Cload=100pF, Max step size		0		1000	kSPS
				0		1000	

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% output voltage range.

35.8 Analog Comparator Characteristics

Table 35-8. Analog Comparator Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Units
V_{off}	Input Offset Voltage				<±10		mV
I_{lk}	Input Leakage Current				<1000		pA
	Input voltage range			-0.1		AV_{CC}+ 0.1	V
	AC startup time				100		µs
V_{hys1}	Hysteresis, None				0		mV
V_{hys2}	Hysteresis, Small	mode = High Speed (HS)			13		
		mode = Low Power (LP)			30		
V_{hys3}	Hysteresis, Large	mode = HS			30		
		mode = LP			60		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T= 85°C	mode = HS		90	100	ns
		mode = HS			95		
		V_{CC} = 3.0V, T= 85°C	mode = LP		200	500	
		mode = LP			200		
	64-Level Voltage Scaler	Integral non-linearity (INL)			0.5	1	LSB
	Current source accuracy after calibration				5		%
	Current source calibration range			4		6	µA

35.9 Bandgap and Internal 1.0V Reference Characteristics

Table 35-9. Bandgap and Internal 1.0V Reference Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Startup time	As reference for ADC or DAC	1 Clk_{PER} + 2.5µs			µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T= 85°C, After calibration	0.99	1	1.01	
	Variation over voltage and temperature			±1.0		%

35.10 Brownout Detection Characteristics

Table 35-10. Brownout Detection Characteristics[1]

Symbol	Parameter	Condition	Min	Typ	Max	Units
	BOD level 0 falling Vcc		1.62	1.62	1.72	V
	BOD level 1 falling Vcc			1.81		
	BOD level 2 falling Vcc			2.01		
	BOD level 3 falling Vcc			2.21		
	BOD level 4 falling Vcc			2.41		
	BOD level 5 falling Vcc			2.61		
	BOD level 6 falling Vcc			2.81		
	BOD level 7 falling Vcc			3.01		
t_{BOD}	Detection time	Continous mode		0,4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.6		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

35.11 External Reset Characteristics

Table 35-11. External Reset Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{EXT}	Minimum reset pulse width			90	1000	ns
V_{RST}	Reset threshold voltage	V_{CC} = 2.7 - 3.6V		0.50*V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.40*V_{CC}		

35.12 Power-on Reset Characteristics

Table 35-12. Power-on Reset Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{POT-}	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.2		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

35.13 Flash and EEPROM Memory Characteristics

Table 35-13. Endurance and Data Retention

Symbol	Parameter	Condition		Min	Typ	Max	Units
	Flash	Write/Erase cycles	25°C	10K			Cycle
			85°C	10K			
		Data retention	25°C	100			Year
			55°C	25			
	EEPROM	Write/Erase cycles	25°C	80K			Cycle
			85°C	30K			
		Data retention	25°C	100			Year
			55°C	25			

Table 35-14. Programming time

Symbol	Parameter	Condition	Min	Typ[1]	Max	Units
	Chip Erase	256KB Flash, EEPROM[2] and SRAM Erase		105		ms
		192KB Flash, EEPROM[2] and SRAM Erase		90		
		128KB Flash, EEPROM[2] and SRAM Erase		75		
		64KB Flash, EEPROM[2] and SRAM Erase		55		
	Flash	Page Erase		6		
		Page Write		6		
		Page WriteAutomatic Page Erase and Write		12		
	EEPROM	Page Erase		6		
		Page Write		6		
		Page WriteAutomatic Page Erase and Write		12		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

35.14 Clock and Oscillator Characteristics

35.14.1 Calibrated 32.768kHz Internal Oscillator characteristics

Table 35-15. Calibrated 32.768kHz Internal Oscillator characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

35.14.2 Calibrated 2MHz RC Internal Oscillator characteristics

Table 35-16. Calibrated 2MHz Internal Oscillator characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8	2.0	2.2	MHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration stepsize			0.22		

35.14.3 Calibrated and tunable 32MHz Internal Oscillator characteristics

Table 35-17. Calibrated 32MHz Internal Oscillator characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30	32	55	MHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	
	DFLL calibration step size			0.23		

35.14.4 32kHz Internal ULP Oscillator characteristics

Table 35-18. 32kHz Internal ULP Oscillator characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Output frequency			38		kHz

35.14.5 Internal Phase Locked Loop (PLL) characteristics

Table 35-19. Calibrated 32MHz Internal Oscillator characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{IN}	Input Frequnecy	Output frequnecy must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Ouput frequnecy [1]		20		32	
			20		128	
	Start-up time			25		µs
	re-lock time			25		

1. The maximum ouput frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than 4 times the maximum CPU frequency.

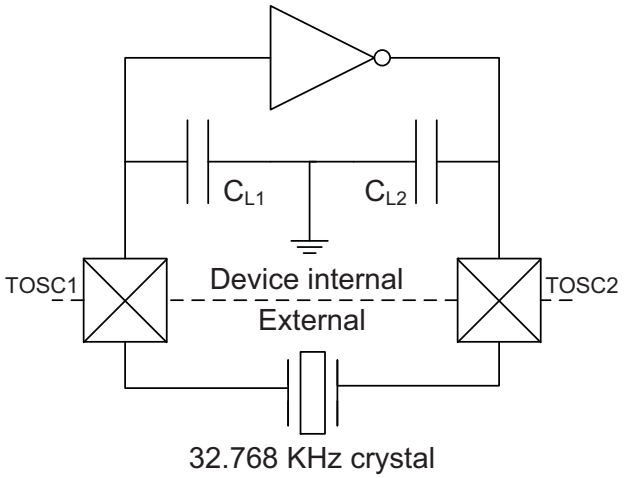
35.14.6 External 32.768kHz Crystal Oscillator and TOSC characteristics

Table 35-20. External 32.768kHz Crystal Oscillator and TOSC characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
C_{IN_TOSC}	Input capacitance between TOSC pins	Normal mode		1.7		pF
		Low power mode		2.2		
	Recommended Safety factor	capacitance load matched to crystal specification	3			

Note: 1. See Figure 35-2 on page 76 for definition

Figure 35-2. TOSC input capacitance



The input capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

35.14.7 External Clock Characteristics

Figure 35-3. External Clock Drive Waveform

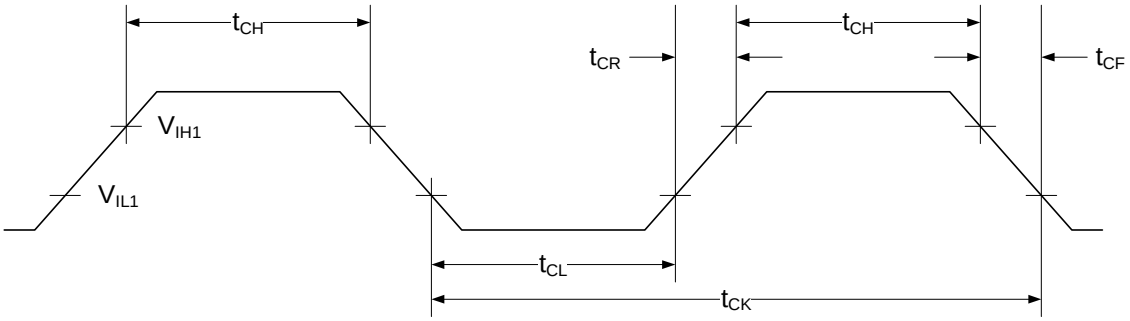


Table 35-21. External Clock used as System Clock without prescaling

Symbol	Parameter	Condition	Min	Typ	Max	Units
$1/t_{CK}$	Clock Frequency[1]	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	30.0			
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	30.0			
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.8V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

Table 35-22. External Clock with prescaler[1] for System Clock

Symbol	Parameter	Condition	Min	Typ	Max	Units
$1/t_{CK}$	Clock Frequency[2]	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	4.5			
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)				1.5	
t_{CF}	Fall Time (for maximum frequency)				1.5	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.8V and 2.7V, and the same applies for all other parameters with supply voltage conditions

35.15 SPI Characteristics

Figure 35-4. SPI Interface Requirements in Master mode

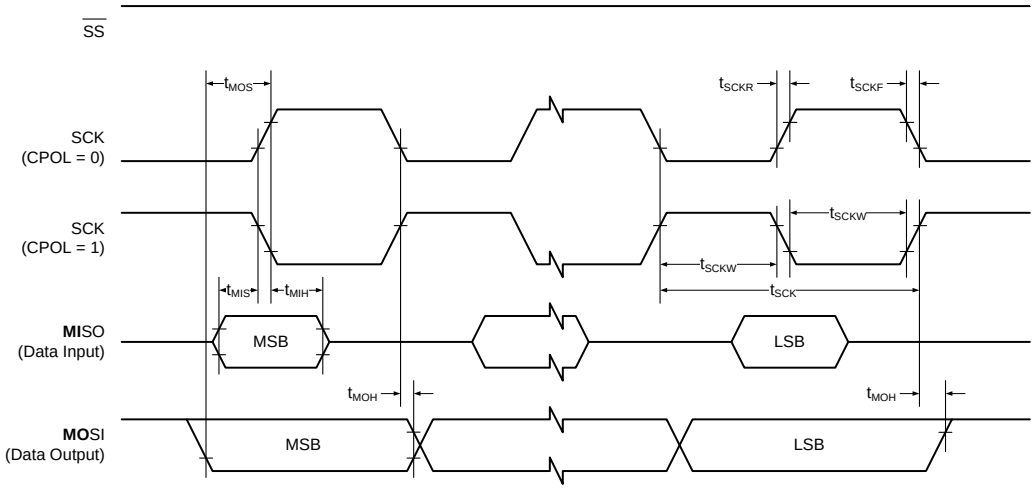


Figure 35-5. SPI Timing Requirements in Slave mode

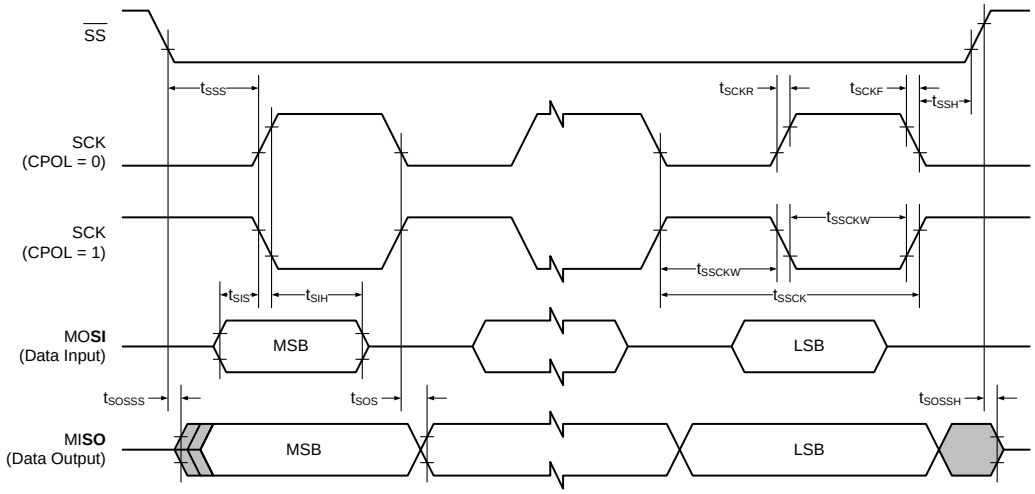


Table 35-23. SPI Timing Characteristics and Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{SCK}	SCK Period	Master		(See Table 21-4 in XMEGA AU Manual)		ns
t_{SCKW}	SCK high/low width	Master		0.5*SCK		
t_{SCKR}	SCK Rise time	Master		2.7		
t_{SCKF}	SCK Fall time	Master		2.7		
t_{MIS}	MISO setup to SCK	Master		10		
t_{MIH}	MISO hold after SCK	Master		10		
t_{MOS}	MOSI setup SCK	Master		0.5*SCK		
t_{MOH}	MOSI hold after SCK	Master		1		
t_{SSCK}	Slave SCK Period	Slave	4*t Clk_{PER}			
t_{SSCKW}	SCK high/low width	Slave	2*t Clk_{PER}			
t_{SSCKR}	SCK Rise time	Slave			1600	
t_{SSCKF}	SCK Fall time	Slave			1600	
t_{SIS}	MOSI setup to SCK	Slave	3			
t_{SIH}	MOSI hold after SCK	Slave	t Clk_{PER}			
t_{SSS}	$\overline{SS}$ setup to SCK	Slave	21			
t_{SSH}	$\overline{SS}$ hold after SCK	Slave	20			
t_{SOS}	MISO setup SCK	Slave		8		
t_{SOH}	MISO hold after SCK	Slave		13		
t_{SOSS}	MISO setup after $\overline{SS}$ low	Slave		11		
t_{SOSH}	MISO hold after $\overline{SS}$ high	Slave		8		

35.16 Two-Wire Interface Characteristics

Table 2-1 describes the requirements for devices connected to the Two Wire Serial Bus. The XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 35-6.

Figure 35-6. Two-Wire Interface Bus Timing

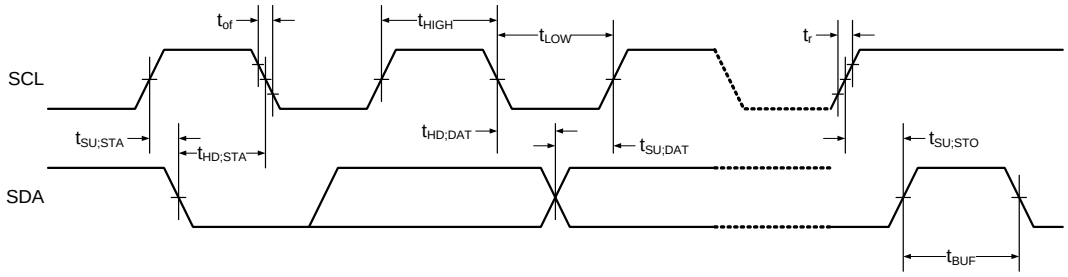


Table 35-24. Two Wire Serial Bus Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage		$0.7V_{CC}$		V_{CC}+0.5	V
V_{IL}	Input Low Voltage		0.5		$0.3*V_{CC}$	
V_{hys}	Hysteresis of Schmitt Trigger Inputs		$0.05V_{CC}$ (1)			
V_{OL}	Output Low Voltage	3mA, sink current	0		0.4	
t_r	Rise Time for both SDA and SCL		$20+0.1C_b$ (1)(2)		300	ns
t_{of}	Output Fall Time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$ (2)	$20+0.1C_b$ (1)(2)		250	
t_{SP}	Spikes Suppressed by Input Filter		0		50	
I_I	Input Current for each I/O Pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O Pin				10	pF
f_{SCL}	SCL Clock Frequency	f_{PER} (3)>max($10f_{SCL}$, 250kHz)	0		400	kHz
R_P	Value of Pull-up resistor	$f_{SCL} \leq 100kHz$	$\frac{V_{CC}-0.4V}{3mA}$	$\frac{300ms}{C_b}$		Ω
		$f_{SCL} > 100kHz$				
$t_{HD;STA}$	Hold Time (repeated) START condition	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{LOW}	Low Period of SCL Clock	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			
t_{HIGH}	High Period of SCL Clock	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq 100kHz$				
		$f_{SCL} > 100kHz$				

Table 35-24. Two Wire Serial Bus Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq 100kHz$	0		3.45	µs
		$f_{SCL} > 100kHz$	0		0.9	
$t_{SU;DAT}$	Data setup time	$f_{SCL} \leq 100kHz$	250			
		$f_{SCL} > 100kHz$	100			
$t_{SU;STO}$	Setup time for STOP condition	$f_{SCL} \leq 100kHz$	4.0			
		$f_{SCL} > 100kHz$	0.6			
t_{BUF}	Bus free time between a STOP and START condition	$f_{SCL} \leq 100kHz$	4.7			
		$f_{SCL} > 100kHz$	1.3			

Notes:
1. Required only for $f_{SCL} > 100kHz$
2. C_b = Capacitance of one bus line in pF
3. f_{PER} = Peripheral clock frequency

36. Typical Characteristics

36.1 Active Supply Current

Figure 36-1. Active Supply Current vs. Frequency
f_{SYS} = 0 - 1.0MHz External clock, T = 25°C

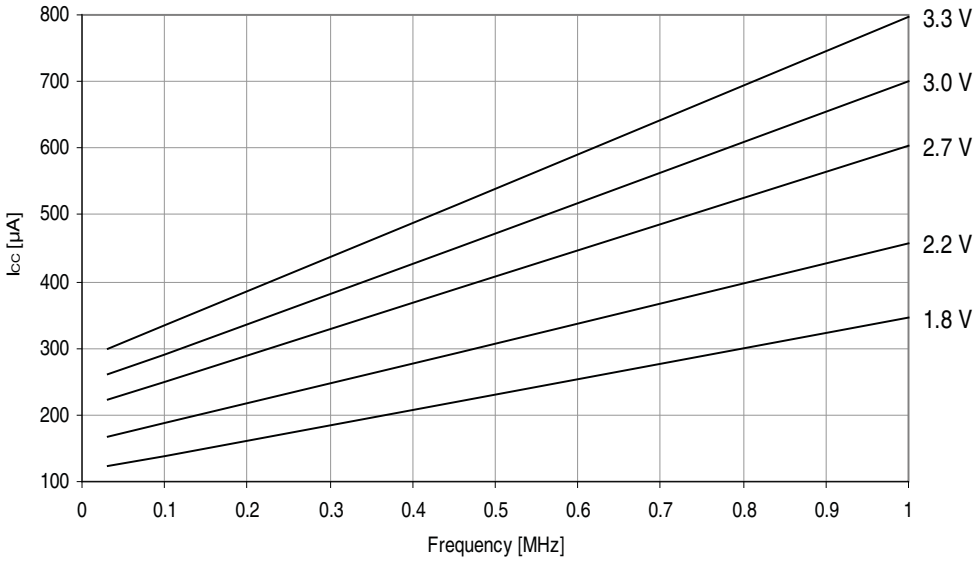


Figure 36-2. Active Supply Current vs. Frequency
f_{SYS} = 1 - 32MHz External clock, T = 25°C

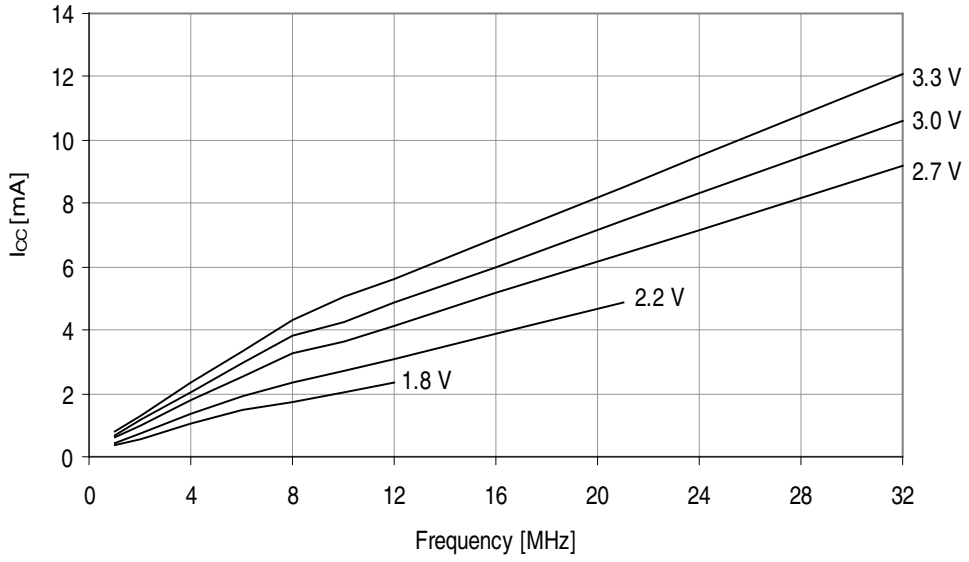


Figure 36-3. Active Supply Current vs. Vcc

f_{SYS} = 1.0MHz External Clock

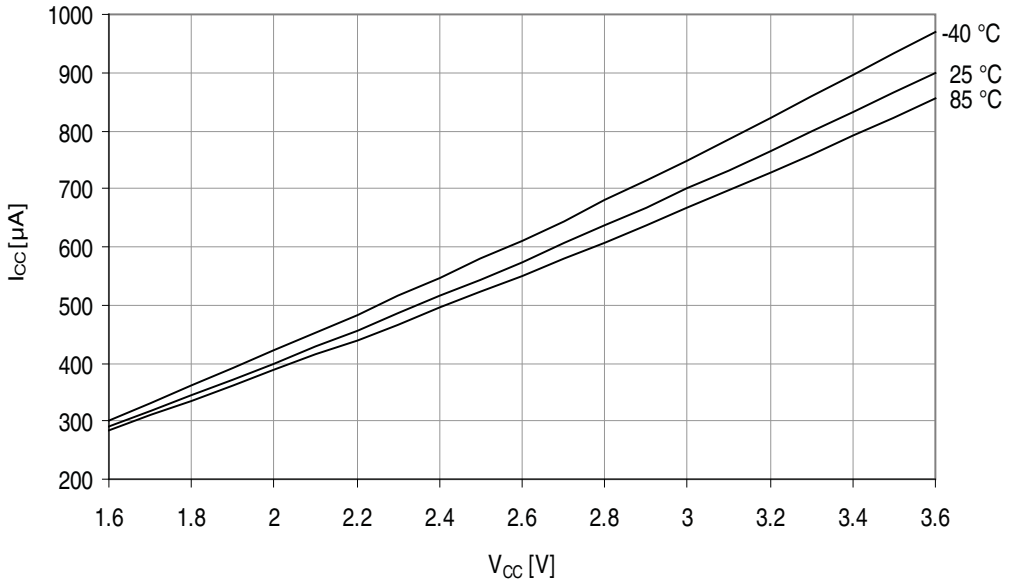
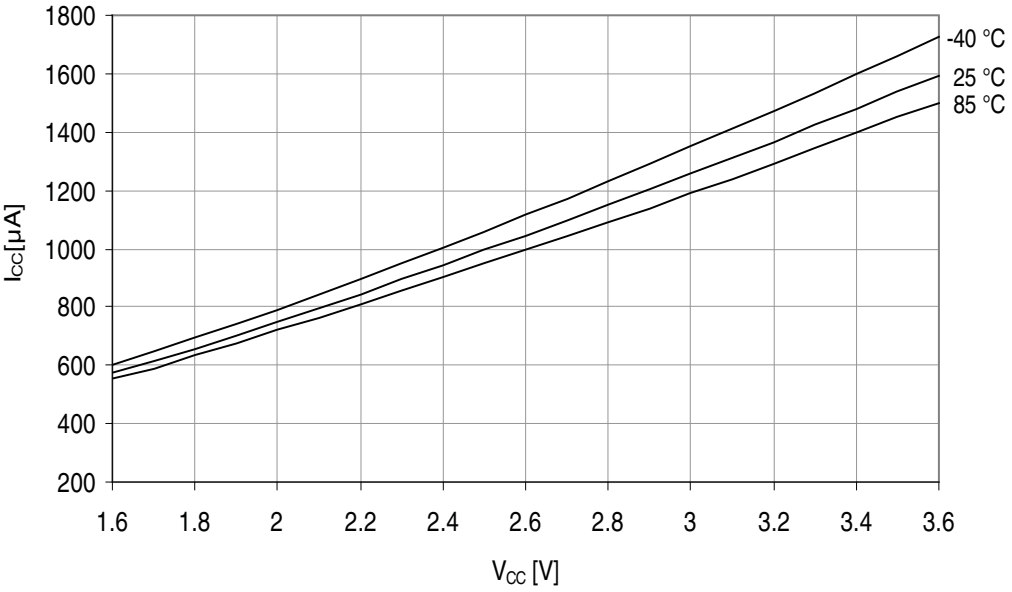


Figure 36-4. Active Supply Current vs. Vcc

f_{SYS} = 2.0MHz internal Oscillator



36.2 Idle Supply Current

Figure 36-5. Idle Supply Current vs. Frequency
f_{SYS} = 0 - 1.0MHz, T = 25°C

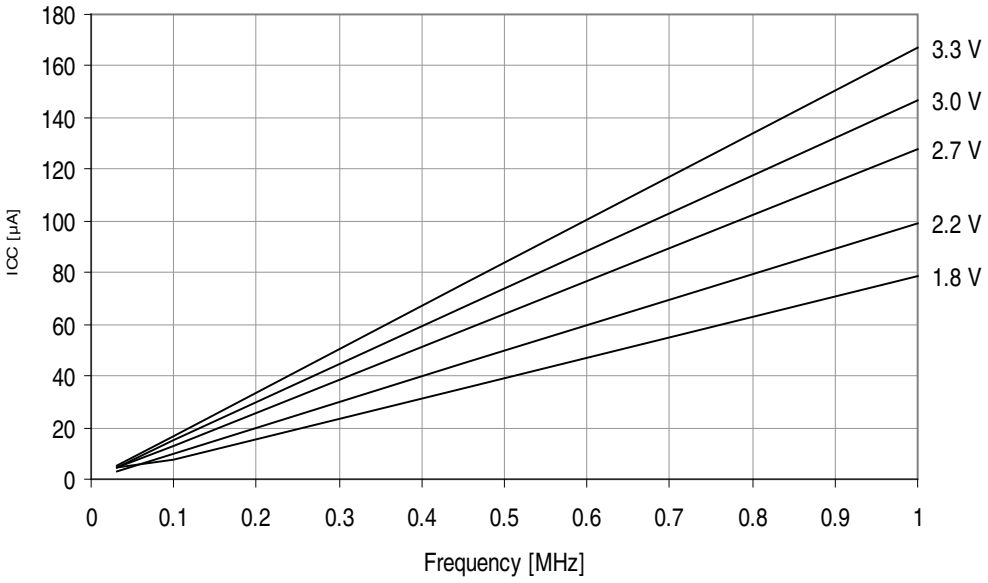


Figure 36-6. Idle Supply Current vs. Frequency
f_{SYS} = 1 - 32MHz, T = 25°C

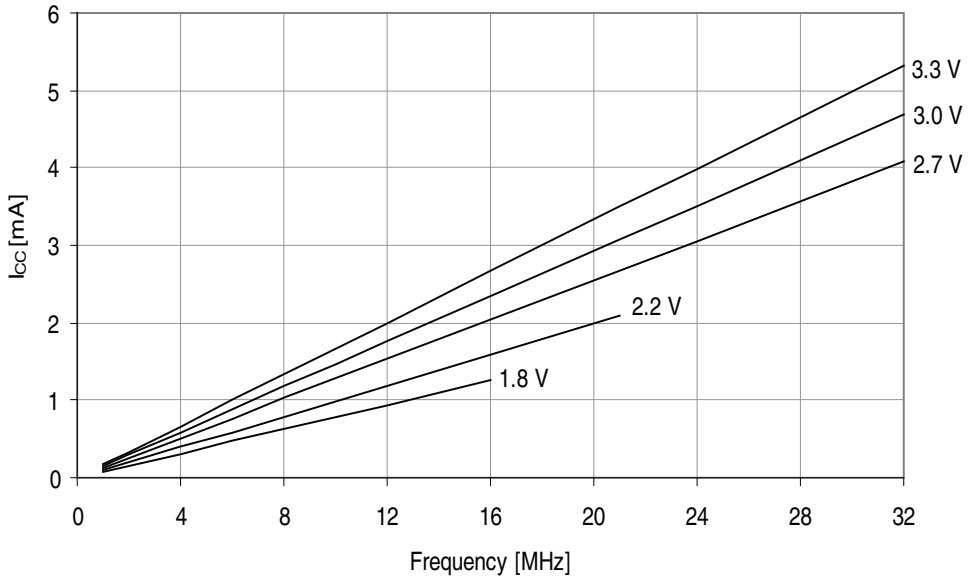


Figure 36-7. Idle Supply Current vs. Vcc

f_{SYS} = 32.768kHz internal Oscillator

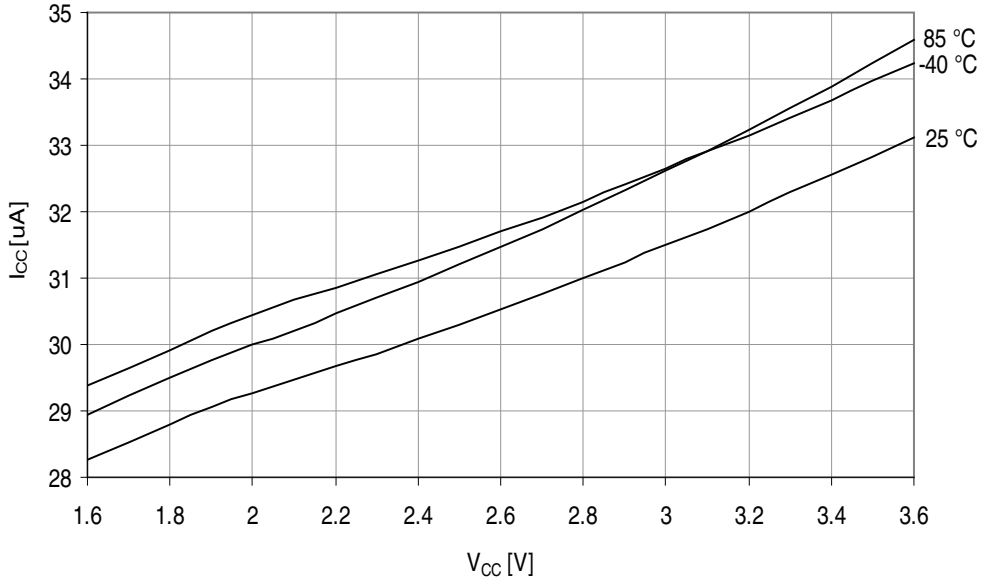


Figure 36-8. Idle Supply Current vs. Vcc

f_{SYS} = 2.0MHz internal Oscillator

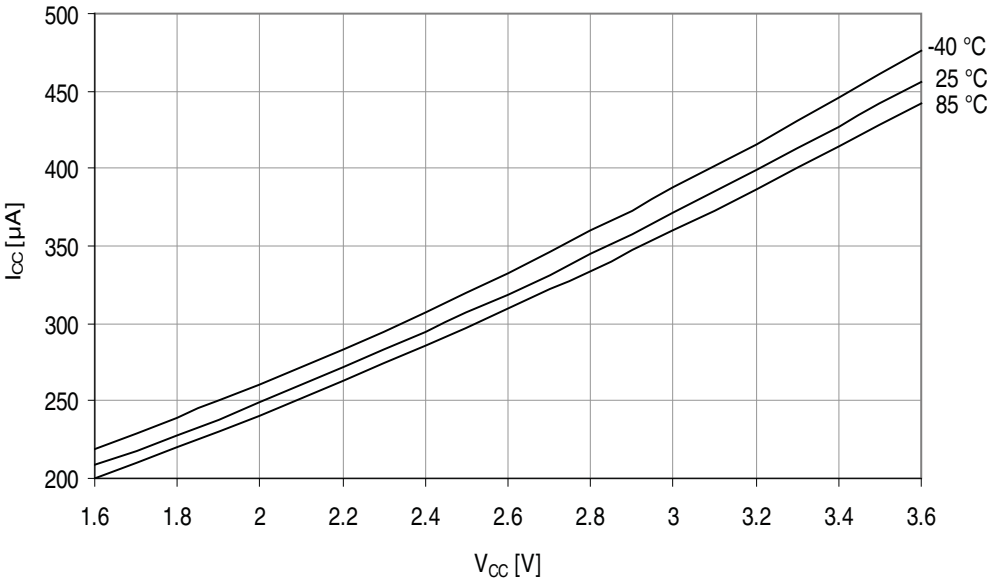
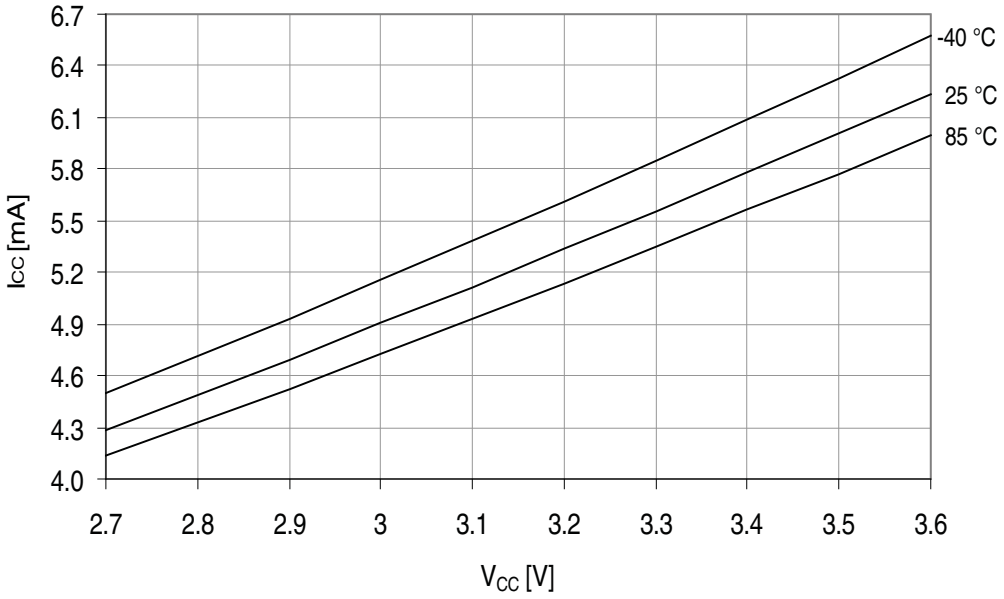


Figure 36-9. Idle Supply Current vs. Vcc

f_{SYS} = 32MHz internal Oscillator



36.3 Power-down Supply Current

Figure 36-10. Power-down Supply Current vs. Vcc

All functions disabled

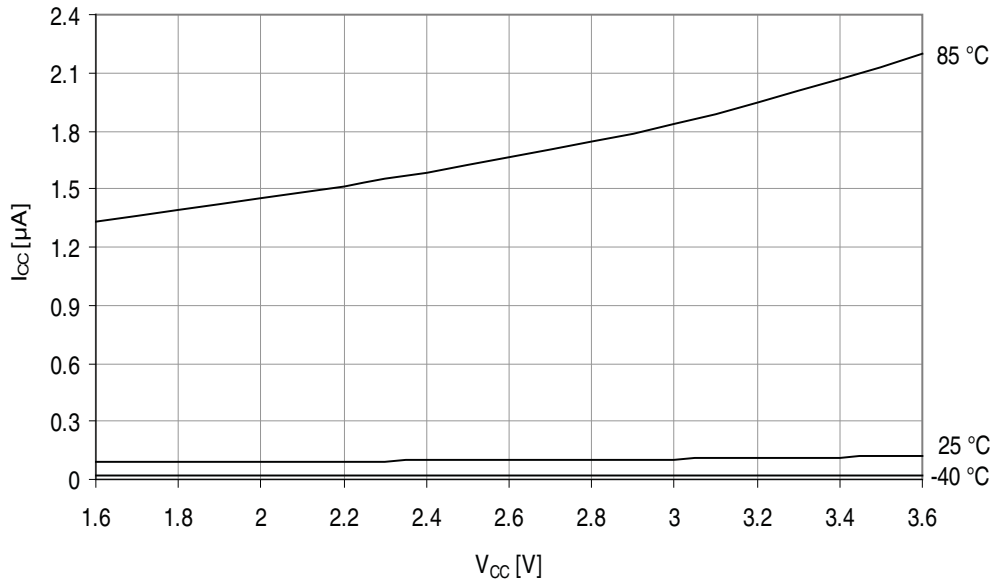
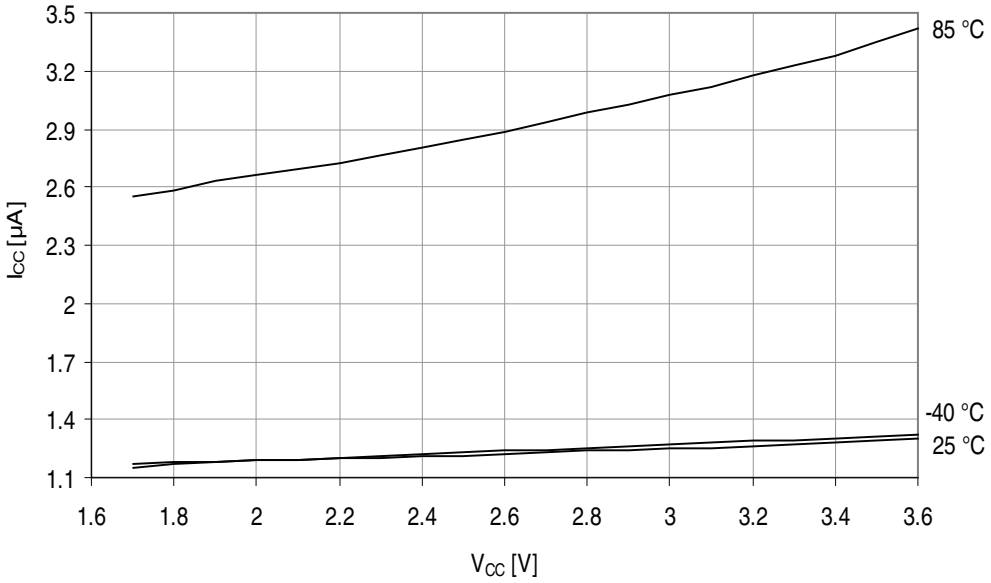


Figure 36-11. Power-down Supply Current vs. Vcc
Sampled BOD, WDT, RTC from ULP



36.4 Pin Pull-up

Figure 36-12. Reset and I/O Pull-up Resistor Current vs. Reset Pin Voltage
V_{CC} = 1.8V

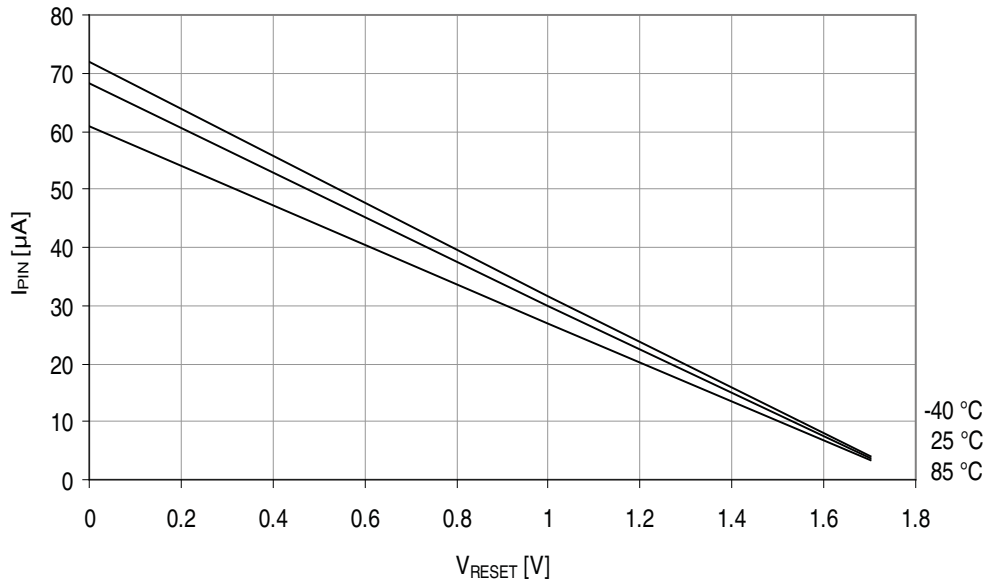


Figure 36-13. Reset and I/O Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 3.0V

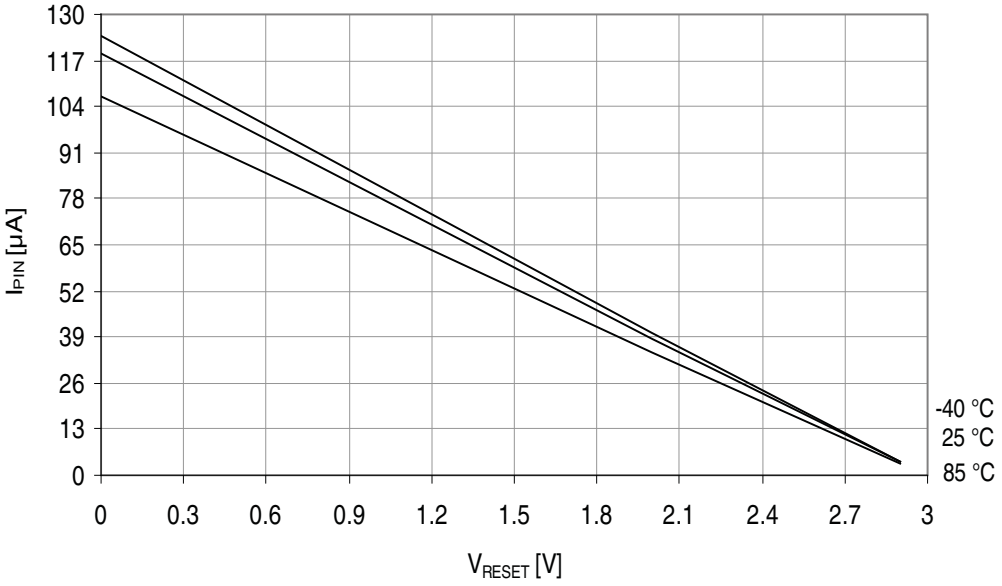
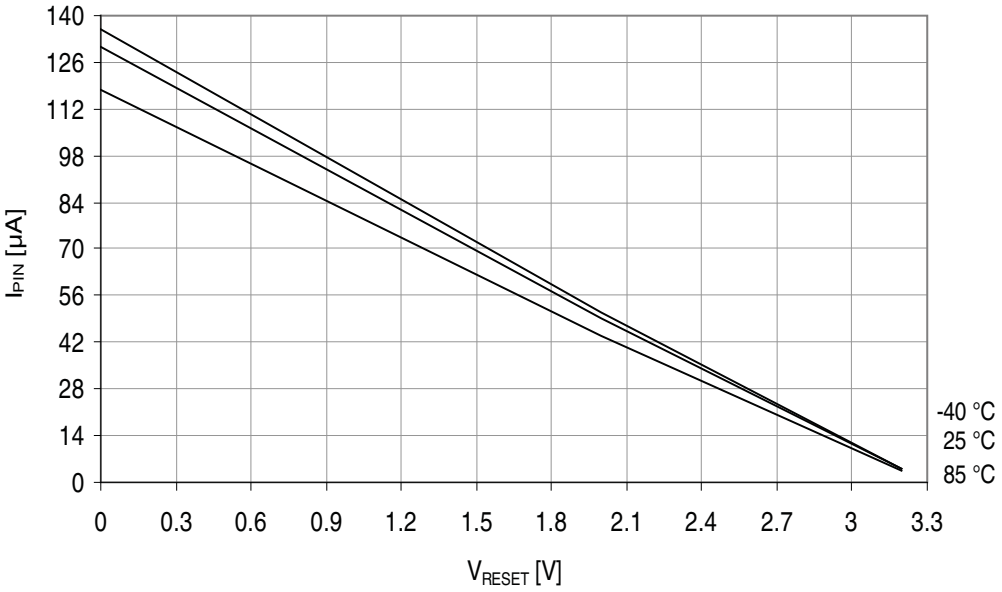


Figure 36-14. Reset and I/O Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 3.3V



36.5 Pin Output Voltage vs. Sink/Source Current

Figure 36-15. I/O Pin Output Voltage vs. Source Current

Vcc = 1.8V

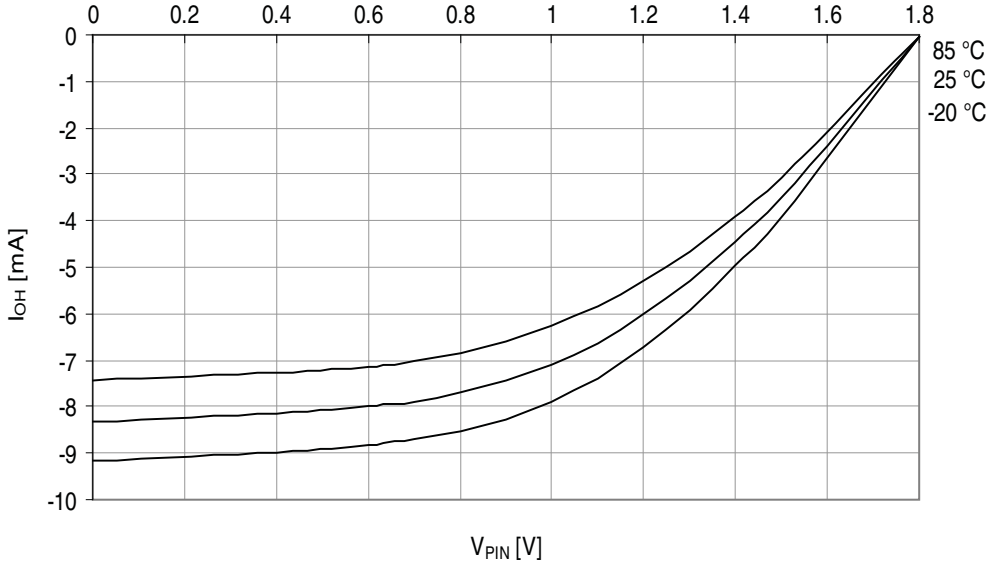


Figure 36-16. I/O Pin Output Voltage vs. Source Current

Vcc = 3.0V

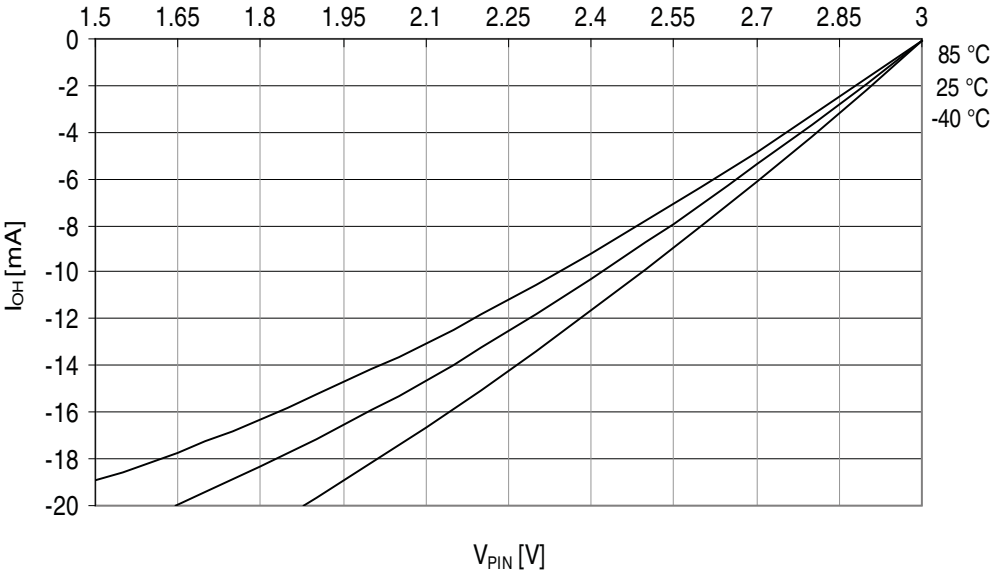


Figure 36-17. I/O Pin Output Voltage vs. Source Current

Vcc = 3.3V

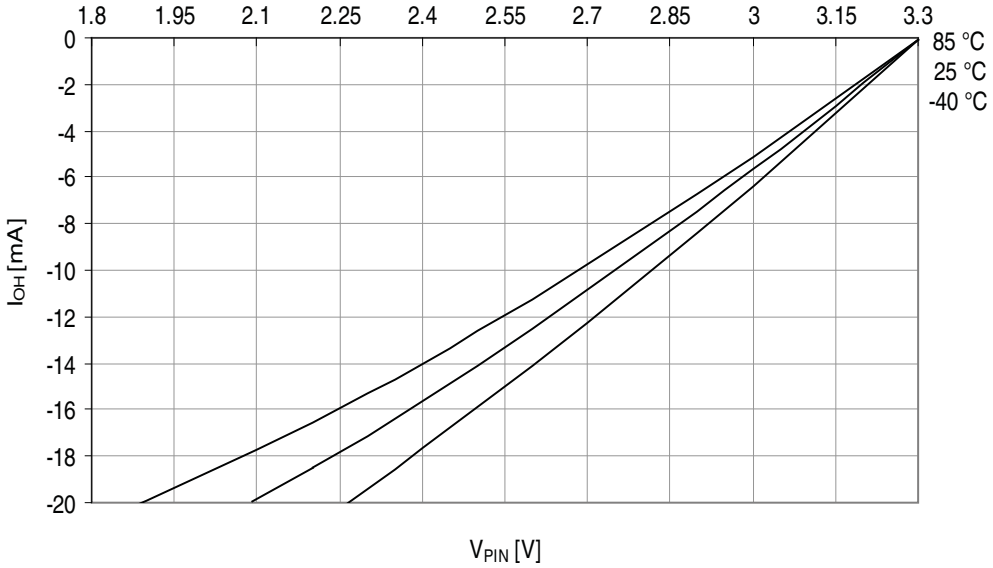


Figure 36-18. I/O Pin Output Voltage vs. Source Current

T = 25°C

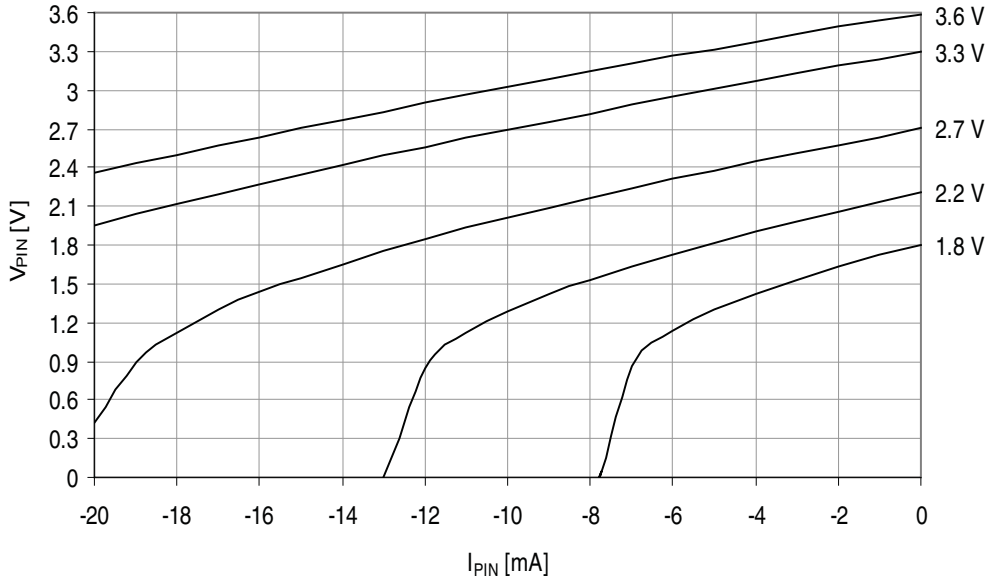


Figure 36-19. I/O Pin Output Voltage vs. Sink Current

Vcc = 1.8V

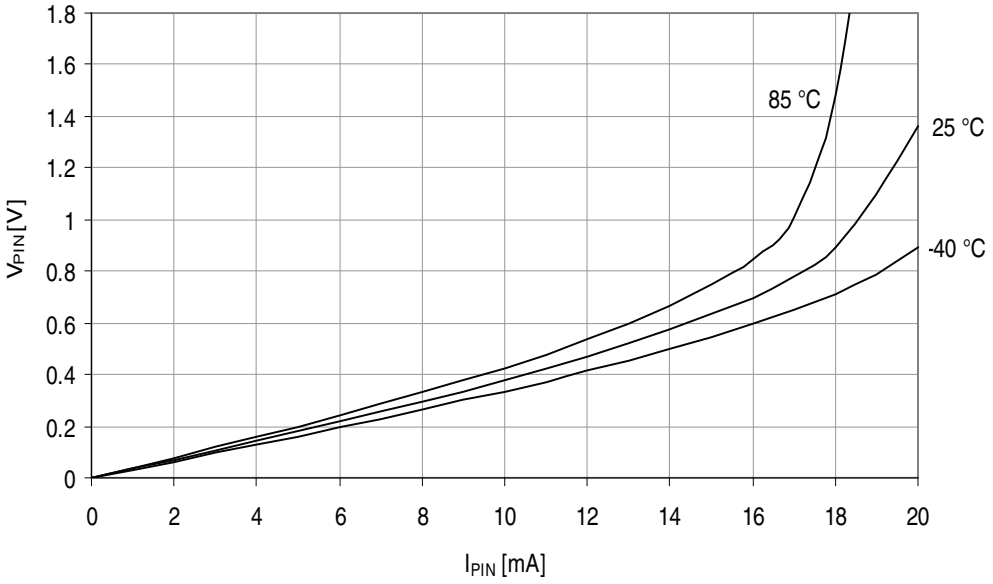


Figure 36-20. I/O Pin Sink Current vs. Output Voltage

Vcc = 1.8V

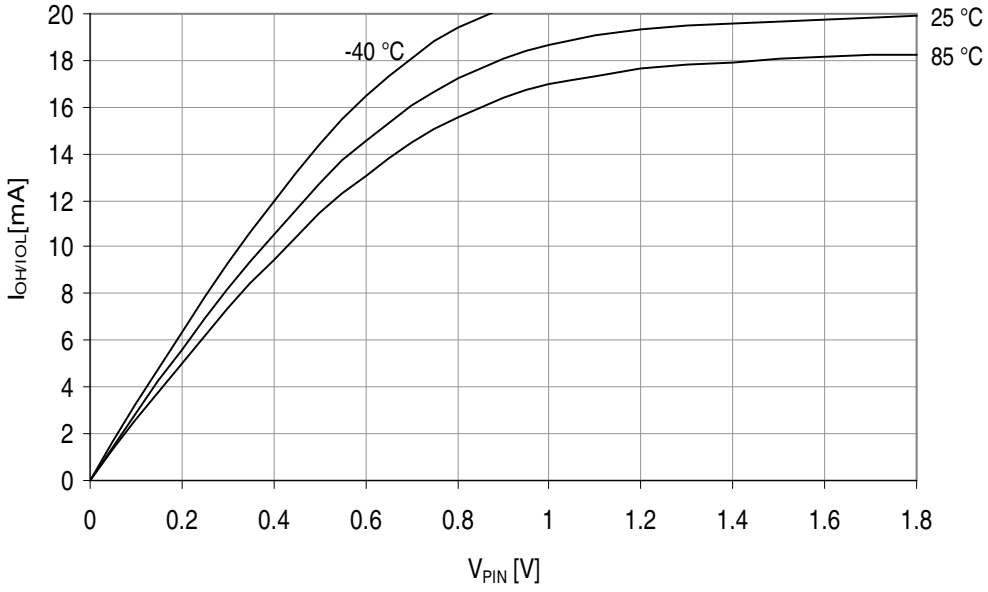


Figure 36-21. I/O Pin Sink Current vs. Output Voltage

Vcc = 3.0V

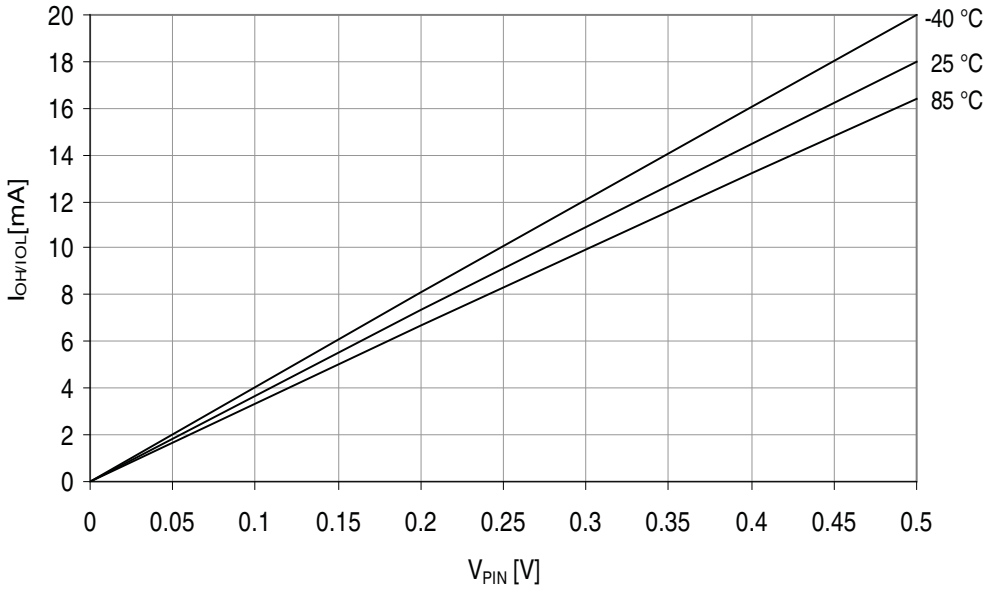
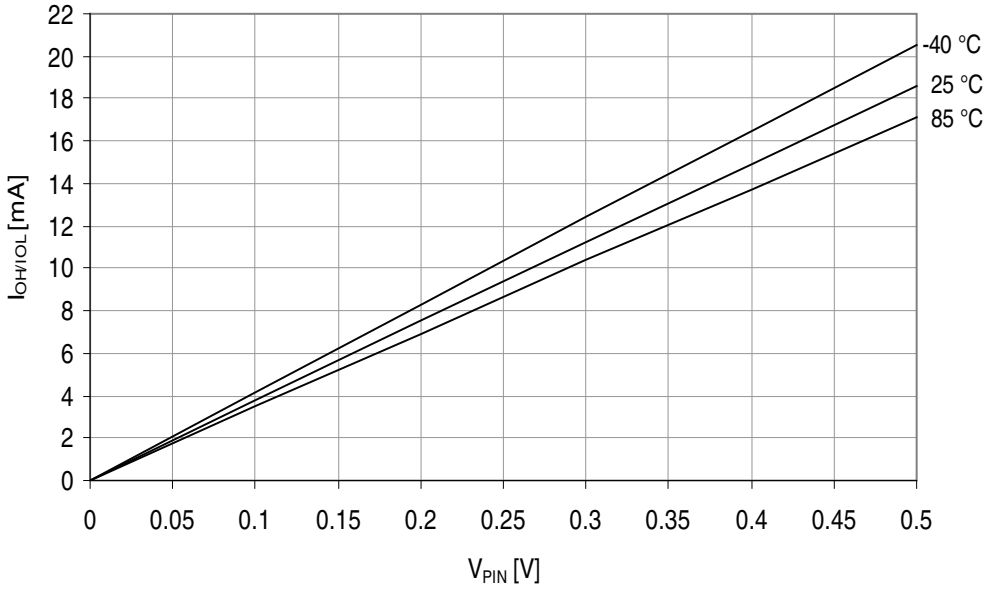


Figure 36-22. I/O Pin Sink Current vs. Output Voltage

Vcc = 3.3V



36.6 Pin Thresholds and Hysteresis

Figure 36-23. I/O Pin Input Threshold Voltage vs. V_{CC}

T = 25°C

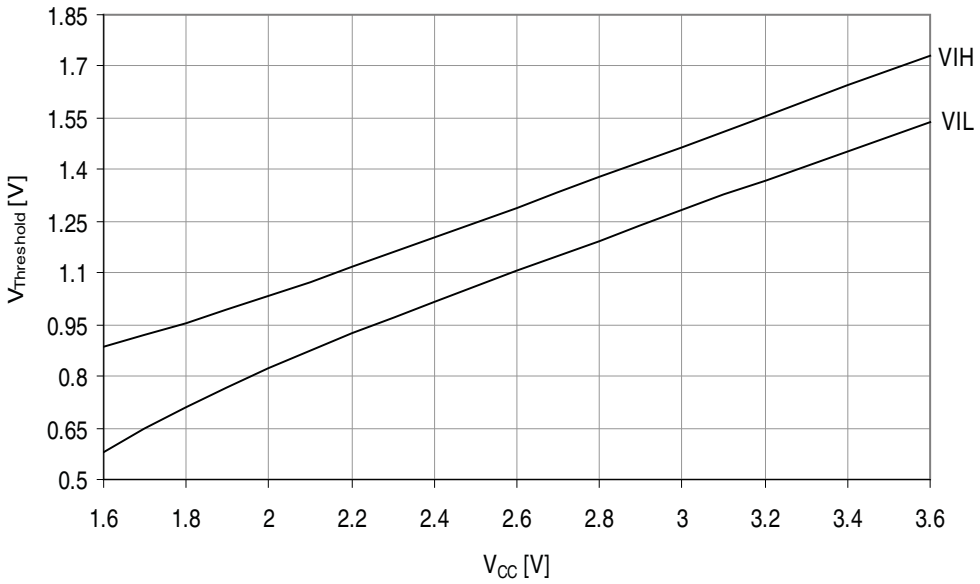


Figure 36-24. I/O Pin Input Hysteresis vs. V_{CC}

T = 25°C

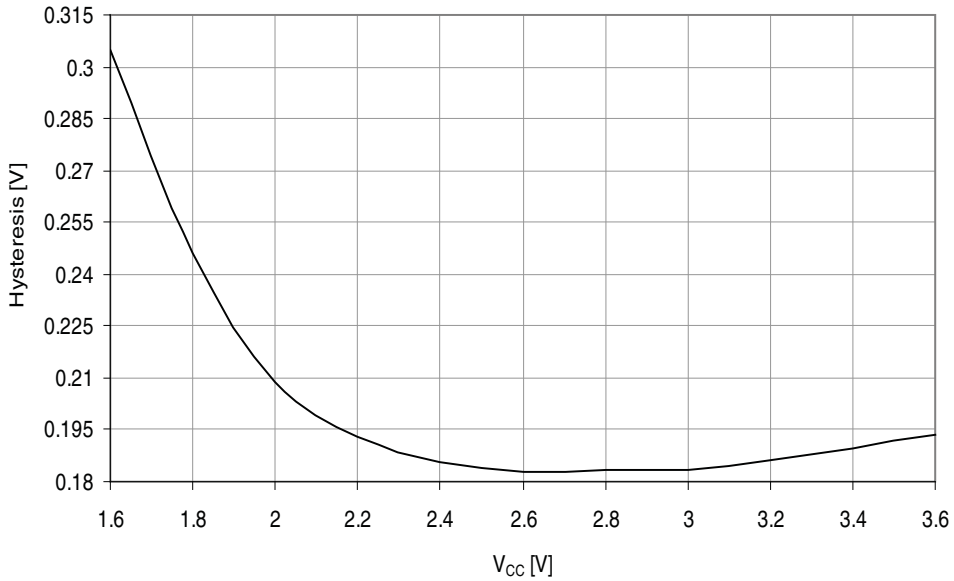


Figure 36-25. Reset Input Threshold Voltage vs. V_{CC}

V_{IH} - I/O Pin Read as "1"

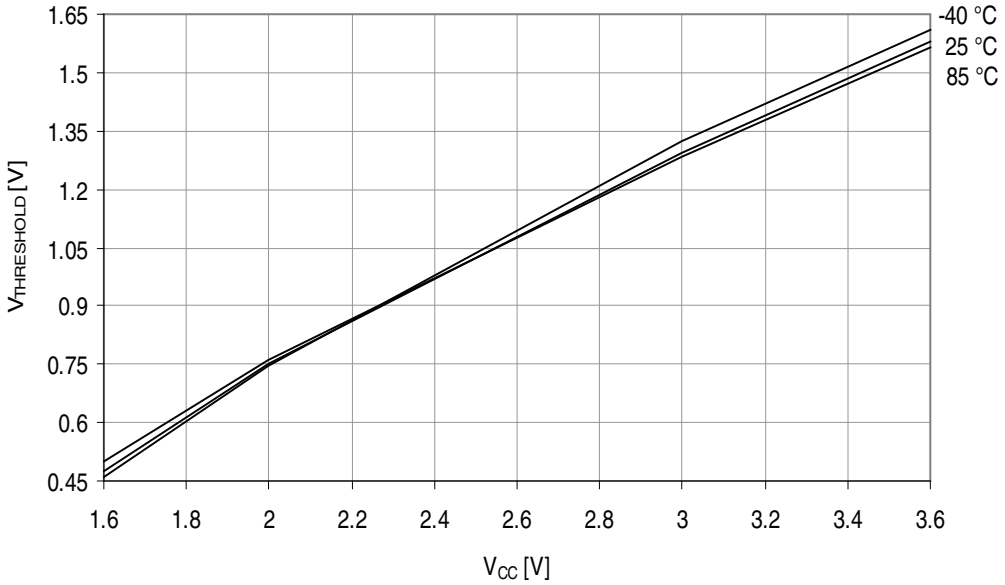
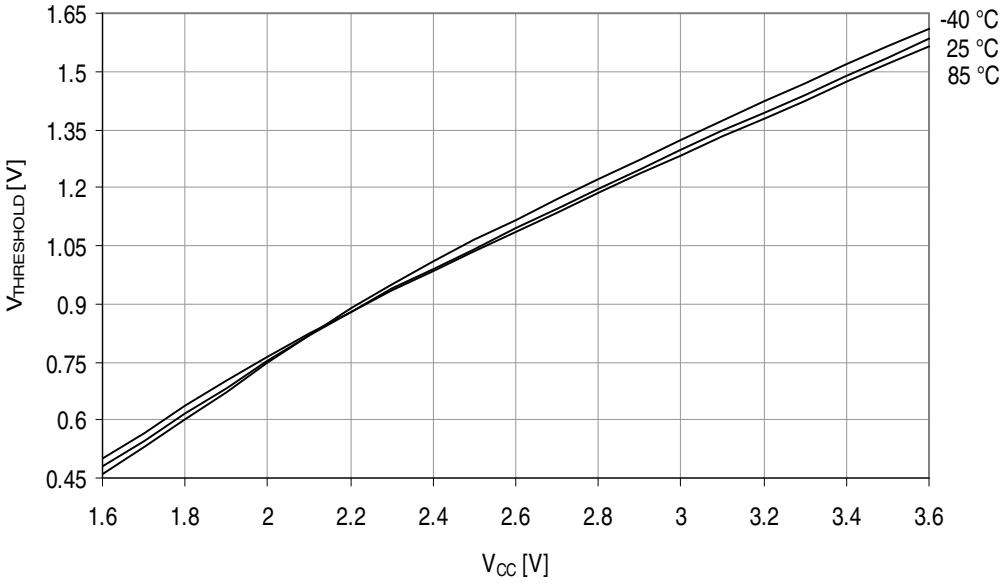


Figure 36-26. Reset Input Threshold Voltage vs. V_{CC}

V_{IL} - I/O Pin Read as "0"



36.7 Bod Characteristics

Figure 36-27. BOD Thresholds vs. Temperature

BOD Level = 1.6V

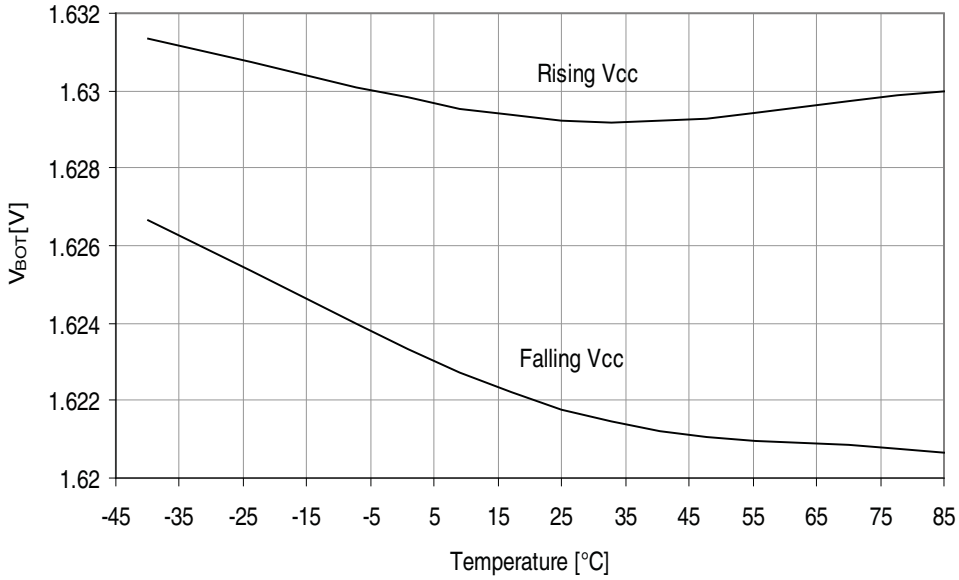
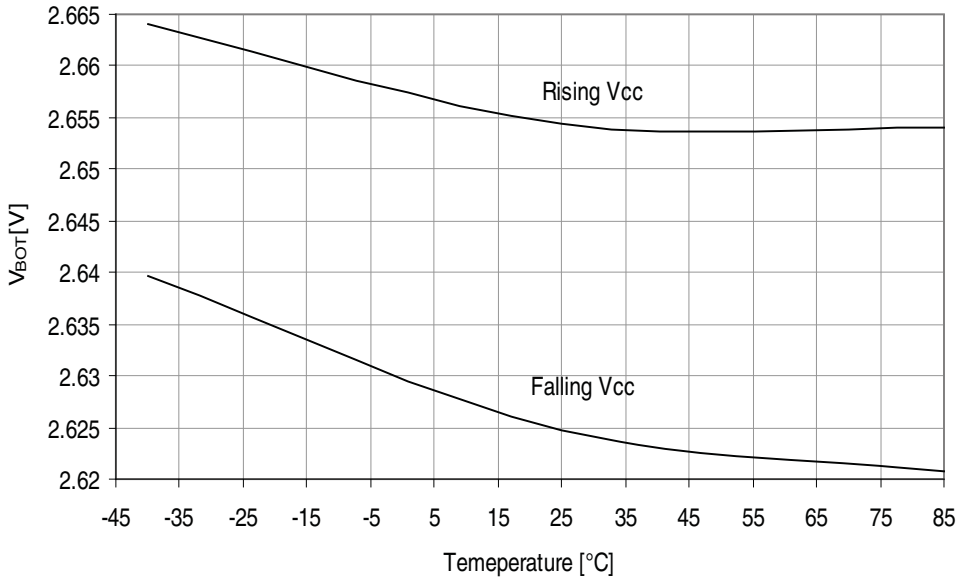


Figure 36-28. BOD Thresholds vs. Temperature

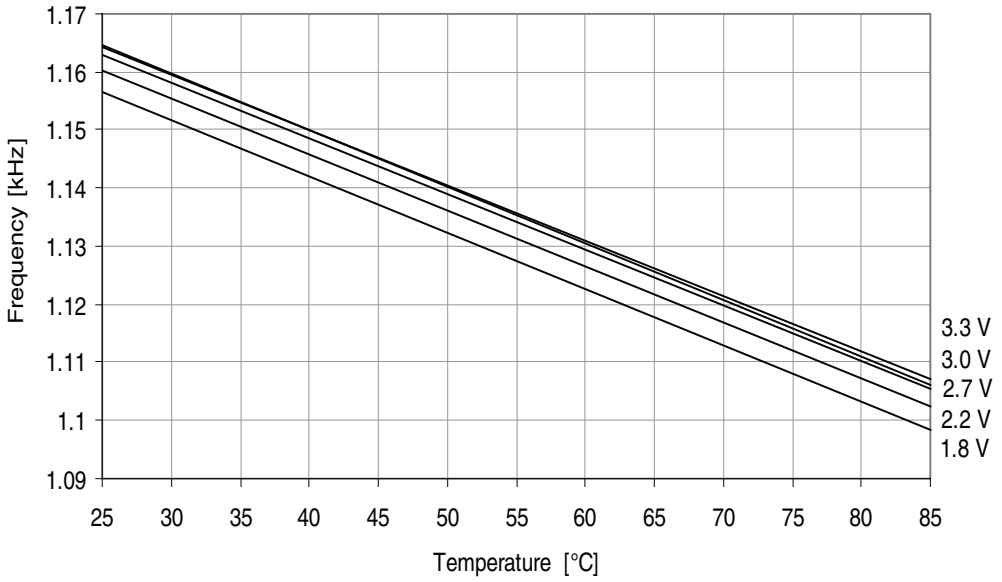
BOD Level = 2.6V



36.8 Oscillators

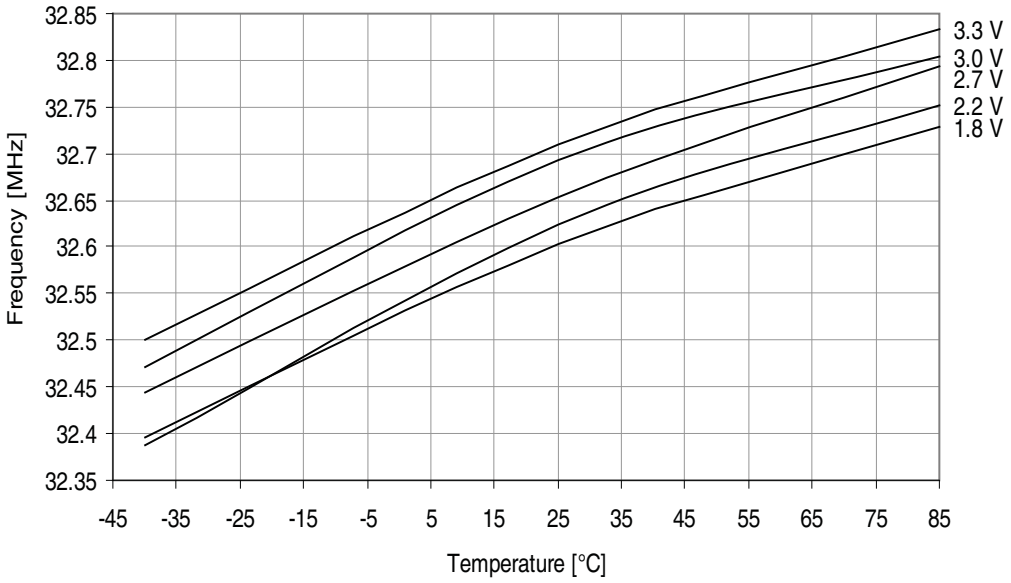
36.8.1 Internal 1kHz Oscillator

Figure 36-29. 1kHz Ouput from Internal ULP Oscillator Frequency vs. Temperature



36.8.2 32.768kHz Internal Oscillator

Figure 36-30. 32.768kHz Internal Oscillator Frequency vs. Temperature



36.8.3 2MHz Internal Oscillator

Figure 36-31. 2MHz Internal Oscillator CALA Calibration Step Size

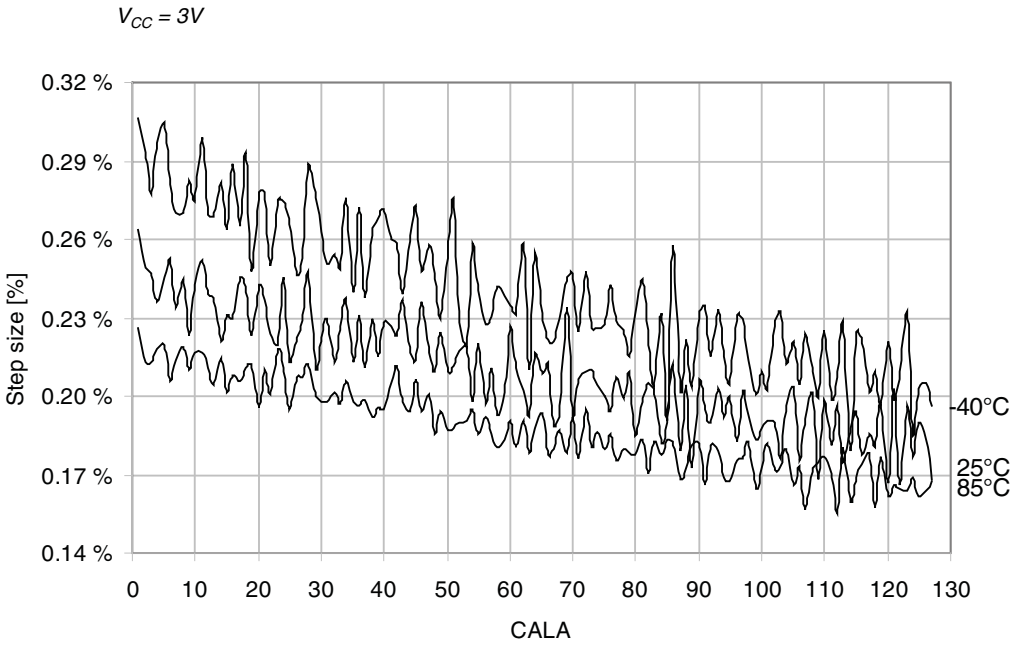


Figure 36-32. 2MHz Internal Oscillator Frequency vs. Temperature

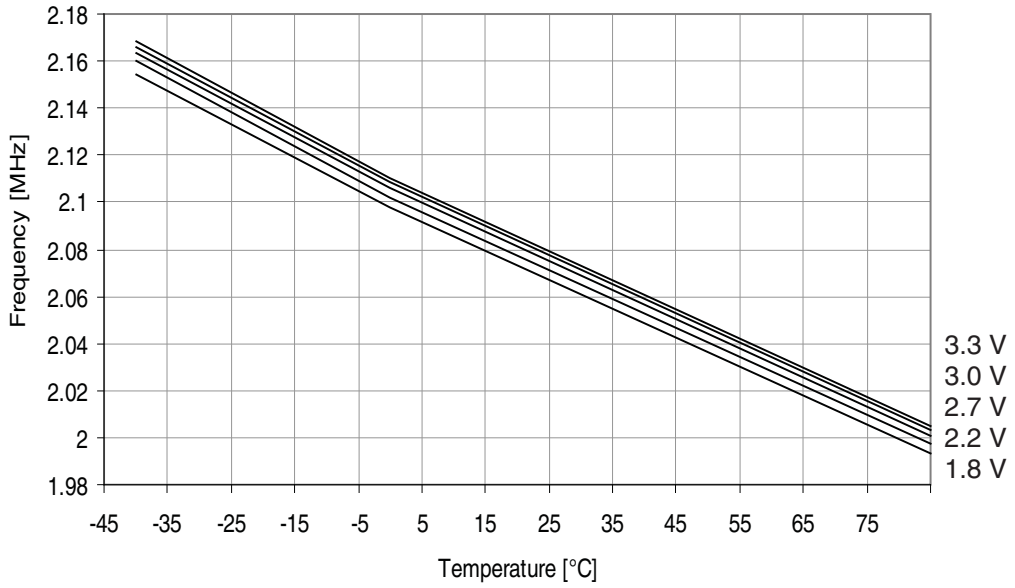
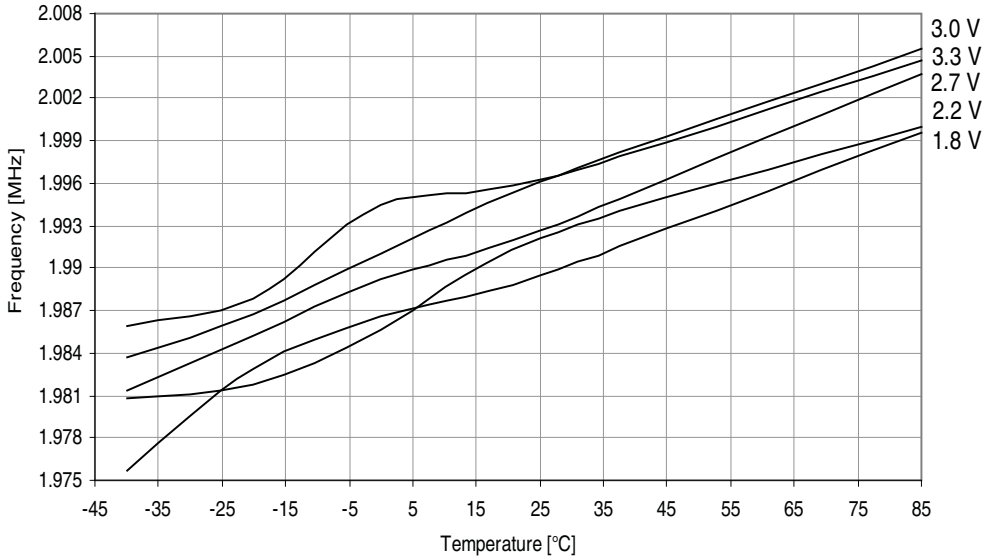


Figure 36-33. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from 32.768kHz internal oscillator



36.8.4 32MHZ Internal Oscillator

Figure 36-34. Internal 32MHz Oscillator Frequency vs. Temperature

DFLL disabled

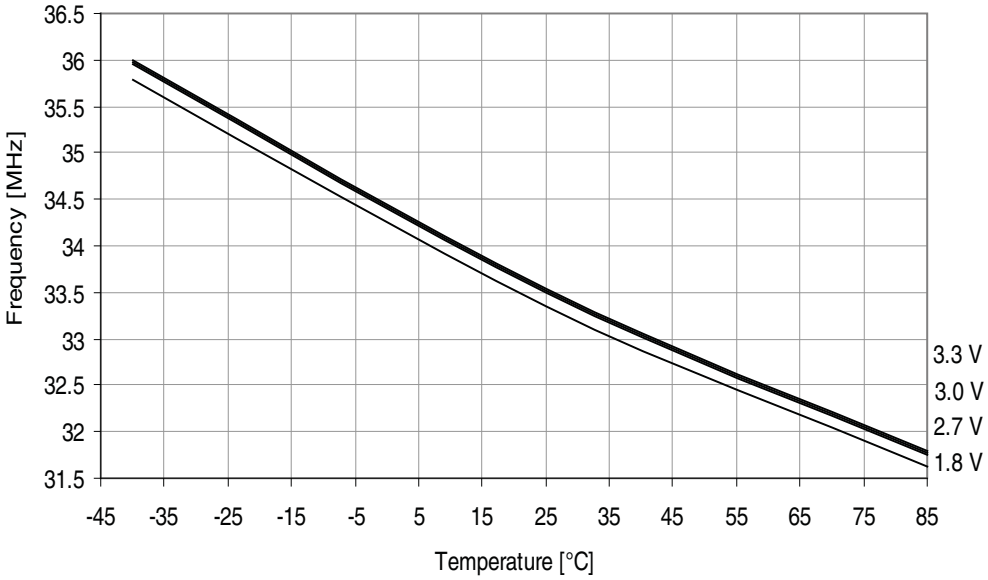


Figure 36-35. 32MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from 32.768kHz internal oscillator

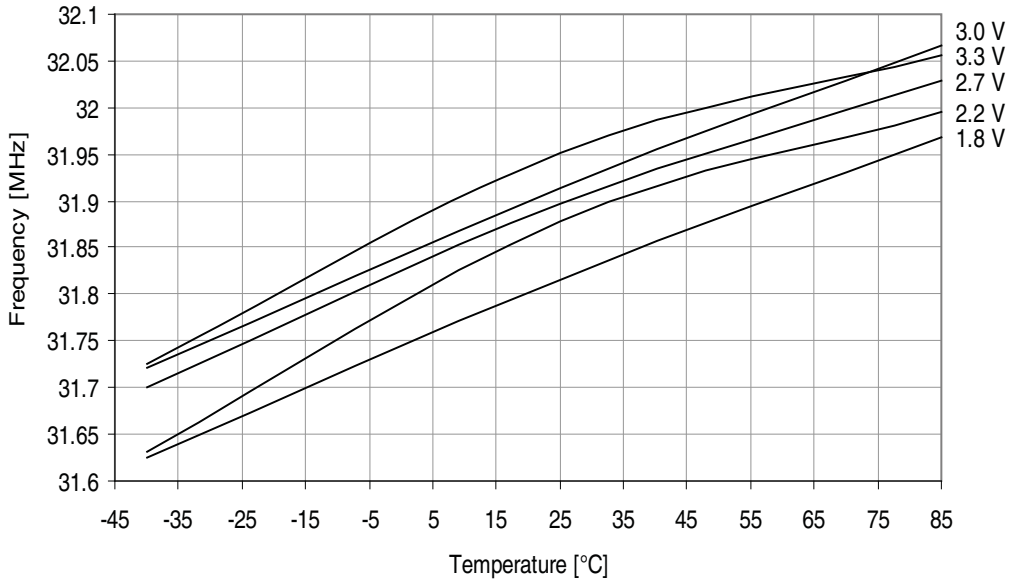
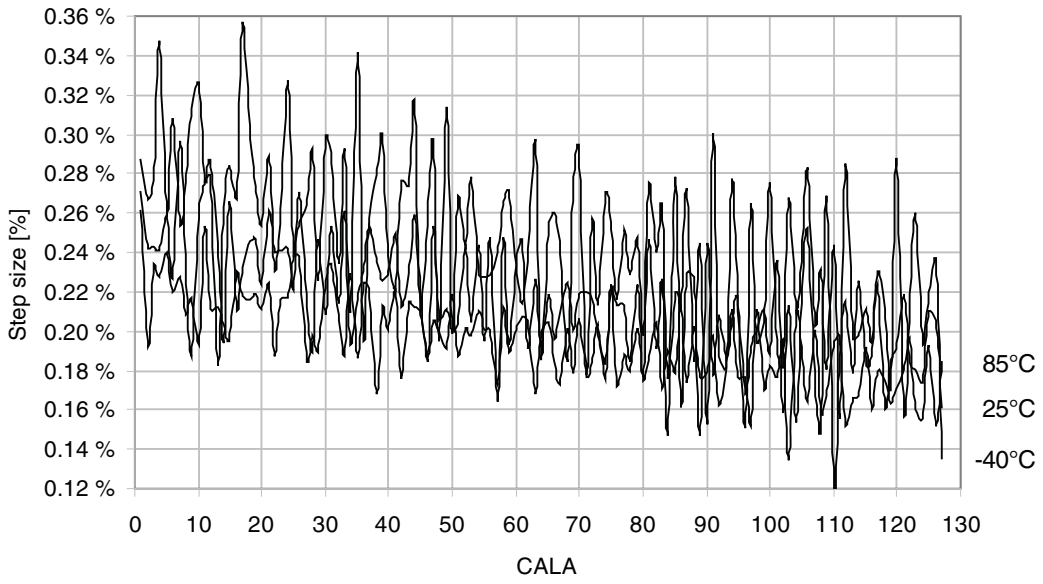


Figure 36-36. 32MHz Internal Oscillator CALA Calibration Step Size

V_{CC} = 3.0V



36.8.5 32MHz Internal Oscillator Calibrated to 48MHZ

Figure 36-37. 48MHz Internal Oscillator Frequency vs. Temperature
DFLL disabled

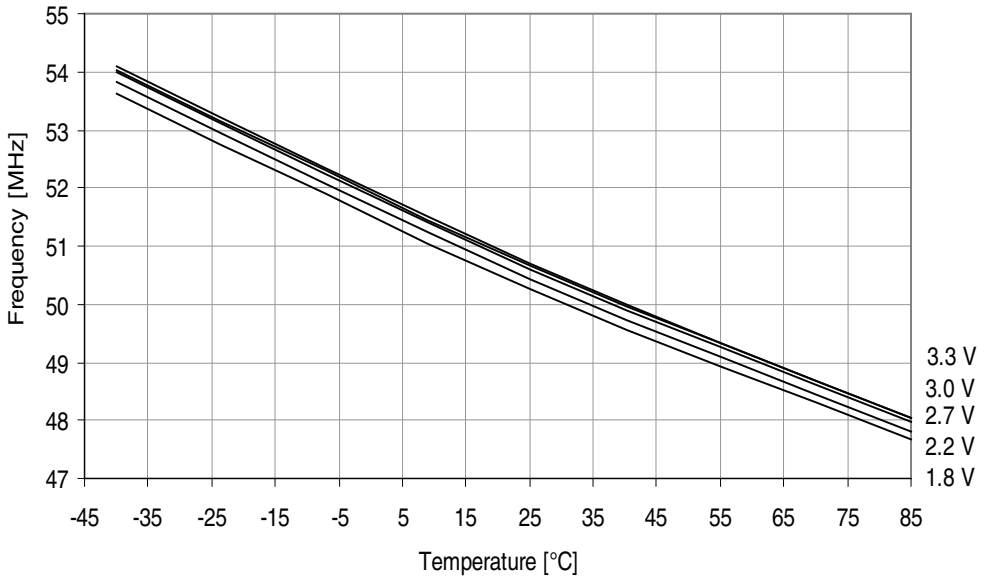
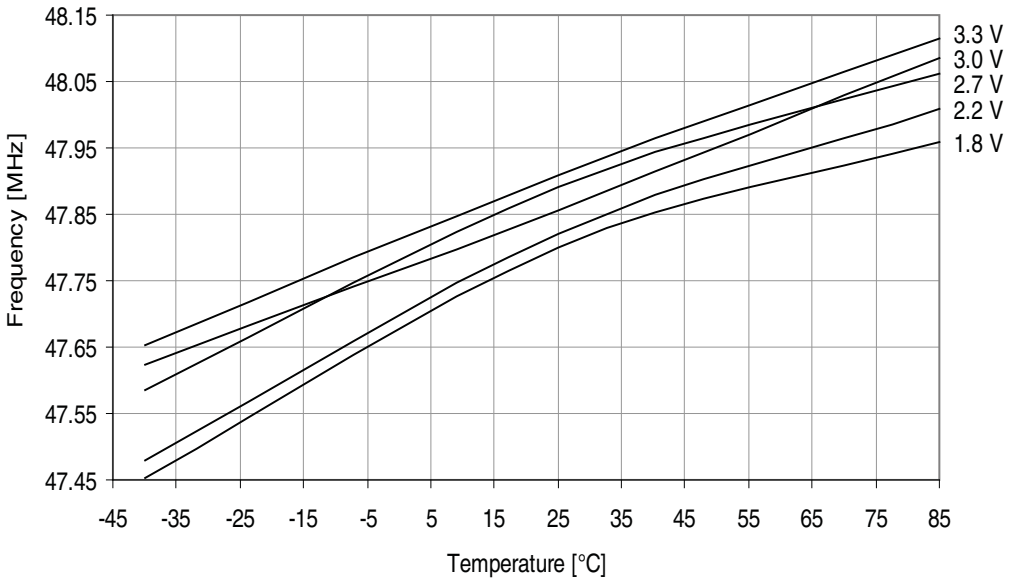


Figure 36-38. 48MHz Internal Oscillator Frequency vs. Temperature
DFLL enabled, from 32.768kHz internal oscillator



36.9 Analog comparator characteristics

Figure 36-39. AC propagation delay vs. Vcc
High-speed mode

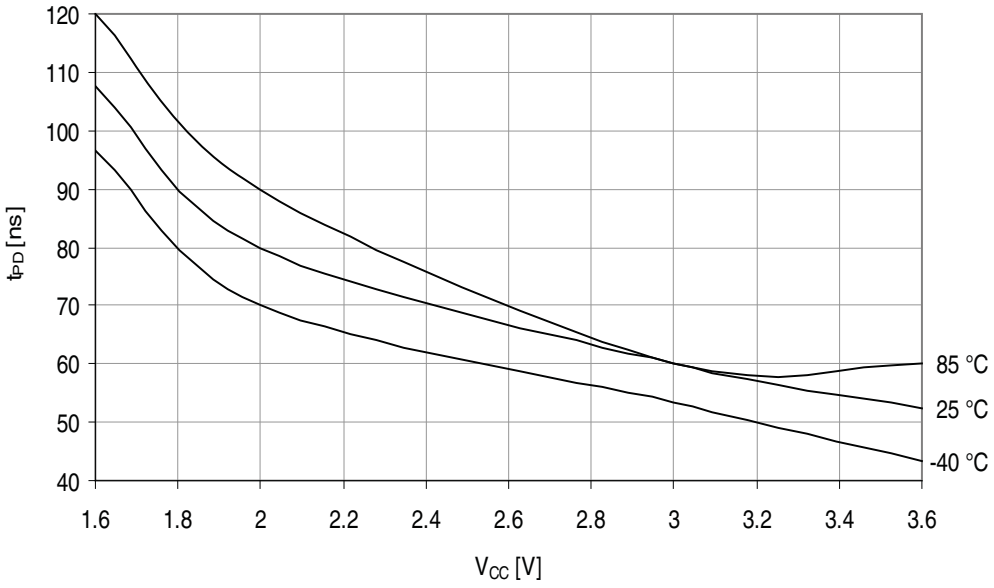


Figure 36-40. AC propagation delay vs. Temperature
High-speed mode

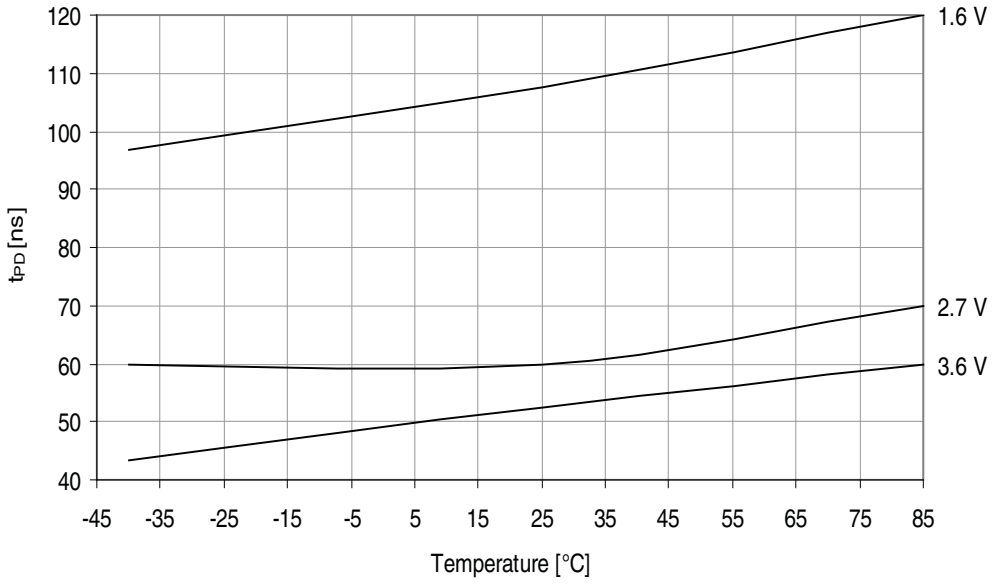


Figure 36-41. AC current consumption vs. Vcc

Low-power Mode mode

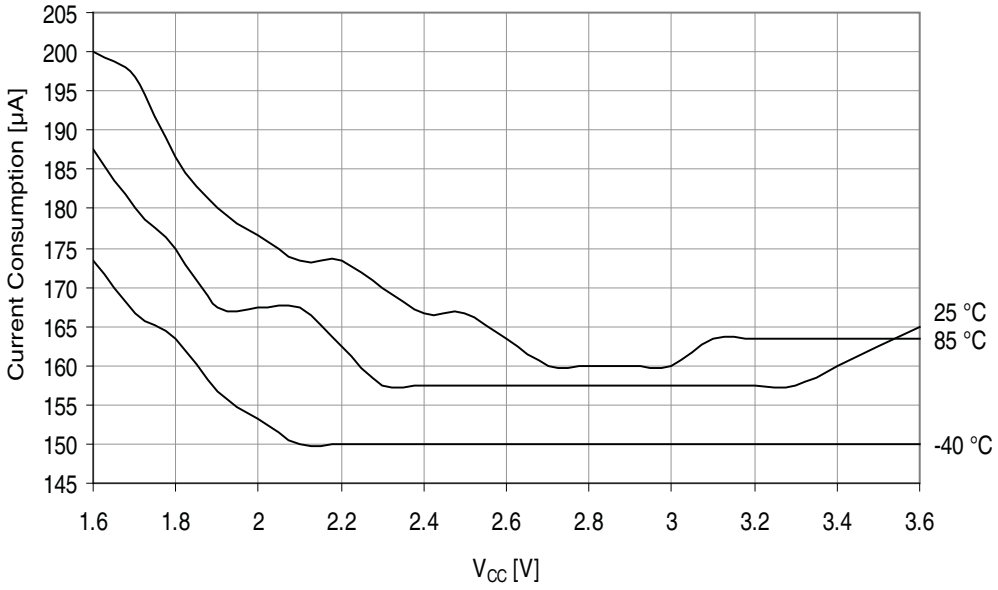
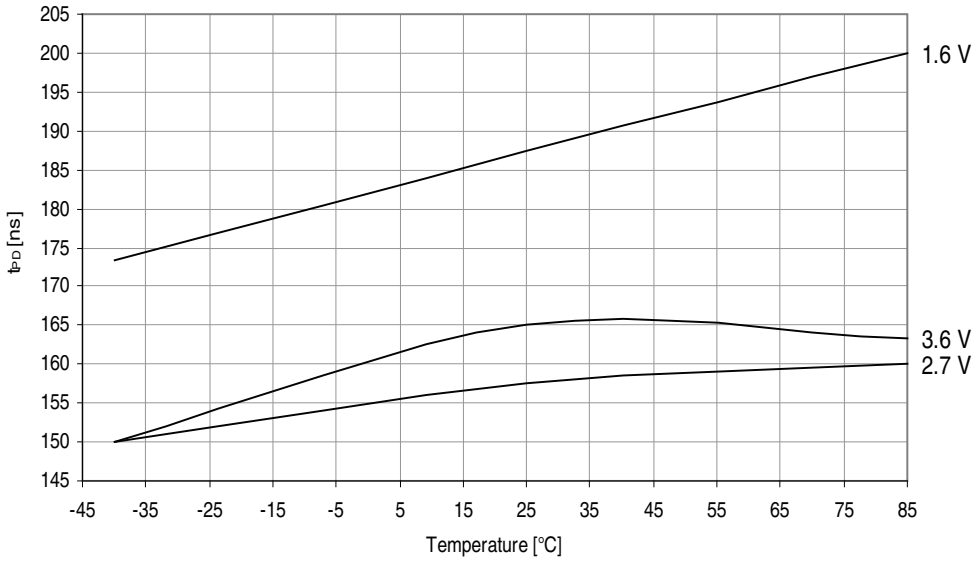


Figure 36-42. AC propagation delay vs. Temperature

Low-spower mode



36.10 ADC Characteristics

Figure 36-43. Gain Error vs. External VREF

Differential Mode, V_{CC} = 3.6V, External reference

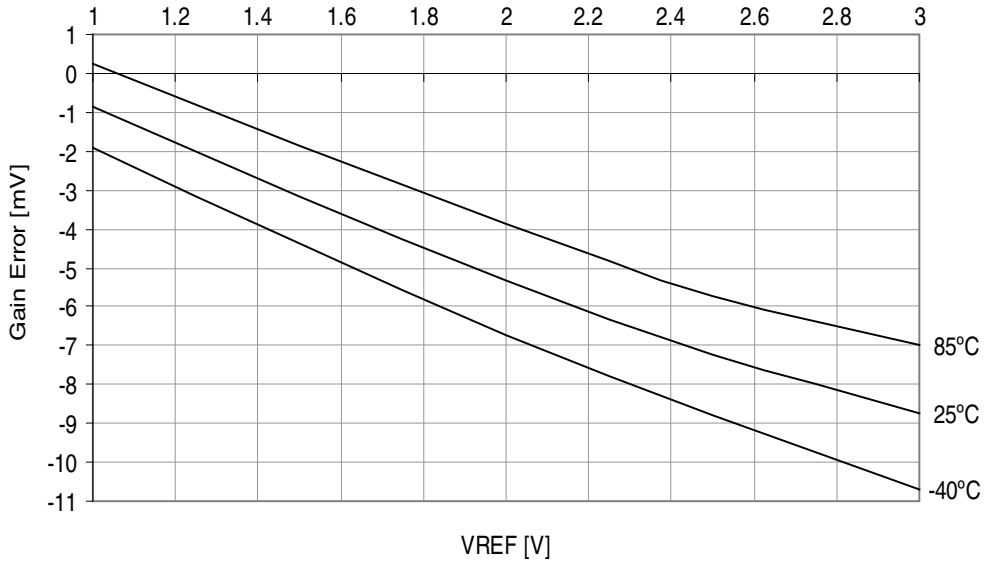


Figure 36-44. Gain Error vs. V_{CC}

Differential Mode, External reference

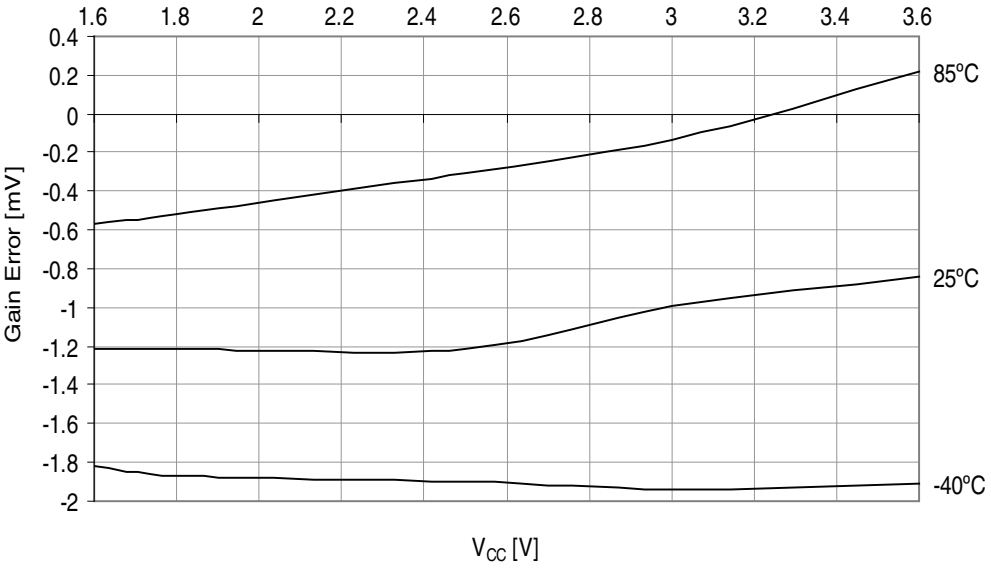


Figure 36-45. Offset vs. External VREF

Differential Mode, V_{CC} = 3.6V, External reference

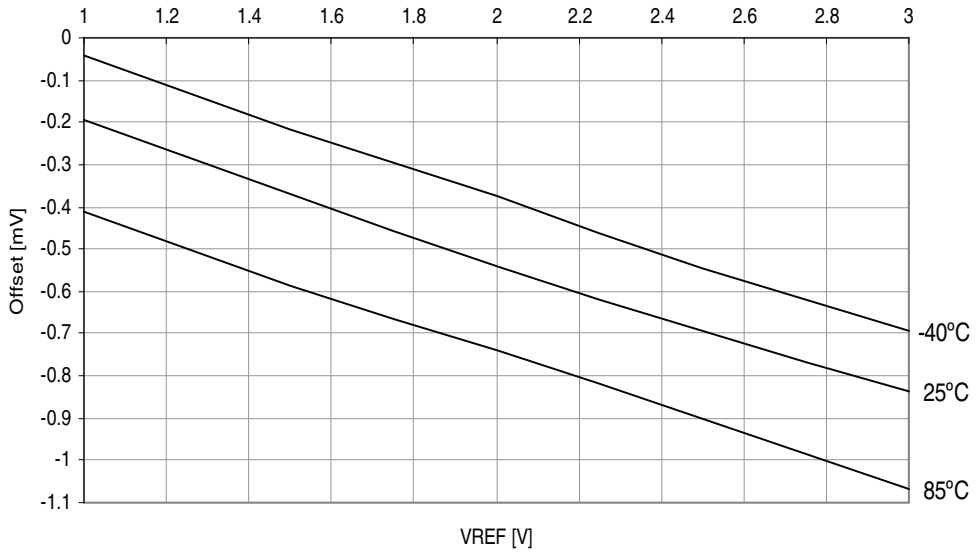


Figure 36-46. Offset vs. V_{CC}

Differential Mode, V_{CC} = 3.6V, External reference.

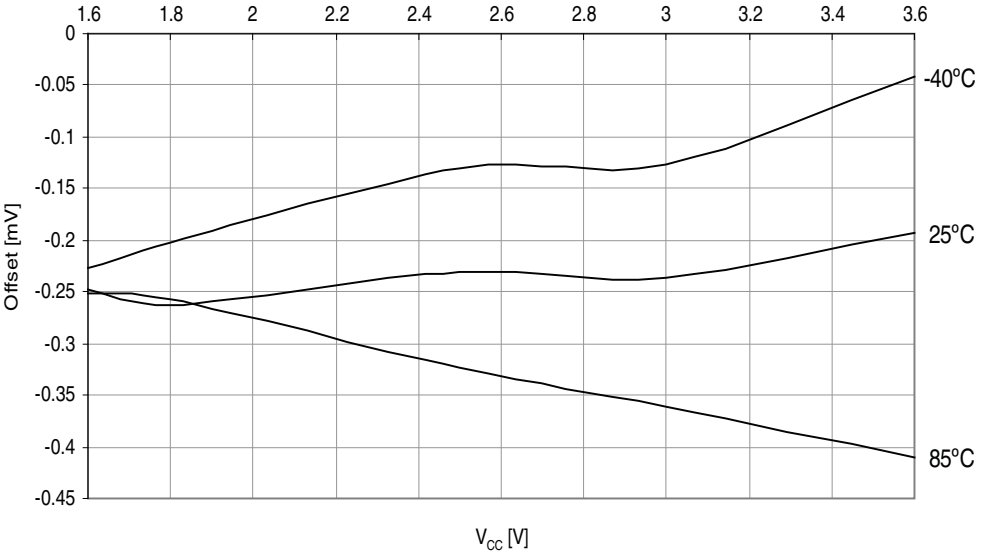


Figure 36-47. Gain Error vs. Temperature

Differential Mode, V_{CC} = 3.6V, External reference

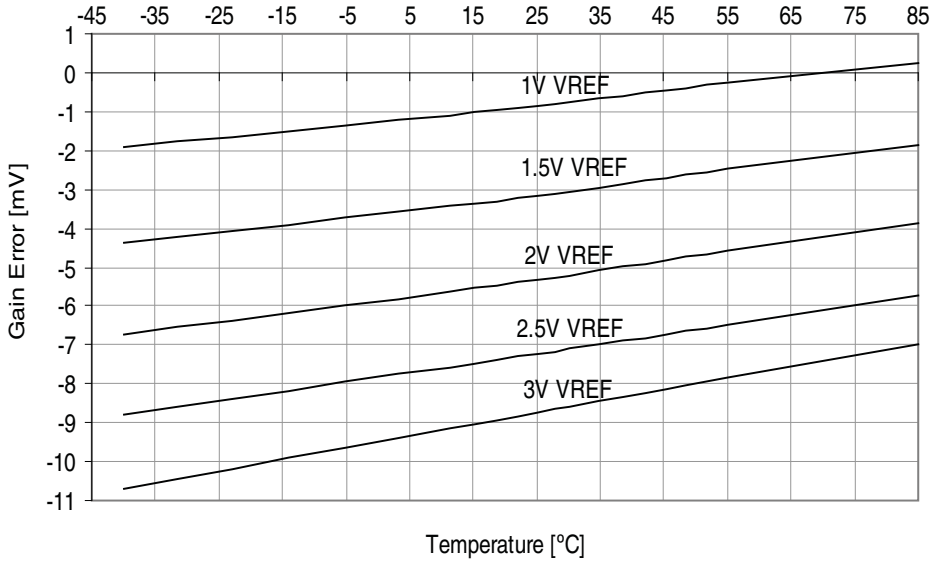


Figure 36-48. INL vs. External VREF

Differential Mode, V_{CC} = 3.6V

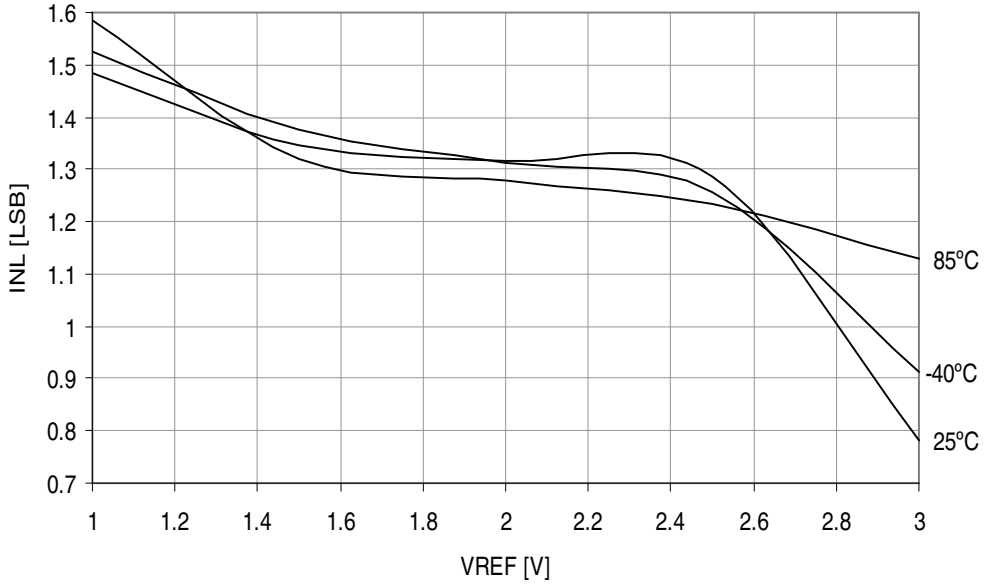
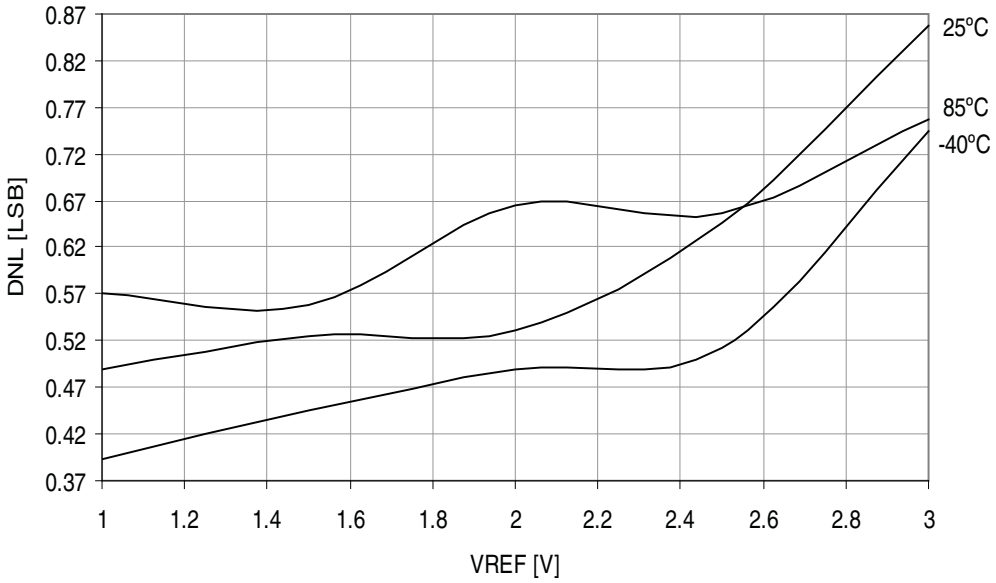


Figure 36-49. DNL vs. External VREF

Differential Mode, V_{CC} = 3.6V



36.11 DAC characteristics

Figure 36-50. DNL vs. External VREF

V_{CC} = 3.6V, External reference

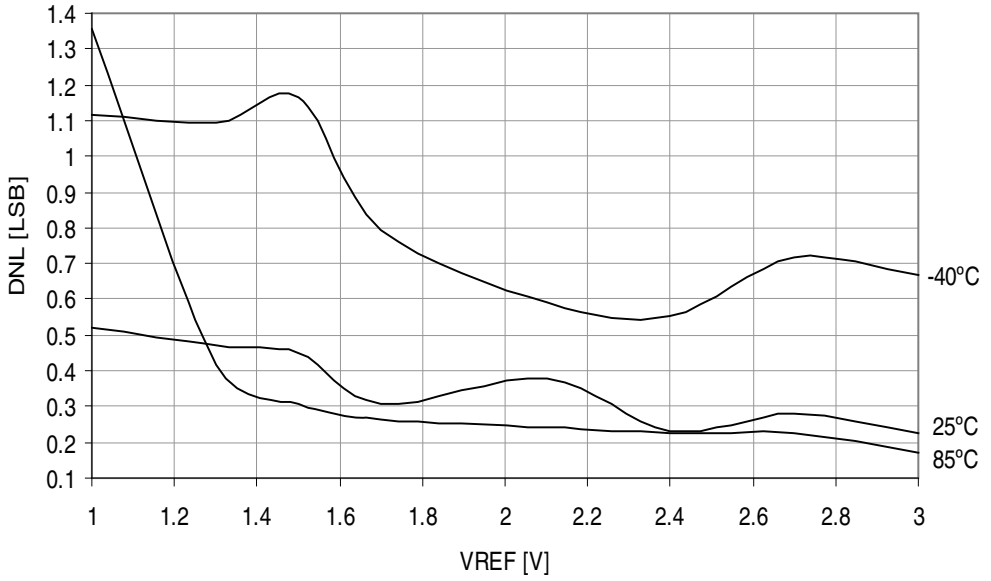
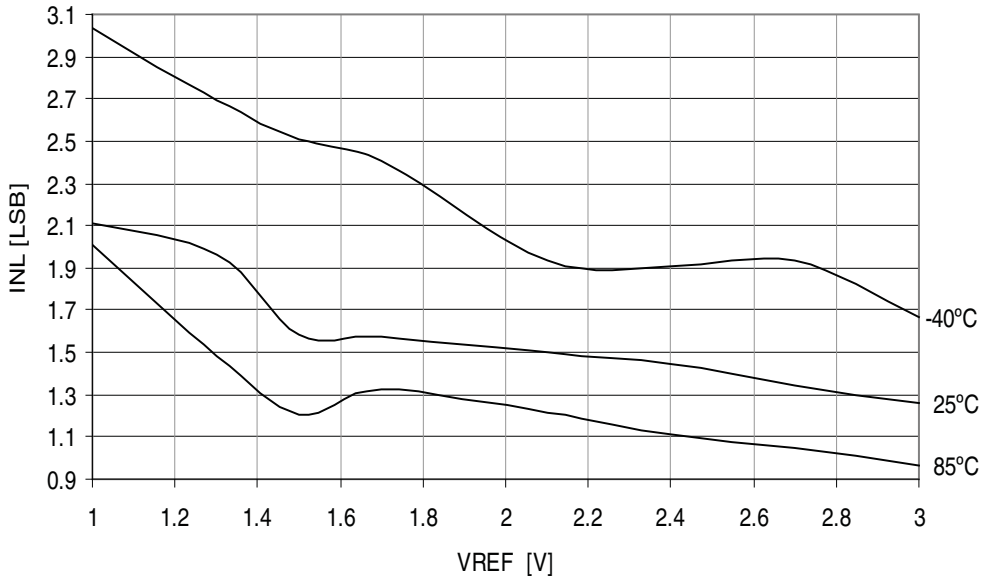


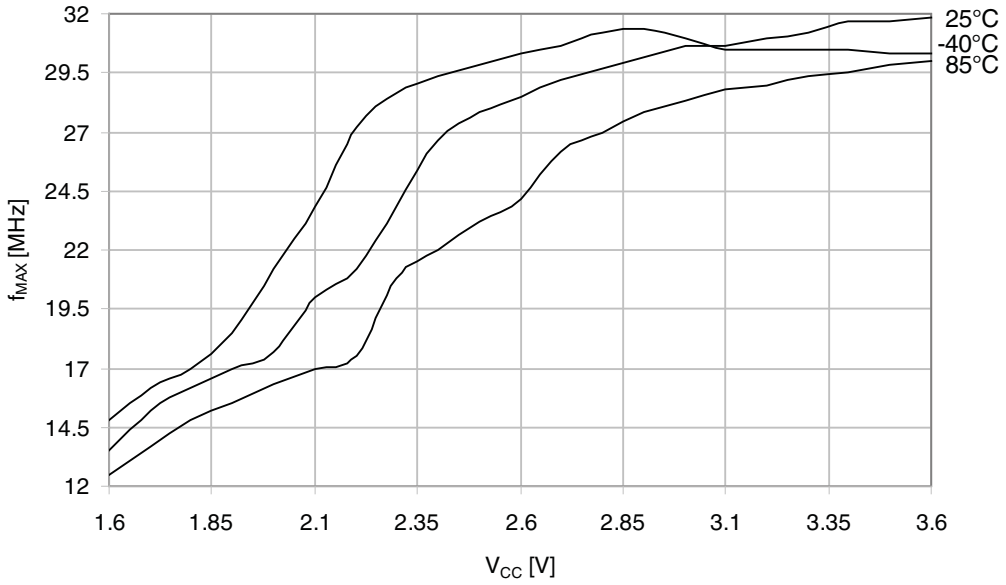
Figure 36-51. INL vs. External VREF

V_{CC} = 3.6V, External reference



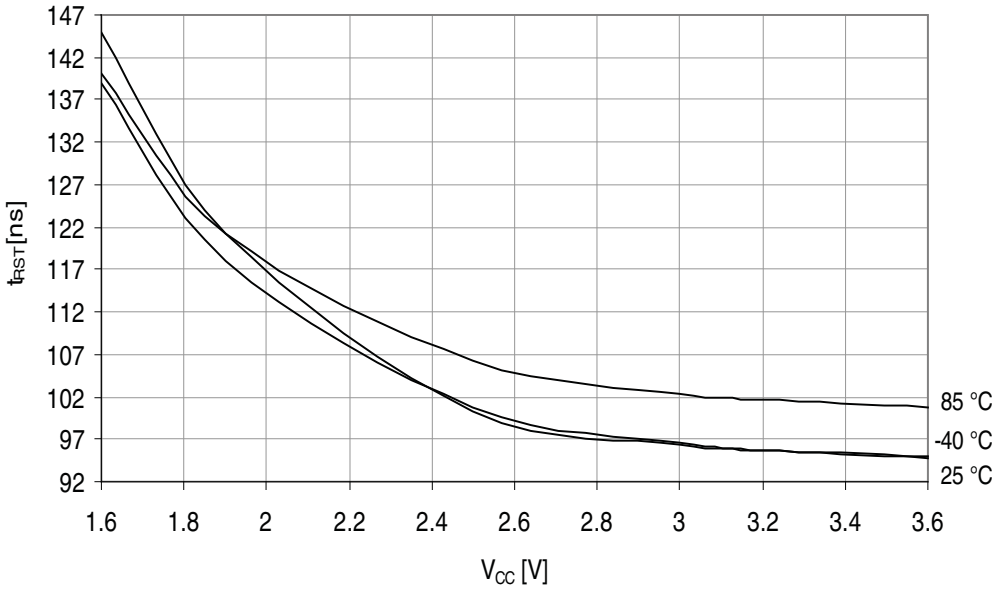
36.12 PDI characteristics

Figure 36-52. Maximum PDI speed vs. Vcc



36.13 Reset pin Pulsewidth

Figure 36-53. Minimum Reset Pulse Width vs. Vcc



37. Errata

37.1 ATxmega64A3U, ATxmega128A3U, ATxmega192A3U, ATxmega256A3U

37.1.1 Rev. G

- **AWeX fault protection restore is not done correct in Pattern Generation Mode**

1. **AWeX fault protection restore is not done correctly in Pattern Generation Mode**
   When a fault is detected the OUTOVEN register is cleared, and when fault condition is cleared, OUTOVEN is restored according to the corresponding enabled DTI channels. For Common Waveform Channel Mode (CWCM), this has no effect as the OUTOVEN is correct after restoring from fault. For Pattern Generation Mode (PGM), OUTOVEN should instead have been restored according to the DTILSBUF register.

   Problem fix/Workaround
   For CWCM no workaround is required.

   For PGM in latched mode, disable the DTI channels before returning from the fault condition. Then, set correct OUTOVEN value and enable the DTI channels, before the direction (DIR) register is written to enable the correct outputs again.

   For PGM in cycle-by-cycle mode there is no workaround.

37.1.2 Rev. A-F

Not sampled.

38. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

38.1 8386A – 07/11

1. Initial revision.

Table of Contents

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